Lumped Versus Distributed *RC* and *RLC* Interconnect Impedances

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Abstract— **A Fourier analysis of on-chip signals in CMOS integrated circuits is presented in this paper. It is demonstrated that on-chip signals can be approximated by a Fourier series up to the 15th harmonic component. The effective load impedance characterizing a distributed *RC* and *RLC* line driven by a CMOS logic gate is based on a Fourier analysis of the on-chip signals. The voltage waveform based on the effective load impedance approaches a distributed *RC* and *RLC* line approximated by sections of lumped *RC* and *RLC* elements.**

I. Introduction

As integrated circuit technologies continue to improve, the feature size of MOS transistors and interconnect lines has decreased [1, 2]. Since the chip size and integration density have both increased dramatically, the average interconnect length has not scaled down with decreasing feature size. Therefore, on-chip interconnect has become increasingly important [3]. The delay of these highly scaled circuits is now dominated by the interconnect impedances rather than the active transistors [2, 4].

On-chip interconnections in CMOS integrated circuits can be modeled as distributed lines [5]. However, a distributed model causes significant computational complexity in characterizing the propagation delay and voltage waveform of a CMOS logic gate driving on-chip interconnect since the MOS transistors are nonlinear devices. Nonlinear circuit theory is therefore required to solve the circuit equations characterizing this system. In order to develop analytic expressions characterizing the behavior of a CMOS logic gate driving an *RC* or *RLC* interconnect, some simplifying approaches need to be applied.

A Fourier analysis of typical on-chip signals in CMOS integrated circuits is presented in this paper. On-chip signals are approximated by a Fourier series up to the 15th harmonic component. The effective load impedance of a distributed *RC* and *RLC* line driven by a CMOS logic gate is based on this Fourier analysis of the on-chip signals, which includes the frequency dependence of the interconnect impedances. The effective load impedance model presented here considers the input transition time and the distributed characteristics of the on-chip interconnections. The voltage waveform based on the effective load impedance model is similar to a distributed *RC* and *RLC* line approximated by sections of lumped *RC* and *RLC* elements.

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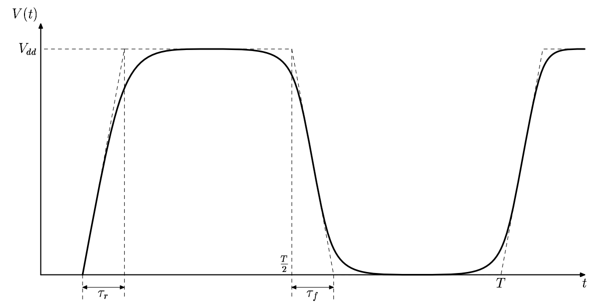


Fig. 1. Typical voltage waveform of an on-chip signal in a CMOS integrated circuit.

A Fourier analysis of typical on-chip signals in CMOS integrated circuits is presented in Section II. The effective load impedance of a distributed *RC* and *RLC* line is developed in Section III based on a Fourier analysis of the on-chip signals. The effective load impedance model is also compared in this section to a distributed line model followed by some concluding remarks in Section IV.

II. Fourier Analysis of On-Chip Signals

The solid line shown in Fig. 1 depicts a typical voltage waveform of an on-chip signal in a CMOS integrated circuit. The signal is assumed to behave periodically with a period of T. The dashed line shown in Fig. 1 approximates an on-chip signal, with rising and falling transition times τ_r and τ_f, respectively. The signal represented by the dashed line shown in Fig. 1 can be expressed as

$$V(t) = \begin{cases} \frac{t}{\tau_r} V_{dd} & 0 \le t \le \tau_r, \\ V_{dd} & \tau_r \le t \le \frac{T}{2}, \\ V_{dd}(1 - \frac{t}{\tau_f} + \frac{T}{2\tau_f}) & \frac{T}{2} \le t \le (\frac{T}{2} + \tau_f), \\ 0 & (\frac{T}{2} + \tau_f) \le t \le T. \end{cases} \quad (1)$$

For on-chip signals in a practical CMOS integrated circuit, τ_r is typically similar to τ_f. Therefore, the Fourier series of $V(t)$ is

$$V(t) = \frac{V_{dd}}{2} + \sum_{\substack{m=2k+1 \\ k=0}}^{k=\infty} \frac{T}{\tau_r} \frac{V_{dd}}{m^2 \pi^2} [(\cos m\omega_o \tau_r - 1) \cos m\omega_o t + (\sin m\omega_o \tau_r) \sin m\omega_o t], \quad (2)$$

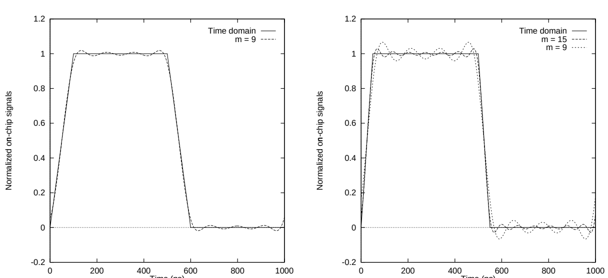
where $\omega_o = 2\pi/T$. The amplitude of the mth order harmonic component is

$$A_m = \frac{T}{\tau_r}\frac{V_{dd}}{m^2\pi^2}\left[(1-\cos m\omega_o\tau_r) + |\sin m\omega_o\tau_r|\right]\frac{\sqrt{2}}{2}, \tag{3}$$

where m is an odd number. Note that the amplitude of the DC component is $V_{dd}/2$ where A_m depends upon the ratio of T over τ_r, which means significantly higher order harmonic components are necessary for short transition times. Since A_m deceases quadratically with m, $V(t)$ can therefore be approximated by the first several higher order harmonic components.

For the condition of $\tau_r/T = 0.1$ ($\tau_r = 100$ ps at a one gigahertz operating frequency), the Fourier series with $m = 9$ is compared to a time domain waveform in Fig. 2(a). Note that the waveform derived from the Fourier series is quite close to the voltage waveform derived in the time domain with $m = 9$. If τ_r/T is greater than 0.1, a Fourier series with $m = 9$ can be used to model the on-chip signals in a CMOS integrated circuit.

If the transition time of the on-chip signals is quite short, for example, if $\tau_r/T = 0.05$ ($\tau_r = 50$ ps at a one gigahertz operating frequency), the waveforms derived from the Fourier series with $m = 9$ and $m = 15$ are similar to the time domain waveform as shown in Fig 2(b). Note that the waveform determined by the Fourier series with $m = 15$ is quite accurate as compared to the time domain waveform. Therefore, if τ_r/T is less than 0.1, the Fourier series with $m = 15$ can be used to approximate on-chip signals in a CMOS integrated circuit.



(a) $\tau_r/T = 0.1$ and $m = 9$

(b) $\tau_r/T = 0.05$, $m = 9$, and $m = 15$

Fig. 2. Comparison of signal waveform derived from a Fourier series with the waveform derived from the time domain.

III. Effective Lumped Load Versus Distributed Load

On-chip interconnections can be approximated by sections of lumped circuit elements [1, 5, 6]. Based on a Fourier analysis of the on-chip signal presented in Section II, analytic expressions characterizing the effective load impedance of a distributed line are developed and compared to SPICE for a distributed *RC* and *RLC* line in Sections III-A and III-B, respectively.

A. Distributed RC lines

A distributed *RC* line can be approximated by n sections of lumped *RC* elements as shown in Fig. 3(a) [6]. In order to derive tractable analytic expressions characterizing the output waveform of a CMOS logic gate driving a resistive-capacitive interconnect, an effective load resistance and capacitance are used to approximate a distributed *RC* line as shown in Fig. 3(b).

If the number of sections n is more than two, the effective load resistance and capacitance can be determined from (6) and (7) (see Table I) based on an $L2$ circuit model of a nonuniform *RC* line as shown in Fig. 4(a). In order to simplify the problem, a distributed *RC* line is assumed in this discussion to be uniform.

In practical CMOS integrated circuits, the output transition time of a CMOS logic gate is typically similar to the input transition time [7]. Therefore, if the number of sections n is fixed, the effective load resistance and capacitance can be approximated by

$$R_{\text{eff}} = \left[A_0 R_{\text{eff}}(0) + \sum_{\substack{m=2k+1\\k=0}}^{k=4\text{ or }7} A_m R_{\text{eff}}(m\omega_o)\right] \left(A_0 + \sum_{\substack{m=2k+1\\k=0}}^{k=4\text{ or }7} A_m\right)^{-1}, \tag{8}$$

and

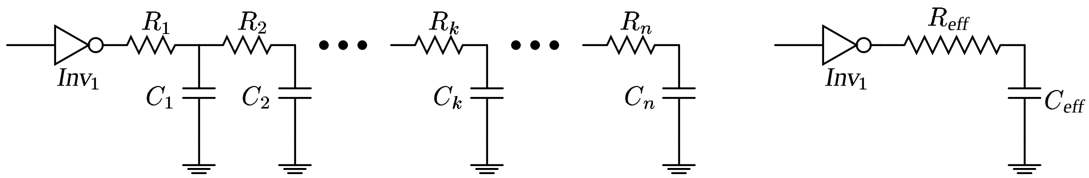
$$C_{\text{eff}} = \left[A_0 C_{\text{eff}}(0) + \sum_{\substack{m=2k+1\\k=0}}^{k=4\text{ or }7} A_m C_{\text{eff}}(m\omega_o)\right] \left(A_0 + \sum_{\substack{m=2k+1\\k=0}}^{k=4\text{ or }7} A_m\right)^{-1}, \tag{9}$$

where $A_0 = V_{dd}/2$ which is the amplitude of the DC component of the on-chip signals in a CMOS integrated circuit.

SPICE simulations based on an effective load resistance and capacitance, determined from (8) and (9), are compared to a distributed *RC* line as shown in Fig. 5. Note that the voltage waveform based on the effective load resistance and capacitance is almost the same as the voltage waveform based on a distributed *RC* line model.

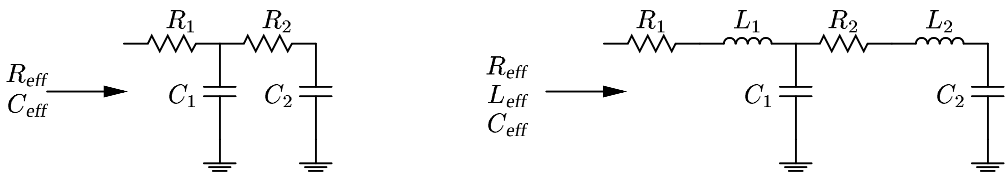
B. Distributed RLC lines

There are two time constants associated with a distributed *RLC* line, an inductive time constant $\sqrt{LC}$ and



(a) (b)

Fig. 3. A resistive-capacitive interconnect line, (a) a distributed *RC* line approximated by n sections of lumped elements, (b) the effective load impedance, R_{eff} and C_{eff}.



(a) (b)

Fig. 4. L2 model of nonuniform *RC* and *RLC* lines, (a) a resistive-capacitive load, (b) an inductive load.

TABLE I

ANALYTIC EXPRESSIONS CHARACTERIZING THE EFFECTIVE LOAD IMPEDANCE OF A DISTRIBUTED *RC* LINE

Number of sections (n)	Analytic Expressions
$n=1$	$R_{\text{eff}}(\omega) = R$ (4) $C_{\text{eff}}(\omega) = C$ (5)
$n \geq 2$	$R_{\text{eff}}(\omega) = R_1 + \frac{R_2}{(R_2\omega C_1)^2 + (\frac{C_1+C_2}{C_2})^2}$ (6) $C_{\text{eff}}(\omega) = \frac{(\omega R_2 C_2)^2 (\frac{C_1}{C_1+C_2})^2 + 1}{(\omega R_2 C_2)^2 \frac{C_1}{C_1+C_2} + 1}(C_1 + C_2)$ (7)

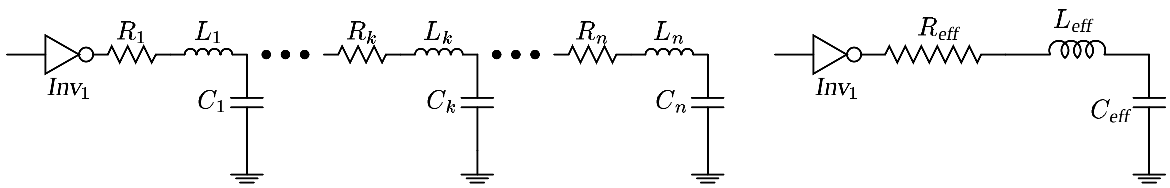
a resistive time constant *RC* [8]. The condition for the on-chip inductance to be significant is if the inductive time constant is comparable to or exceeds the resistive time constant of an on-chip interconnection [9, 10]. A distributed *RLC* line can be approximated by n sections of lumped *RLC* elements as shown in Fig 6(a). In order to analyze the timing and voltage characteristics of a CMOS logic gate driving an inductive interconnect line, a distributed *RLC* line can be approximated by an effective load resistance, inductance, and capacitance, as shown in Fig. 6(b).

The waveforms derived from SPICE simulations based on an effective load resistance, inductance, and capacitance are compared to the waveforms derived from a distributed *RLC* line model as shown in Figs. 7 and 8. Note that the voltage waveform based on an effective load resistance, inductance, and capacitance is almost the same as the voltage waveform based on a distributed *RLC* line model.

Although the effective *RC* or *RLC* impedance is based on an assumption of a uniformly distributed *RC* or *RLC* line, this method can also be applied to a nonuniformly distributed *RC* or *RLC* line. Based on the relative ratio of the interconnect impedance associated with each section of a nonuniformly distributed *RC* or *RLC* line, the effective load impedance can be determined based on an $L2$ circuit model and applying a recursive calculation of the distributed interconnect line.

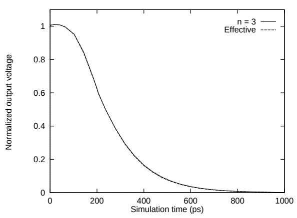
IV. CONCLUSIONS

A Fourier analysis of typical on-chip signals in CMOS VLSI circuits is presented in this paper. The on-chip signals are approximated by a Fourier series up to the 15th harmonic component. The effective load impedance of a distributed *RC* and *RLC* line driven by a CMOS logic gate is presented based on a Fourier analysis of the on-chip signals. The voltage waveform based on the effective load impedance is shown to be quite similar to the voltage waveform of a distributed *RC* and *RLC* line approximated by sections of lumped elements.

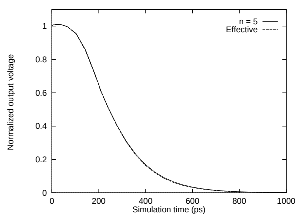


(a) (b)

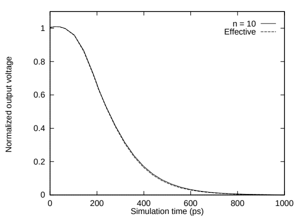
Fig. 6. An inductive interconnect line, (a) a distributed *RLC* line approximated by n sections of lumped elements, (b) the effective load impedance, R_{eff}, L_{eff}, and C_{eff}.



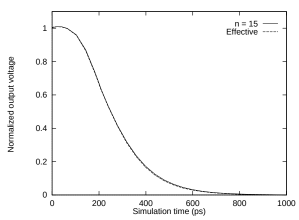
(a) SPICE simulation with $n = 3$ versus the effective load model



(b) SPICE simulation with $n = 5$ versus the effective load model

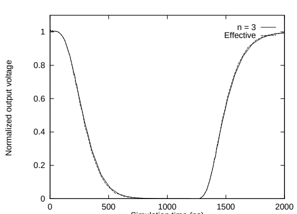


(c) SPICE simulation with $n = 10$ versus the effective load model

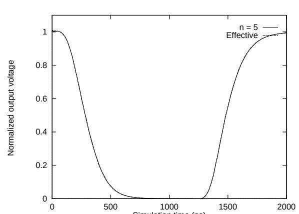


(d) SPICE simulation with $n = 15$ versus the effective load model

Fig. 5. Comparison of the effective load model with SPICE for a distributed *RC* line, $R = 500\,\Omega$ and $C = 0.2$ pF with $n = 3$, 5, 10, and 15, respectively.

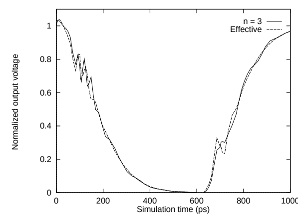


(a) SPICE simulation with $n = 3$ versus the effective load model

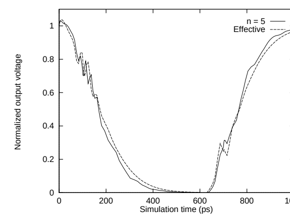


(b) SPICE simulation with $n = 5$ versus the effective load model

Fig. 7. Comparison of the effective load model with SPICE for a distributed *RLC* line with $R = 45.0\,\Omega$, $L = 1.0$ nH, and $C = 0.5$ pF with $n = 3$ and 5.



(a) SPICE simulation with $n = 3$ versus the effective load model



(b) SPICE simulation with $n = 5$ versus the effective load model

Fig. 8. Comparison of the effective load model with SPICE for a distributed *RLC* line with $R = 45.0\,\Omega$, $L = 2.0$ nH, and $C = 1.0$ pF with $n = 3$ and 5.

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