A Novel High-Speed Binary and Gray Incrementer/Decrementer for an Address Generation Unit

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Abstract

An Incrementer/Decrementer (INC/DEC) is a common building block in many digital systems like address generation unit which are used in microcontrollers and microprocessors. In this paper, novel architectures and designs for binary and gray INC/DECs are presented which are more efficient in terms of speed without compromising in power. The proposed architectures lay emphasis on the usage of hybrid logic that is, coupling of transmission gate with CMOS gates at appropriate stages for efficient design. Also, efficient utilization of the output and its complement, available in all existing implementations of gates, is done by using multiplexers in the proposed gray INC/DEC. For a 32-bit input, the proposed binary and gray INC/DEC achieve an improvement of 47%, 33% in delay and reduction of 38%, 28% in power-delay product respectively.

1. Introduction

The incrementer/decrementer (INC/DEC) is a digital module which can count up or down by one step and is a common building block in many digital systems like microprocessor, microcontroller and frequency divider [1,2]. It is also mainly used in a address generation unit where optimization of the circuit in terms of power is a important criterion. The current architectures of binary INC/DEC are mainly adder/subtractor-based, counter-based or carry look-ahead adder-based [3-4]. Recently, a MUX-based binary INC/DEC which is more efficient than the previous INC/DECs has been proposed in literature [5]. A gray INC/DEC (same as a gray code counter) consists of a binary INC/DEC coupled with gray to binary and binary to gray converters [6]. Since there is only one bit difference between adjacent numbers in a gray code sequence, only one bit transitions occur while counting with gray incrementer/decrementer. This limits the potential for transition errors as well as reduces the electrical noise generated unlike the binary counters.

This paper presents novel architectures and implementations for both binary and gray INC/DECs. The proposed implementations lay emphasis on the usage of hybrid logic, that is, coupling of transmission gates with CMOS gates at appropriate stages rather than using complete CMOS or transmission gate designs. This reduces high power dissipation due to cascading of transmission gates while giving lesser propagation delay. A novel gray to binary converter is also proposed which is coupled with the binary INC/DEC to obtain a new gray INC/DEC.

2. Binary Incrementer/Decrementers (INC/DECs)

2.1. Existing Architectures for Binary INC/DECs

There are various architectures for binary INC/DECs in literature. The carry propagation adder (CPA)-based INC/DEC is shown in Fig. 1(a). In this circuit, in order to implement increment and decrement, the operand B and carry input are tied to the mode selection signal (Inc/Dec) or its complement. With this configuration, there is a carry propagation effect from Cin to Cout through a series of full adders that makes the circuit slow.

The carry lookahead adder (CLA) based INC/DEC [7] is shown in Fig. 1(b). Although the speed can be improved to a certain extent, the circuit becomes too complex and has higher power dissipation when compared to CPA-based model.

A MUX-based binary INC/DEC, [5] shown in Fig. 1(c), is efficient in terms of both speed and hardware complexity when compared to adder-based INC/DECs. However, a series of (n-1) OR gates in its critical path hampers the speed of the circuit to a certain extent.

The critical path delay of this INC/DEC consists of (n-2) OR gates and a MUX.

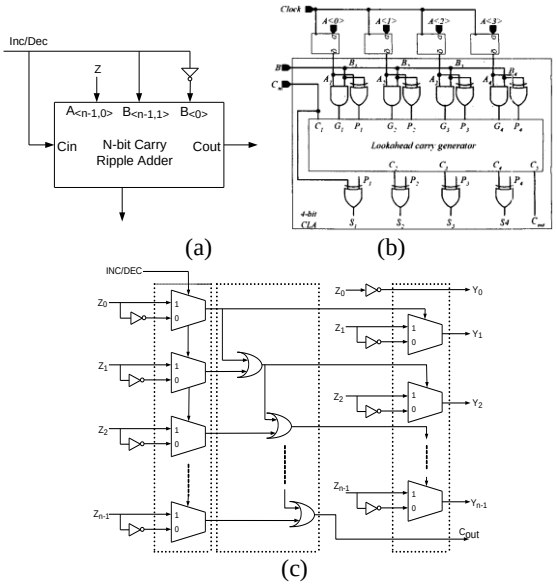


Fig. 1. Existing architectures of binary INC/DECs (a) CPA-based (b) CLA-based (c) MUX-based.

2.2. Proposed Architecture for MUX-based Binary INC/DECs

The proposed n-bit MUX-based INC/DEC is shown in Fig.2. It is composed of a data-in MUX array, data-out MUX array and a decision box (DB) used to find the least significant one bit (LSOB). The data-in MUX array and data-out MUX array are used to select between the input Z and its complement for decrement and increment respectively. Although 2n inverters are listed in Fig.2 for easy understanding, only n inverters are actually needed for implementation. To implement the function of increment and decrement by the same circuit, we use mode selection signal Inc/Dec. When the operand Z is to be incremented by 1, the signal Inc/Dec is set to 0 and if it is to be decremented by 1, Inc/Dec is set to 1.

The DB lies in the critical path of the INC/DEC and hence plays a crucial role in dictating the overall delay of the circuit. Therefore, optimizing the DB improves the overall performance of the INC/DEC. The output of data-in MUX array is $D_{n-1}D_{n-2}\ldots D_1D_0$. In the conventional MUX-based INC/DEC, the decision box consists of (n-1) OR gates connected in series which increases the delay of the circuit to a great extent. Hence, in the proposed DB, 8-bit look-ahead blocks are provided to reduce the delay of the circuit. Every 8-bit look-ahead block gives the OR of corresponding 8 input bits, hence to obtain the OR of the first 16 bits we need to OR the outputs of the 1st two look-ahead blocks. Similarly the carry at any stage can be obtained by OR-ing of the previous look-ahead blocks. The DB block implemented for a 32-bit input is shown in Fig 4.

The critical path delay of the proposed INC/DEC consists of ($^{\log}{}_2\, m + (n/m) - 2 + m$) gates where m is the m-bit look-ahead block. In this paper, we utilize a 8-bit look-head adder shown in Fig.3(a). Hence, the critical path delay of the proposed n-bit binary INC/DEC is ($n/m+9$) gates. The delay and complexity of existing and proposed circuits are analyzed in Table I.

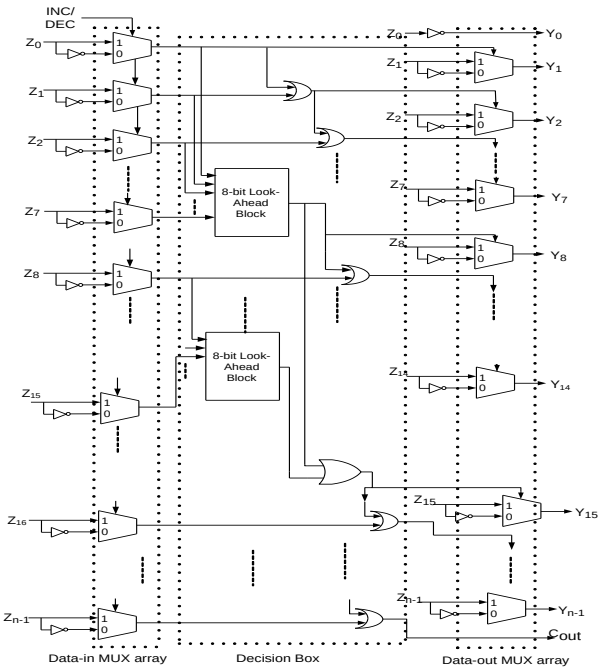


Fig 2. Proposed architecture of MUX-based binary INC/DEC.

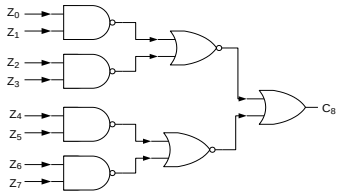


Fig 3. An 8-bit look-ahead block used in proposed INC/DEC

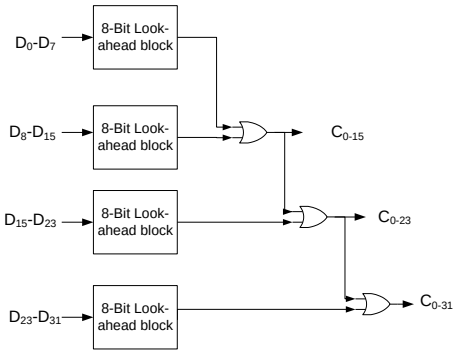


Fig 4. Proposed architecture of Decision Block (DB) implemented for a 32 bit input.

Also, in the DB of proposed circuit, hybrid logic (i.e. coupling of pass-transistor and CMOS logic) is used. According to this logic, a CMOS OR gate (shown in Fig 3c) is used after every two pass-transistor OR gates (shown in Fig. 3b). This implementation reduces power and delay parameters of the proposed circuit when compared to the conventional implementation which uses only CMOS gates.

Table 1. Analysis of Existing and Proposed architectures for Binary INC/DEC

INC/DEC	Complexity	Delay
CPA based	N*FA + Inv	$N*t_{FA} + t_{inv}$
MUX-based	(2N-1)MUX + N*Inv + (N -1)OR	$(N-1)t_{OR} + 2*t_{MUX}$
Proposed Hybrid INC/DEC	(2N-1)MUX + N*Inv + (N-1)OR + N/M(4*NAND+2*NOR+ OR)	$(Log_2M+ N/M + (M-2))* t_{OR} + 2*t_{MUX}$

3. MUX-based Gray INC/DECs

A gray INC/DEC (also called gray counter) consists of 3 parts: gray to binary converter, binary INC/DEC and binary to gray converter. Among the three, gray to binary converter largely determines the delay as it lies on the critical path. Hence, optimizing the gray to binary converter increases the overall efficiency of the gray INC/DEC.

The conventional implementation of an n-bit gray to binary converter is shown in Fig.5(a) which has a critical path delay of (n-1) XOR gates. The proposed implementation of the n-bit gray to binary converter is shown in Fig. 5(b) which has ((n-2) MUX + 1 XOR-XNOR) gates in the critical path.

In the existing implementations of all XOR gates, both output and its complement are available [8]. However, existing architectures do not use these outputs efficiently. In the proposed converter, both these outputs are efficiently utilized to improve the overall performance by replacing the XOR gates with MUXes. By using output and its complement at every stage, the total number of garbage outputs is reduced. Also, hybrid logic i.e. coupling of CMOS and transmission gate MUXes (shown in Fig. 6(a) and Fig. 6(b) respectively) is used which further optimizes the circuit.

The existing architecture for an n-bit gray INC/DEC [6] is shown in Fig. 7. The critical path of this INC/DEC consists of (n+2)-XOR gates.

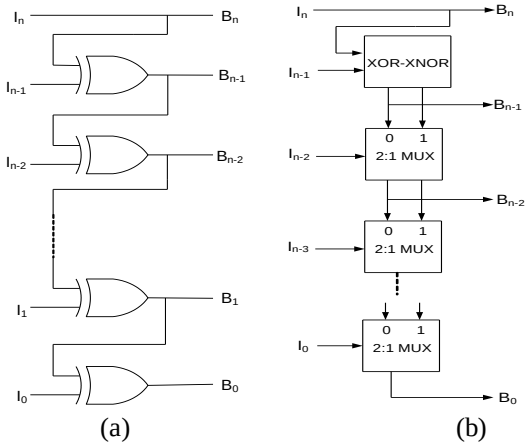


Fig. 5. Architectures of gray to binary converters (a) existing (b) proposed.

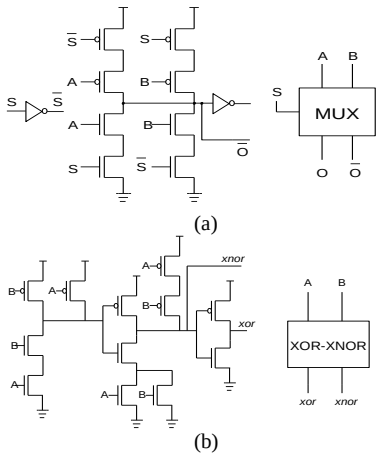


Fig 6. CMOS implementations of (a) MUX (b) XOR-XNOR.

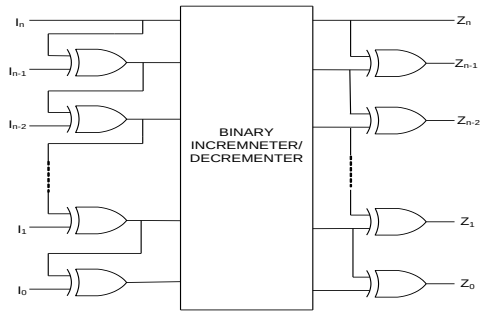


Fig 7. Existing architecture of gray INC/DEC.

The proposed architecture for MUX-based gray INC/DEC is shown in Fig.8. It consists of 3 parts: proposed gray to binary converter, MUX-based INC/DEC and binary to gray converter. The critical path of the gray INC/DEC is largely determined by the delay of the gray to binary converter and not on the INC/DEC. Hence the delay of the proposed circuit is (n-MUX + 1 XOR-XNOR) gates.

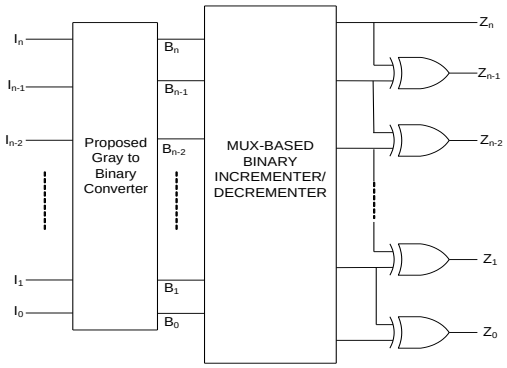
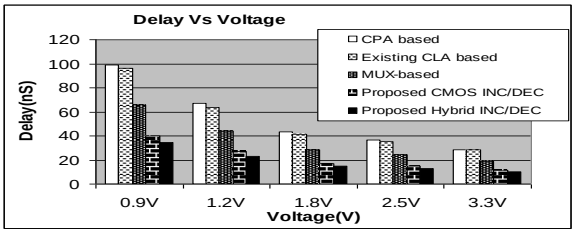


Fig 8. Proposed architecture of MUX-based gray INC/DEC.

4. Simulation Results and Discussion

All the simulations have been done using Cadence Tools 5.10.41. The calculation of power and delay are calculated using the Virtual Analog Simulation Tool already integrated into Cadence Tools. All the schematics are done using the CMOS 0.18-µm technology. The simulations are performed under various voltages ranging from 0.9V to 3.3V with a load capacitance of 10 fF. All inputs are fed at a frequency ranging from 100MHz-1GHz.



(a)

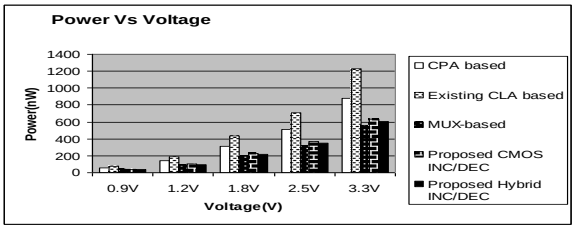
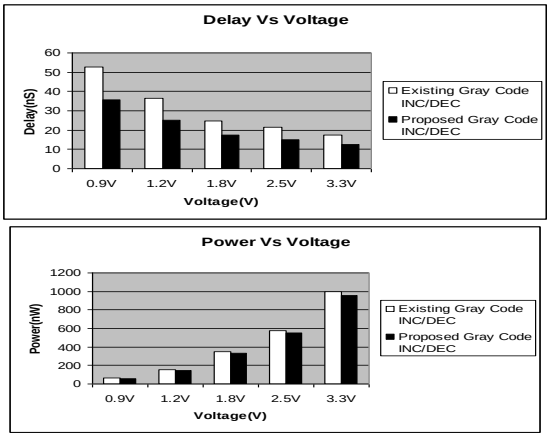


Fig 9. Comparisons between proposed and existing architecture for binary INC/DEC (a) Delay (b) Power

From the simulations, it has been observed that the proposed hybrid MUX-based INC/DEC has a 47% less delay and a 38% less power-delay product than the existing best circuit while having 5% more power consumption. The proposed gray to binary converter and gray INC/DEC have also been compared with the existing architectures. The proposed gray INC/DEC is 35% faster and has 28% lesser power-delay product when compared with the existing architectures.



(b)

Fig 9. Comparisons between proposed and existing architecture for Gray INC/DEC (a) Delay (b) Power

5. Conclusions

The existing and proposed architectures of binary and gray code INC/DECs are presented, simulated and compared. Simulations have been performed over a range of 0.9V to 3.3V for circuits designed for 32-bit operation. The proposed binary INC/DEC has a 47% less delay and a 38% less power-delay product when compared to the existing MUX-based design. Also, the proposed gray to binary converter is 35% faster than the traditional design while the proposed gray INC/DEC achieves a delay efficiency of 33% and a reduction of 28% in power-delay product.

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6. References

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