A effective New Learning Approach towards Digital Electronics

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Abstract- Industry scenario now has created a high demand for system designers with the understanding and experience in using programmable logic such as CPLD's and FPGA's. Many universities offer this type of education in advanced digital courses. This paper describes our experience in integrating hardware description language and PLD based on Altera into the basic course of digital design. First and foremost the student's reaction towards the course was positive as the course seems to be a mixture of VHDL and CPLD as they have a prior knowledge and hands on experience on bread boarding. For this purpose , a laboratory with development boards are built and a series of laboratory exercises are developed using the CPLD kits under Altera Quartus II web Edition environment.

Keywords – Digital Design, programmable logic, VHDL, CPLD, Quartus II Web Edition

I. INTRODUCTION

With rapid development of programmable logic devices, it has become mandatory to teach these concepts of reconfigurable hardware at the undergraduate level. Though the effectiveness has improved the digital design teaching by using programmable logic and several universities are on the path of PLD technology in the basic course of digital design which has been a challenge due to scaling up of the laboratory facilities at undergraduate level [1]. Hence, in most of the institutes students are left with simulation using CAD/development tools without having any hands on experience with such devices.

The Wadhwani Electronics Lab team [WEL], provides a low cost solution to teach concepts of digital design using a CPLD with minimal requirements on the student's part. They provided us with 10 development kits free of cost so that it will help students to better understand the concepts of logic design and have hands on experience with reconfigurable logic design. This boosts their confidence level to use state of art technology.

The digital design depends on such individual of the engineering groups who have sound knowledge of the problem, from the top to bottom in the hierarical order , with the expertise in one or two areas[2].

It is observed and experienced ([3]-[4]) that use of discrete elements in lab sessions is ineffiecient and lead to disinterset because of the time spent in building and debugging simple circuits. Appropriate hardware to replace these discrete basic digital components has been a concern since the inception of programmable logic([5]-[6]). This paper elaboartes our experience in integrating VHDL and programmable logic device (CPLD) based on Altera tools. The paper is arranged as follows: Section II gives the features of Digital Design course Section III Overview of Programmable Logic Devices. Section III Hardware Desciption Language. Section IV gives the Teaching the Software of digital design . Section V Lab Session and mini project. Section VI Experience Section VIII Acknowlegment and lastly the conclusion.

II. DIGITAL DESIGN COURSE

For engineering curriculum, under the entry level of electrical, electronics and computer have the first digital design course which is extended over 12 weeks with 48 hours of lectures and 24 hours of laboratory sessions. The topics included in this course are Boolean algebra and logic gates, Reduction Methods, Combinational and Sequential Circuits and introduction to Finite State Machines. The choice of textbooks is done which have integration of theory, software and its applications using Programmable logic Devices [(7)-(11)]. The books which we chose were Wakerley [7], Morris Mano [8]. The main aim of this course are (1) to teach the basic concept of digital design and (2) to illustrate as how the digital circuits are designed today using CAD tools and mapping the designs to programmable logic devices with the help of CPLD. The lab is based on 14 experiments using bread boarding and discrete components during Semester III. Throughout the course basic concepts are cleared by way of examples that involve simple circuit to complex design. Introduction to hardware description Language i.e. VHDL is covered in Simulation Software Workshop which is in Semester IV that includes 4 lecture hours and 8 lab hours allocated for

VHDL. They perform 6 experiments which covers all the modelling concepts of VHDL and a mini project for the same where the interfacing of hardware is done with CPLD kit and display the output in real time. The study in lab session is limited to CPLD as the infrastructure of lab is limited to enough number of development kits. The motivation and support was given by Wadhwani Electronics Lab (WEL), IIT Bombay by donating 10 development kits to our institute on attending one of their Short-term training Program. This fact reinforced our decision to use these kits for doing experiments and mini projects.

III. OVERVIEW OF PROGRAMMBALE LOGIC DEVICE

Programmable Logic Devices started in early 70's [12] that can be configured by the user to perform a large variety of logic functions. The internal schematic arrangement includes two types of devices, the circuits or building blocks and interconnections can be configured by the user to perform the required function or set of functions. The configurations can be modified or altered any number of times by user, by reprogramming the device. The main goal behind creating such a chip is reconfiguration in sum of products form where AND gates form products and OR gates form sum. The IC created with the above mentioned architecture is called PAL [13]. The various types of PLD are different from one another in terms of architecture, logic capacity and programmability. The types are:

1. PROM – a fixed array of AND gate and a programmable array of OR gates for a particular logic function.
2. PAL – a programmable array of AND gate feeding a fixed array of OR gates.
3. PLA – a programmable array of AND gates feeding a programmable array of OR gates.

Out of these 3 the efficient one is PLA which is feasible to construct small sequential systems. The above mentioned devices are limited to small sized resources called as Simple Programmable Logic Devices (SPLD's)

The Complex Programmable Logic Devices (CPLD) are formed of several PAL devices limited to each other by programmable interconnections.[14].The architecture of CPLD device is used to create large combinational and sequential systems.. The programming technology used in CPLD is EEPROM/Flash. The main vendors for CPLD/FPGA are Xilinx and Altera.

IV. HARDWARE DESCRIPTION LANGUAGE

VHDL stands for Very High Speed Integrated Circuit Hardware Description Language. VHDL was the first HDL to be standardised by IEEE. VHDL is commonly used as a design entry language for programmable logic devices in electronic design automation of digital circuits. It is a general purpose hardware description language that is specifically designed to describe the function and organisation of digital hardware system, circuit boards and components at many levels of abstraction ranging from simple gates to complete electronics systems. VHDL model is textual description of hardware design or a piece of design that when simulated duplicates the design behaviour of the required system to be modelled or simulated before synthesis, tools translates the design into real hardware i.e. gates and wires. VHDL allows the description of concurrent systems (many parts, each with its own sub-behaviour working at the same time) or sequential systems (working in a sequence).

Electronic Design Automation (EDA) tools are used for VHDL/Verilog synthesis and simulation: Quartus II Web Edition from Altera (synthesis), ISE Foundation from Xilinx, FPGA Advantage, Leonardo Spectrum and Modelsim (Simulation) from mentor Graphics, Design Complier, RTL Synthesis from Synopsys, Synplify Pro from Synplicity and Encounter RTL from Cadence.

VHDL code can be written using either structural or behavioural representations. Once written, VHDL code can

Then be run through sophisticated EDA tools which will generate actual low level gates. Later these designs can be transferred to programmable devices where they can be checked for proper working.

The basic VHDL design flow in top-down digital design system is shown in fig.1 [15]. The first step in synthesis is compilation .It is the conversion of VHDL source code to a net list. The second step is optimisation which applied on gate level for speed and area. The design is then simulated and finally place and route to give the physical layout for a programmable device (CPLD/FPGA).

V.TEACHING SOFTWARE OF DIGITAL DESIGN

Knowing the programming language, students have an affinity in simulating the code on the software. They have the satisfaction in having achieved the program work in real time applications instead of clipping and cutting wires. Overall the performance is high, cost and area occupied is less for an application worked on CPLD kit. Most important, we can reuse the CPLD kit again and again with different applications .These factors help to improve the size and challenge of designs that students can work on. Always students have a question. How the data is downloaded on Programmable chip? Answer is: It already has the gates but only interconnections are to be done with one gate to the other. So different programmable technologies are used each of the PLD's. The technology used for CPLD is EEPROM /Flash and for FPGA it is the SRAM.

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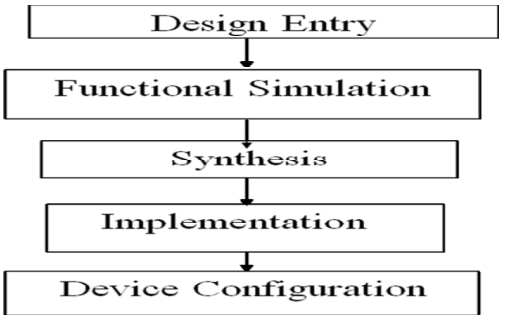

Figure 1. VHDL Design Flow

VI. ALTERA MAX3000A BOARD

The development boards are designed and developed by Wadhwani Electronics lab, IIT Bombay [16]. It is also called as Helium 1.1 board as depicted in figure 2.The main feature of the board are as follows:

- Based on Altera architecture
- Device used on board: EPM3064A(1250 usable gates)
- Powered and programmed through USB.
- 8 switches as inputs and 8 outputs as LED's.
- 8 user configurable I/O pins for interfacing to external circuitry.
- On-board clock of 1Hz.

The software used is Quartus II Web Edition [17].

There is a provision of giving an external clock for particular application. The development kit is connected through PC via JTAG cable. So we need to install the Urjtag file in order to download the bit pattern into the kit. In order to have the compatibility with PC and the kit some drivers are to be installed [18] otherwise the bit pattern will not get downloaded properly. The procedure for installing the driver is given in WEL website.

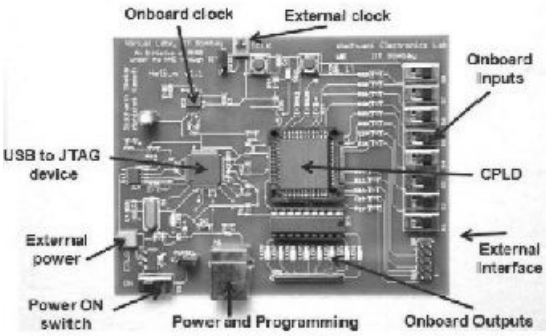

Figure 2.Altera MAX 3000A Development Board

VII. LABORATORY SESSIONS AND MINI PROJECT

The lab sessions are the integral part of the course. The main aim of the labs is:

- To help student understand and co-relate the theory of HDL.
- To give the student a practical flavour with the process of design and implementation of digital circuits.
- To give hands-on experience with EDA tools and development kit for digital hardware development.

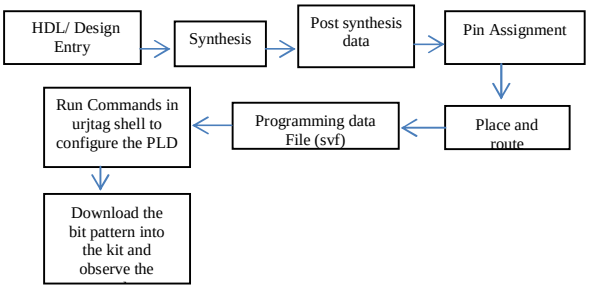

Figure 3. Pictorial representation of generating a bit pattern

The logic circuits that students build using discrete components were limited to LSI chips that contain less logic gates. As the complexity increases the clipping and cutting wires would increase which would lead to frustration in getting in result of any specific application. Students really enjoyed working on PLD's as they could see the output in real time. The simulation projects were helpful as the students could understand and co-relate with the theory subject...

The course laboratory is formed of 14 experiments with discrete components which are covered in Digital Design. The list of experiments includes: Study of different Logic gates, Introduction to Arithmetic circuits, Design aspects of Combinational and Sequential circuits, Study of Finite State Machines (Mealy and Moore), Sequence Detectors and Generators. Introduction to Altera Quartus II environment.

This CAD tool does not have in built simulator as in Xilinx so that students can check the O/P graphically before synthesizing or downloading the bit pattern in the kit. The simulator used is Qsim called as Altera U.P simulator [19].Later the UrJTAG shell is opened and run following commands sequentially:

cable ft2232 (press enter)
detect
svf D:/counter.svf

The first line state to connect the driver, if it is correct gives the statement connected to libftd2xx driver. Detect the device, if detected gives the details of the altera kit. Next give the path of bit pattern which was created by the software. Now we are in stage to observe the results. This is well explained pictorially as depicted in figure 3. The main aim of using altera software is again all the software used is freeware

Following is the outline of 6 experiments we used while offering the course Software Simulation Workshop in semester IV.

Lab1: Introduce the students with Quartus II 11.0 web edition which is a free ware in altera site .They used the development kit and configured a simple ex-or gate using switches and LED's for I/P and O/P as shown in figure 4. This lab also helps the students to get practise with each component of the kit by testing and debugging if in case of any problem.

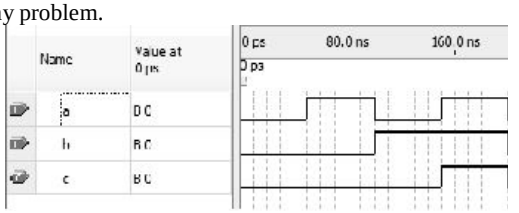

Figure 4. Waveform of ex-or gate

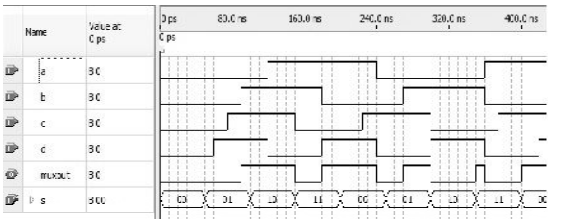

Figure 5. Waveform of MUX

Lab2: The students were exposed to the field of combinational circuits wherein they could co-relate theory statements in practicals by performing experiments on half adder, Full adder and Multiplexer. The output waveforms are as shown in figure 5.

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Lab 3: The students have done the programs on Sequential circuits i.e. D flip Flop, Counter and shift register wherein the get know the basic operation of each as shown in waveform figure 6.
Lab4: At this stage they are almost familiar with VHDL command and programming language. The lab is introduced to know the basic concepts and steps for Finite state machines. The waveform for traffic light controller is shown in figure 7.

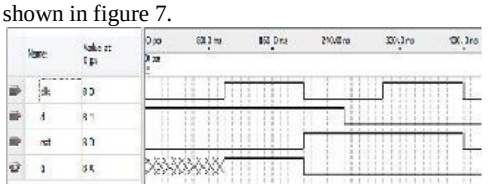

Figure 6. Waveform of D Flip-Flop

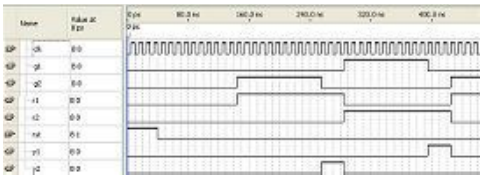

Figure 7. Waveform of Traffic light controller

Lab5: The students at this stage are familiar with the kit and software. They now do the literature survey for the mini project where the duration is 4 weeks. They should be now in the state of interfacing the CPLD kit with real time hardware.

VII. EXPERIENCE

The main goal of this project to students was to get hands on experience with state of art kit in basic course of Digital Design using VHDL and CPLD programmable logic for mapping designs. They had a satisfaction of preparing daughter boards for the CPLD kit so that they could display the result in real time. The students had to struggle a lot initially in installing the software in the laptops or PC. Later they overcome all the difficulties and were successful in doing the mini projects.
The biggest challenge was to cover the material and teach the students with the concepts of VHDL with 6 weeks. Students have found the VHDL topic interesting as they had exposure to virtual lab site if in case of any problems.

VIII. FUTURE WORK

Presently the students have got an exposure with only the CPLD kit. We are planning to have the FPGA kits for use in more advanced Digital Design courses. We will plan to develop new teaching material for the new set of lab sequence so that students get creative ideas in developing a prototype daughter boards.

VIII. ACKNOWLEDGMENT

Sincere thanks to WEL Virtual lab, IIT Bombay for donating 10 development kits to our college. Moreover their support and help provided, whenever we faced problem with kit and software. The software required are all open source, Quartus II 11.0 Web Edition, Altera U.P Monitor Program (Simulator), and Urjtag from Altera website [19]. With zero investment we could provide the knowledge of programmable logic which is in practise at some extent in present industry scenario.

IX. CONCLUSION

Teaching digital logic design with VHDL and synthesizing using CPLD presents an integral approach to digital logic principles and implementation to make them think more within the short duration. This was possible by introducing digital design concepts, VHDL coding, simulation, synthesis and reconfiguring again and again. Moreover, the students accepted the challenge except the few. This was started for the first time and worked out to be positive and aim for higher applications in the future. It is a mixture of hardware and software. We could conclude our experience, describing the use of VHDL, synthesize on CPLD and could present it with the real time hardware was a success for the entry level engineering students in electronics and telecom stream.

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