A Multimetal Surface Micromachining Process for Tunable RF MEMS Passives

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***Abstract*—This paper reports on a microfabrication technology for implementing high-performance passive components suitable for advanced RF front-ends. This technology offers three metal layers with different thicknesses, one dielectric, and two sacrificial layers, enabling the fabrication of continuously tuned capacitors, capacitive and ohmic switches, as well as high-Q inductors all on a single chip. To demonstrate the versatility of this technology, several passive components are fabricated on a Borosilicate glass substrate ($\varepsilon_r = 4.6$). A high-Q tunable capacitor is fabricated exhibiting an electrostatic tuning range of more than 6 : 1. The temperature variation of capacitance from 223 to 333 K is less than 9%, and the tuning speed is better than 80 μs. To achieve a higher zero-bias capacitance, a tunable capacitor bank is also implemented, which can be tuned from 2.2 pF to 6.1 pF. In addition, a coupled inductor pair with self-inductances of 15 and 21 nH is implemented showing Qs exceeding 40 at 800 MHz. Measurements are compared with high frequency structure simulator (HFSS) electromagnetic simulations, showing good agreement. The technology reported is post-CMOS compatible and low cost. [2011-0331]**

***Index Terms*—High quality factor, RF MEMS, surface micromachining, tunable passives, ultra high frequency.**

I. Introduction

THE POTENTIAL of RF microelectromechanical systems (MEMS) technology for implementing front-end components and modules with strict RF performance is already proven. Using micromachining technologies, individual RF components including antenna arrays [1], [2], matching network [3], [4], phase shifters [5], [6], single-input multiple-output switches [7], [8], and band-select filters [9]–[12] are demonstrated. However, as each of the aforementioned RF modules requires diverse types of passives and as such poses different constraints on the fabrication technology, it is fabricated on a separate substrate and integrated with other parts in a system-in-package [13] or assembled on a printed circuit board [14], [15]. Compared with the system-on-chip, these approaches not only demand a larger area but are also more costly. In addition, the loss and parasitics of metal routings and bondwires required for chip-to-chip connections would be major concerns, particularly at higher frequencies where they could significantly degrade the RF performance [16]. Therefore, a technology is needed that offers all possible RF passives, the building blocks of RF systems, on a single substrate at low cost. To this end, several issues must be addressed. First, such a technology must offer multiple metal layers to allow implementation of different passives, tunable or fixed, rigid, or compliant. Thick electroplated metals will be necessary for high-Q inductors, whereas thinner metals with low intrinsic stress will be needed for the released membrane of tunable capacitors and switches. Another consideration would be the selection of sacrificial layers and the release process for tunable components including air-suspended membranes. Last, a number of interlayer dielectrics with different properties might be needed for large-value metal-insulator-metal (MIM) capacitors or small-capacitance under-pass routings.

Philips Inc. has shown a fabrication technology for tunable capacitors using silicon dioxide and silicon nitride as the sacrificial layers and nature oxide of aluminum as the dielectric [17]. However, the breakdown voltage of the thin intrinsic aluminum oxide (Al_2O_3) is not sufficiently high, and thus the capacitors cannot sustain high RF powers. Researchers at Georgia Institute of Technology have shown a two metal micromachining process suitable for obtaining laterally tunable capacitors and high-Q inductors [10], [11]. While high-performance components were shown using this technology, the tuning bias voltage of the capacitors was high, as the same electroplated layer defined the tunable capacitors and thick inductors. A different process developed by University of Michigan for fabrication of switches utilized poly-methylmethacrylate (PMMA) as the sacrificial layer [18], but lacked thick metal processing, which is essential for co-integration of high-Q inductors.

In this paper, a surface micromachining process is reported that offers simultaneous fabrication of switches, tunable capacitors, fixed MIM capacitors, high-Q inductors, and coupled inductors. The performance and characterization results of several passives fabricated using this technology are demonstrated and compared with simulations. The proposed technology can be used to fabricate reconfigurable RF modules needed for multistandard radios [19].

II. Fabrication Process

The fabrication process flow is schematically shown in Fig. 1. First, a metal layer consisting of $300\text{A}^\circ\text{Cr}/5000\text{A}^\circ\text{Au}/300\text{A}^\circ\text{Cr}$ is deposited and patterned on borosilicate glass substrate using the lift-off process. This layer is used for bias

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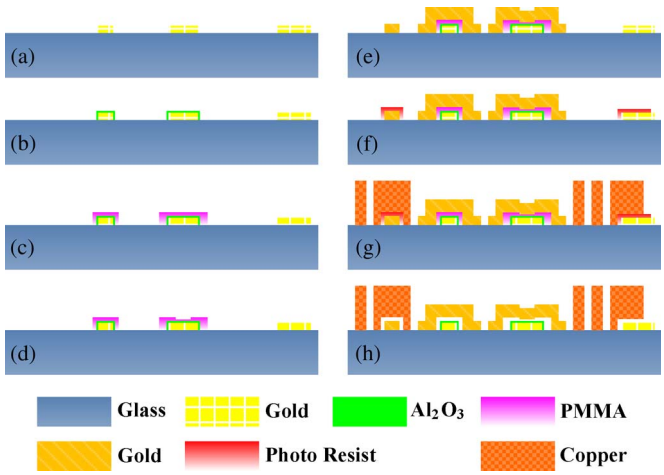

Fig. 1. Fabrication process flow. (a) Au lift-off. (b) Al_2O_3 deposition. (c) PMMA patterning. (d) PMMA thinning. (e) Au electroplating. (f) S1813 lithography. (g) Cu electroplating. (h) Release in acetone followed by CPD.

lines and bottom electrodes of tunable capacitors. Borosilicate glass is chosen because of its low RF loss. Though, the same fabrication process can be applied to other substrates, such as high resistivity and passivated CMOS-grade silicon. Next, a 1000A° thick Al_2O_3 layer is deposited using an atomic layer deposition (ALD) tool with water vapor at 250 °C. ALD Al_2O_3 is chosen as the inter-layer dielectric because of its high dielectric constant (ε_r) of close to 10 and uniform side-wall coverage. The Al_2O_3 is patterned using Transene aluminum etchant Type A at 50 °C.

Next, a sacrificial layer is deposited and patterned. For the selection of the sacrificial layer, the following factors should be considered: the sacrificial layer should not be deformed or attacked during the subsequent processing steps, and its etchant during the release step should have good selectivity against other layers. Some commonly used sacrificial layers are polymers [20], [21], metals [22], [23], silicon dioxide [24], and amorphous silicon [25]. Amorphous silicon can be deposited with various methods such as plasma enhanced chemical vapor deposition (PECVD) or sputtering, and it is not easily attacked or deformed during the post processing steps [26]. The main problem with PECVD amorphous silicon is that it is hard to remove with either wet etchants such as KOH or dry etchants such as xenon difluoride (XeF_2) [27]. Sputtered amorphous silicon is easier to remove with XeF_2. However, the removal of sputtered amorphous silicon in XeF_2 is nonuniform; thereby, long etch time is needed to release the device. The long XeF_2 release step results in increased stress in other metal layers on the wafer (in our case when the release time is increased beyond 15 min). Fig. 2 shows the stress distribution of a gold electroplated silicon wafer when 30 cycles (15 min) and 90 cycles (45 min) of XeF_2 is applied, respectively. Each XeF_2 cycle is composed of 30 s of gas flow step. The stress in the gold layer clearly increases upon long exposure to XeF_2. Although the release condition is subjective to the deposition parameters and properties of the amorphous silicon layer as well as the XeF_2 etch process, and one might characterize a recipe for better release of amorphous silicon, the increased stress in metal layers is hard to avoid. The initial value and the tuning characteristic of capacitive devices are highly dependent on the stress in the released metal film, and therefore, amorphous silicon was not chosen as the sacrificial layer in this process. Instead, uncured PMMA is used as the sacrificial layer. The main advantage of using uncured PMMA is that it can be easily removed in a relatively short time and without damaging other layers on the substrates. Alternatively, a metal could be used as the sacrificial layer. However, for a process consisting of three metal layers and several metal adhesions layers, it is unlikely to find a metal that its etchant is selective to all other metals on the wafer during release.

The PMMA patterning is done in three steps; first, PMMA is removed from unwanted areas. Next, it is thinned down in select areas in two steps to define two different gaps for the continuously tuned capacitors and capacitive switches. 500A° of TiW is used as a hard mask during the PMMA patterning process with O_2 plasma. TiW is subsequently removed in a hydrogen peroxide (H_2O_2) solution.

After sacrificial layer deposition and patterning, 4 μm of gold layer is electroplated to form the top membrane of capacitors and the inductor interconnects. The gold layer is electroplated using the BDT-20 solution at 50 °C and with current density of 2 mA/cm^2, an optimal processing condition for obtaining a uniform and low-stress film. The residual stress and stress gradient of the electroplated gold layer are extracted to be 40 MPa and 2 MPa/μm, respectively, using a microstrain gauge [28] and a cantilever included on the wafer.

After removal of the mold and seed layer, the inductors and thick routing layers are fabricated. Shipley 1813 photoresist is utilized as a sacrificial layer for creating air bridges between the electroplated gold (interconnection) layer and the thick electroplated copper layer (inductor and ground lines). A 35 μm copper layer is electroplated using a 40 μm thick AZ9260 photoresist mold. Finally, the sacrificial layers are removed using PRS2000 followed by acetone and the wafer is dried using critical point drier (CPD) to prevent stiction. Another possible release method is using O_2 plasma. However, long-time O_2 plasma can increase the substrate temperature and cause additional stress in the released membrane [29].

III. Design and Measurement Results

Tunable capacitors, capacitor banks, and inductors are designed and fabricated using the fabrication process outlined in Fig. 1. Unless otherwise stated, the fabricated passive components are measured using an N5241A Agilent PNA-X network analyzer and Cascade Microtech GSG Z-probes. Calibration is performed using the short-open-load-thru method.

A. Tunable Capacitor

For the design of tunable capacitors, the specifications listed in Table I were targeted. A capacitor meeting these specifications allows the implementation of high-performance tunable filters such as the one presented in [19]. In this paper, the capacitors are electrostatically tuned, temperature stable, and have separate RF and dc electrodes for better power handling as well as more convenient tuning. The layout of the tunable capacitor is schematically shown in Fig. 3 (left). For continuously

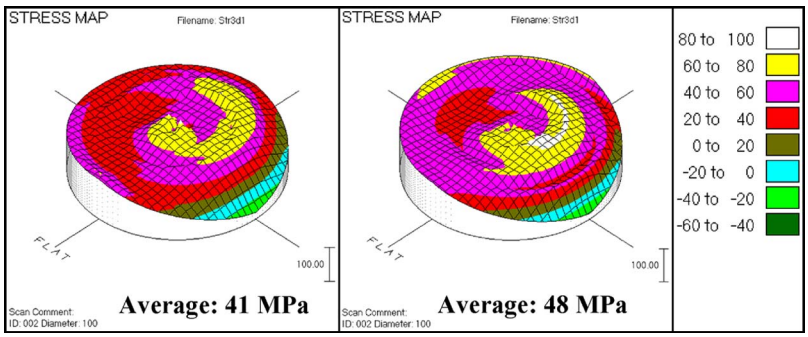

Fig. 2. Residual stress distribution of a 2 μm thick gold layer electroplated on a silicon wafer after 30 cycles (left) and after 90 cycles of XeF_2 etch (right).

TABLE I
TARGET SPECIFICATIONS OF THE TUNABLE CAPACITOR

Specifications	Target
Configuration	One port
Tuning-type	Continuous / Switched
Initial capacitance (C_{IN})	200 fF
Tuning range (C_{FN}/C_{IN})	> 5
Quality factor (Q)	> 100 @ 1GHz
Operation range	up to 2 GHz
Mechanical resonant frequency (f_M)	> 20 kHz
Maximum tuning bias (V_T)	< 40 V
Temperature variation (C_{IN}, C_{FN}, V_T)	< 10 % (223 K ~ 333 K)
Dimensions	$< 400 \times 400$ μm^2

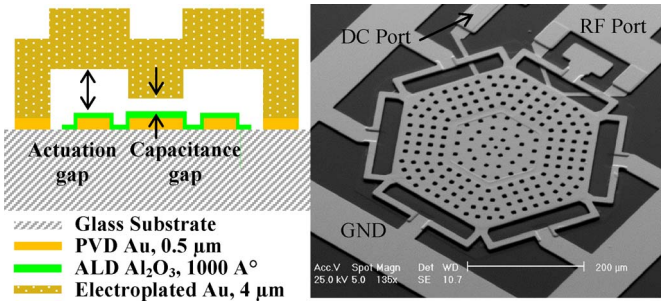

Fig. 3. Layout of the tunable capacitor. Schematic diagram showing cross-section view (left) and top-down SEM view (right).

tuned capacitors (i.e., varactors), a dual-gap configuration is adopted (with an actuation to sense gap of 4 : 1) to overcome the pull-in limitation and achieve better linearity [26]. In switched capacitors, on the other hand, a 4 : 3 dual-gap ratio is used for better fabrication yield. The size of the entire membrane is decided by the center area for initial capacitance of 200 fF and the actuation area for maximum tuning bias of 40 V. The size of the center RF node is 145 μm $\times$ 145 μm, while the overall size of the top membrane is 310 μm $\times$ 310 μm. The actuation air gap is designed to be 2 μm, considering the membrane size and the fabrication yield. Fig. 3 (right) shows a scanning electron microscope (SEM) view of a fabricated tunable capacitor.

For the mechanical design of the capacitor, ANSYS finite-element simulation software [30] is used, considering the residual stress (40 MPa) and stress gradient (2 MPa/μm) of gold extracted from measurements. Other material properties of the gold layer is set as 45 GPa (Young's modulus), 19.30 g/cm^3

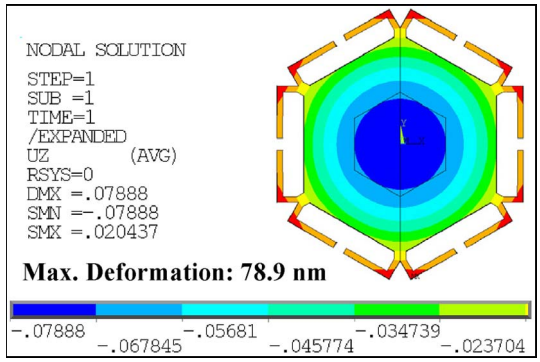

Fig. 4. Deformation of the hexagonal membrane upon 40 MPa of residual stress and 2 MPa/μm of stress gradient at room temperature (300 K).

(mass density), and 14.7 ppm/°C (thermal expansion coefficient), according to the published values for electroplated gold [31]. Two major specifications considered here are the mechanical resonant frequency (f_M) and the temperature stability of capacitance. For the springs, the geometrically compensated spring and anchoring design introduced in [32] was adopted. Prior work using this compensation technique utilized a square-shape membrane [32]. In this paper,a hexagon-shape membrane is selected since it offers a higher mechanical resonant frequency for a temperature stable design. Fig. 4 shows the room temperature deformation of the top membrane for a hexagonal design, having a resonant frequency of 23 kHz, when 40 MPa of residual stress and 2 MPa/μm of stress gradient are considered for the gold layer. This design shows a maximum deformation of less than 80 nm, which is relatively small compared to the capacitance air gap of 0.5 μm.

For the design shown in Fig. 4, the deformation of the gold membrane under different stress conditions is further analyzed. First, the deformation of the membrane with 50, 100, or 200 MPa of residual stress and no residual stress gradient is simulated over the temperature range of 198 K to 373 K. As shown in Fig. 5(a), the deformation is not affected by the residual stress and is less than 10 nm. Therefore, this hexagonal membrane design is very robust against residual stress and temperature variations. The second simulation is under 40 MPa of residual stress and different residual stress gradient of 2, 5, or 10 MPa/μm, respectively [Fig. 5(b)]. The deformation of the membrane is highly affected by the stress gradient. Thus, the stress gradient in the electroplated gold should be carefully controlled. Finally, the membrane deformation is simulated under the same stress conditions over the temperature range of

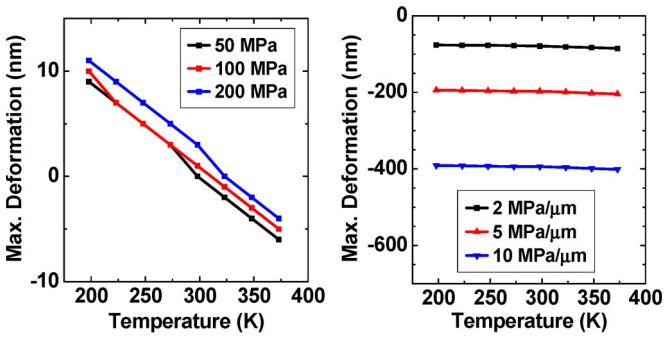

Fig. 5. Maximum deformation of the hexagonal membrane when temperature is varied from 198 K to 373 K: (a) under 50, 100, or 200 MPa of residual stress and (b) under 40 MPa of residual stress and 2, 5, or 10 MPa/μm of stress gradient.

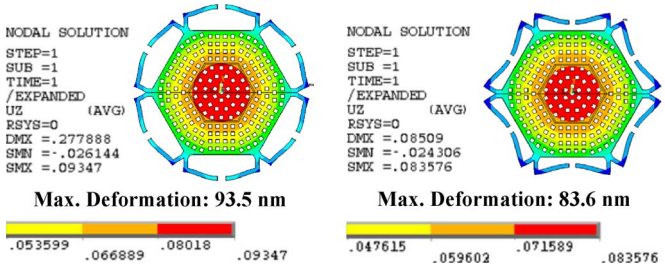

Fig. 6. Deformation of the top membrane upon 40 MPa of residual stress and 2 MPa/μm of stress gradient at 223 K (left) and 333 K (right).

223 K to 333 K, as shown in Fig. 6. The temperature-induced change in the deformation of the central part, which defines the capacitive gap, is limited to 10 nm. The resulting change in the initial capacitance is thus less than 2.5%, proving that this design meets the target specification in terms of temperature stability.

To simulate the electrical properties, such as C_{IN}, C_{FN}, and Q, the high frequency structure simulator (HFSS) 3-D electromagnetic tool [33] is utilized. The conductivity of copper and gold is taken as 5.5×10^7 S/m and 4.0×10^7 S/m in simulations, respectively. The properties of the substrate ($\varepsilon_{\mathrm{r}} = 4.6$ and $\tan\delta = 0.001$) are taken into account for accurate simulation of quality factor and self-resonant frequency (SRF). Accurate simulation of C_{FN} during touch-down of the top membrane is difficult since it is dependent on various factors such as deformation of the top membrane, electrical properties and surface conditions of the dielectric layer, and the electrodes. To reflect these nonidealities, C_{FN} is simulated using a reduced dielectric constant for the aluminum oxide dielectric layer, less than quarter of the bulk value. The dielectric loss ($\tan\delta$) of aluminum oxide is assumed to be 0.005.

The simulated capacitance at the initial and final tuned states is shown in Fig. 7. The measured results of the tunable capacitors (varactors) are also shown on the same figure for easy comparison. The fabricated varactor is continuously tuned from 220 fF to 1.33 pF. The tuning range is slightly smaller than the simulated range of 300 fF to 1.7 pF. The discrepancy between the measured and simulated initial capacitance values can be due to the larger warping of the top membrane, which itself might be the result of a larger stress gradient in the electroplated gold layer. From the measured initial capacitance, around 0.2 μm of membrane warping is expected, which corresponds

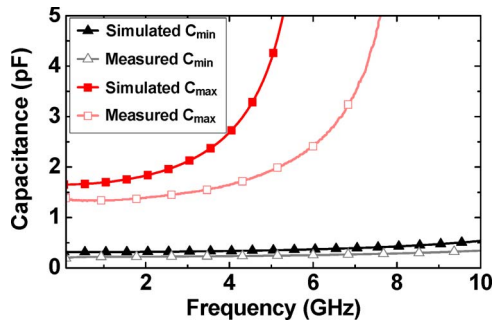

Fig. 7. Initial capacitance and maximum capacitance extracted from the HFSS simulation and measurement result, respectively.

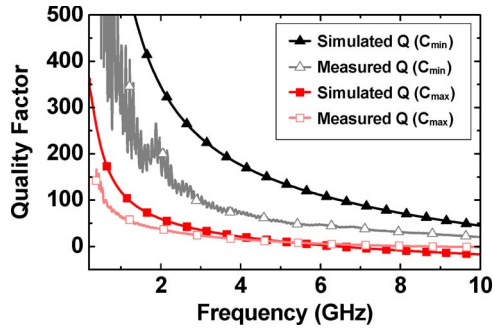

Fig. 8. Q at initial and final states extracted from the HFSS simulation and measurement result, respectively.

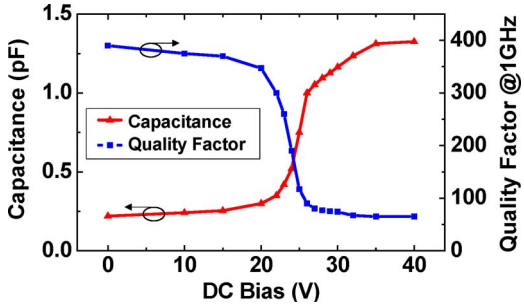

Fig. 9. Measured tuning characteristics of the continuously tuned capacitor. At Stage 1, the air gap closes uniformly. At Stage 2 (after touch-down at 26 V), the membrane conforms to the substrate.

to a residual stress gradient of 4 MPa/μm. The smaller touch-down capacitance value is also due to the warping of the top membrane as well as the rough surface of the electrode.

Fig. 8 shows simulated and measured Qs at the initial and final tuned states. The measured Q is higher than 65 at 1 GHz at all tuned states. The measured SRF is more than 13.5 GHz at the initial state and higher than 8.7 GHz at the final tuned state, which is similar to the simulated value. The measured Q is however lower than simulated value at low frequencies because of the lower conductivity of metals and higher dielectric loss of aluminum oxide compared to the values considered in the HFSS simulations. It is worth mentioning that accurate measurement of Qs in excess of 100 requires more complex measurement methods. One such method is to extract the Q from the bandwidth of a resonator implemented using the capacitor under test and an inductor with a known quality factor [34].

The tuning characteristics of the varactor and switched capacitor are compared in Figs. 9 and 10. Since both capacitors

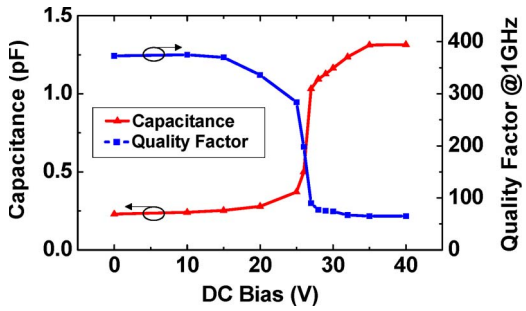

Fig. 10. Measured tuning characteristics of the switched capacitor. At Stage 1, the air gap closes uniformly. At Stage 2 (after touch-down at 27 V), the membrane conforms to the substrate.

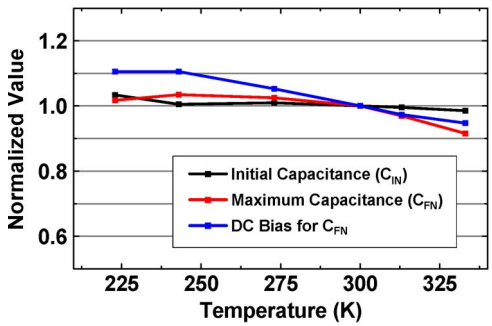

Fig. 11. Measured initial and final capacitance values as well as the maximum dc bias are stable within 5%, 7%, and 9% of their room temperature values.

have the same springs and membrane design and only different capacitance gap size, the final capacitance value and Q is very similar. However, the$C$–V trend shows a clear difference; the largest transition slope of the varactor is 0.25 pF/V while that of the switched capacitor is more than 0.5 pF/V. This is due to the larger actuation to sense gap ratio for the continuously tuned capacitor [17]. For both designs, the largest capacitance value is not achieved at the pull-in bias, but is reached at larger bias voltages close to 35 V at which the membrane is flattened with a larger actuation force. The warping in the membrane can be reduced with a more optimized gold electroplating process. The structural compensation can also be improved to allow better tolerance on the stress gradient.

Fig. 11 shows variation of initial capacitance, maximum capacitance, and tuning bias over temperature range of 223 K to 333 K. Microtech KV-230 cryogenic station and GGB RF probes are used for these measurements. Calibration is redone at each temperature to remove the effect of the probes and cables. The initial and final capacitance values only show 5% and 7% variation, respectively, from the values at room temperature; whereas the required tuning bias shows larger variation of 9%. These results are consistent with ANSYS simulations; the deformation of the top membrane as a result of temperature change is small as the uniformly induced stress is well relieved, laterally.

The tuning speed of the varactor is measured using the setup discussed in [26]. Fig. 12 shows the response of the capacitor (the detected output of the power detector) when 15 V and 40 V of tuning bias is applied, respectively. From the ringing seen in Fig. 12, the mechanical resonance frequency is extracted to be 25 kHz. The measured resonance frequency is in good

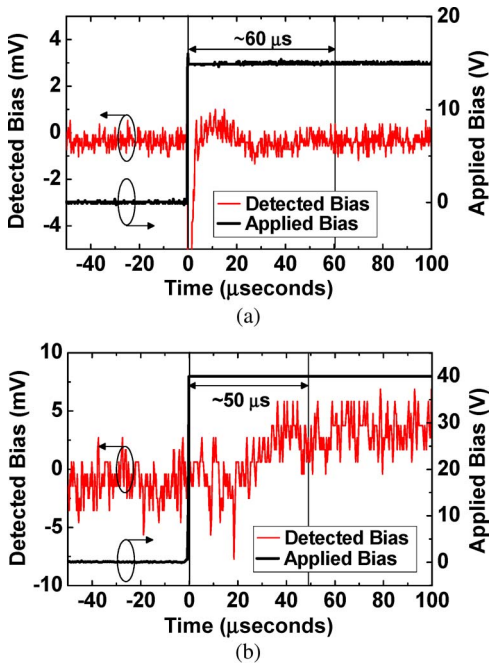

Fig. 12. Tuning speed measurement: (a) with 15 V of tuning bias and (b) with 40 V of tuning bias.

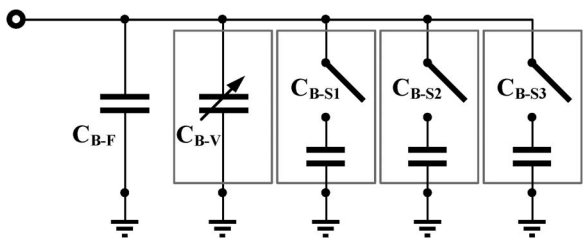

Fig. 13. Schematic view of the tunable capacitor array.

agreement with the ANSYS simulation results (i.e., 25 kHz measured versus 23 kHz simulated). The stabilization time is less than 80 μs.

B. Tunable Capacitor Bank

The tunable capacitor in the previous section has an initial capacitance of 200 fF. To increase the initial capacitance value, a tunable capacitor bank is designed, comprising of one fixed capacitor $(C_{\text{B-F}})$, one varactor $(C_{\text{B-V}})$, and three capacitive switches $(C_{\text{B-S}})$ as shown in Fig. 13. The tuning mechanism is as following: first, the varactor is tuned to its maximum value; next a switch is turned on and the varactor is simultaneously released. For further tuning, the varactor is tuned again until it reaches its maximum value and the next switch is turned on. To achieve continuous tuning, the maximum capacitance of the switched capacitor is designed to be slightly smaller than that of the varactor. The reason to integrate a single varactor and multiple capacitive switches is to improve the fabrication yield and ease the tuning control.

Fig. 14 shows a SEM view of a fabricated tunable capacitor array. The thick copper layer is utilized for routing between the capacitors in the bank and the ground ring in order to minimize

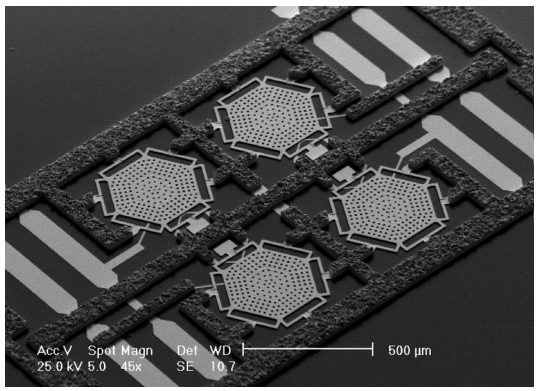

Fig. 14. SEM view of the fabricated tunable capacitor array.

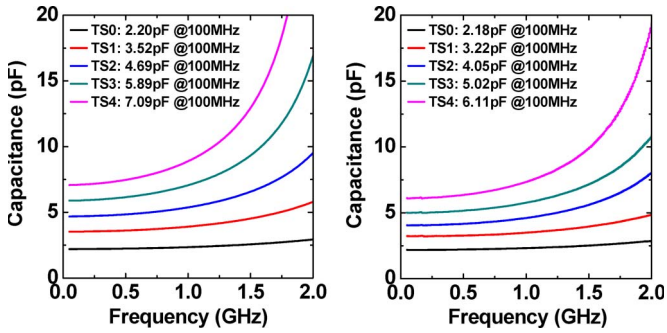

Fig. 15. Extracted capacitance of the tunable capacitor bank at each tuned state: simulation result (left) and measurement result (right).

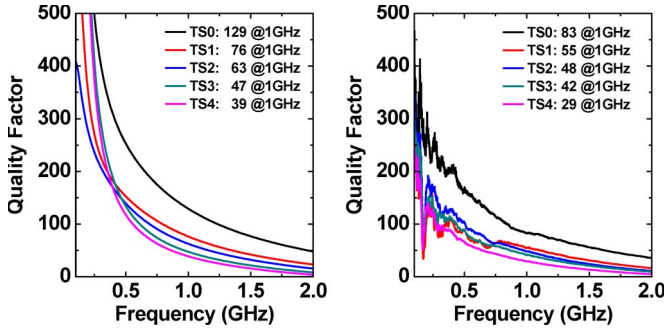

Fig. 16. Extracted Q of the tunable capacitor bank at each tuned state: simulation result (left) and measurement result (right).

RF losses. For insulation of the dc bias lines, 2 μm air bridges are used between the ground and the bias lines. MIM capacitors are implemented using the two thick top metal layers. The MIM capacitors, with a higher capacitance density of 0.4 fF/μm^2 and higher Q compared to the varactors, are used to adjust the initial capacitance value.

The measured and simulated capacitance values at each tuned state are shown in Fig. 15. Tuning state N indicates that N numbersof tunable capacitors are completely tuned. The measured tuning range of capacitance is from 2.2 pF to 6.1 pF, which is smaller than the simulated value in HFSS (i.e., 2.2 pF to 7.1 pF). As described earlier, the membrane deformation and rough surfaces are the reasons for this discrepancy. As expected, the measured Q is also smaller than the simulated value (Fig. 16).

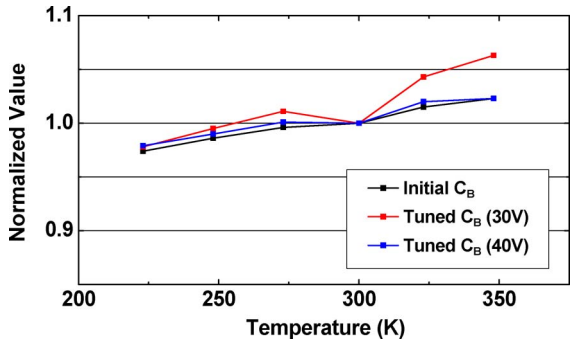

Fig. 17. Temperature variation measurements of the tunable capacitor bank; normalized value of the initial and tuned capacitance with 30 V and 40 V of dc bias.

The temperature variation is performed at different tuning states of the tunable capacitor bank (Fig. 17). Compared to the initial and final tuned states of the varactor, the intermediate tuned state at dc bias of 30 V shows more temperature sensitivity of up to 8.5% over temperature range of 223 K to 348 K.

Table II lists the specifications of recently published, high-performance, continuously tunable capacitors. In order to utilize the capacitor in RF front-ends, all performance aspects of the device need to be carefully addressed; some or none of which is considered for most reported tunable capacitors. These include tuning speed, initial capacitance value, Q, SRF, and temperature stability. The presented tunable capacitor exhibits high Q, high continuous tuning range, and good temperature stability. By placing such high-performance tunable capacitors in a bank, larger value continuously tuned capacitive elements are demonstrated. To our best knowledge, this is the highest performance capacitor bank that offers continuous tuning. Compared to other reported capacitor banks that are switched or digitally tuned [38], [39], the presented capacitor bank offers higher tuning resolution at the cost of lower Q and slower tuning speed.

C. Coupled Inductors

All inductors are designed using the two electroplated metal layers, Au and Cu, to obtain high Q and SRF. To reduce parasitic capacitance and enhance the SRF, the bottom interconnection layer (electroplated Au) is separated from the top copper layer using an air gap of 2 μm. As a proof of concept, a mutually coupled inductor pair is designed. To achieve high $Q(> 40)$ and sufficient coupling constant (> 0.2), the planar configuration is used and the inductor shapeis adjusted to allow larger overlap. The fabricated coupled inductor pair is shown in Fig. 18.

The simulated and measured inductance value is shown in Fig. 19. The extracted effective self-inductances (L_1, L_2) are larger than the simulated value because of larger capacitive parasitics. The measured coupling constant also shows slight difference with the simulated value, which might be due to the substrate characteristics and inaccuracy of simulations. The same trend is observed in the measured Q. Due to the larger

TABLE II
COMPARISON BETWEEN THE HIGH-PERFORMANCE CONTINUOUSLY TUNABLE CAPACITORS

	Rijks '06 [17]	McFeetors '06 [35]	Mahameed '10 [36]	Shavezipur '10 [37]	**This work (a single varactor)**	**This work (a capacitor bank)**
Initial Capacitance	0.26 pF	0.31 pF	0.09 ~ 0.10 pF	1.20 pF	0.22 pF	2.18 pF
Tuning Ratio	4.5	6.2	2.8 ~ 3.3	10.5	6.0	2.8
Quality Factor (at down-state Cap.)	> 100 @ 4 GHz, 1.17 pF	> 100 @ 20 GHz, 1.40 pF	> 100 @ 5 GHz, 0.29 to 0.31 pF	N / A	> 65 @ 1 GHz, 1.33 pF	> 50 @ 600 MHz, 6.11 pF
Tuning Speed	< 400 μs	N / A	N / A	N / A	< 100 μs	< 100 μs
Max. Bias	30 V	45 V, 80 V	75 ~ 80 V	40 V	35 V	35 V
Temperature Stability	< 20%	N / A	< 10%	N / A	< 9%	< 9%

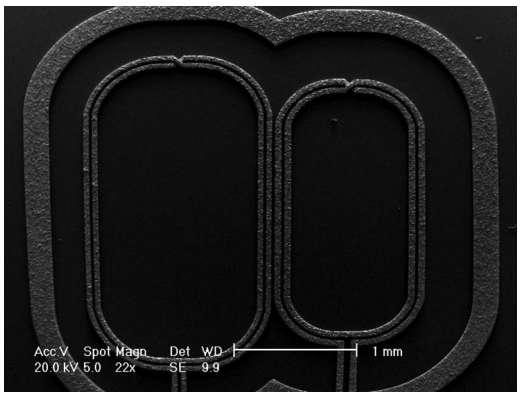

Fig. 18. SEM view of the fabricated coupled inductors.

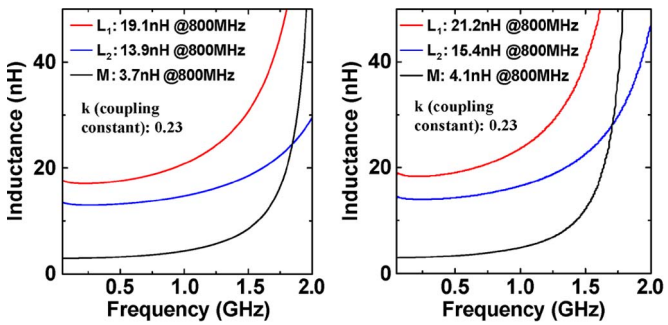

Fig. 19. Extracted inductance from simulation (left) and measurement (right).

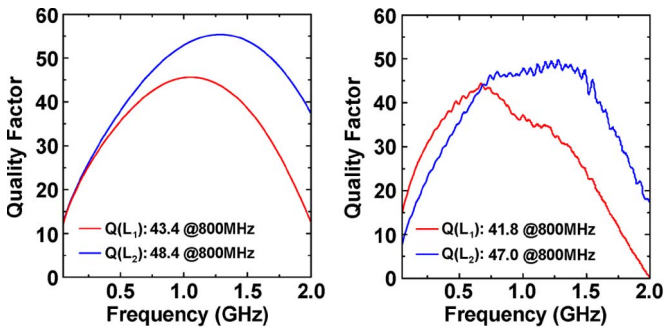

Fig. 20. Extracted Q from simulation (left) and measurement (right). The drop of quality factor at 900 MHz is due to the substrate effects.

substrate loss and parasitics seen in the fabricated devices, the measured Q and SRF are slightly lower than the simulated values (Fig. 20).

IV. CONCLUSION

A surface micromachining technology is described which allows fabrication of high-performance RF passive components at low temperature and low cost. Several high-performance components were developed, including a tunable capacitor bank and a coupled inductor pair. The presented passive components can be utilized as a part of the RF front-end systems such as tunable antennas, phase shifters, matching networks, and tunable band selection filters. The presented fabrication technology can be extended to implement other passive components and circuits.

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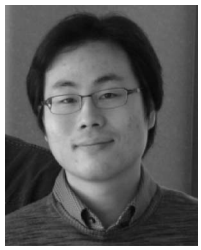

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