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List of Abbreviations

AC	Alternative Current
ADC	Analog-to-Digital Converter
ASK	Amplitude Shift Keying
BEOL	Back End Of Line
BiCMOS	Bipolar-CMOS
BPSK	Binary Phase Shift Keying
BWRC	Berkeley Wireless Research Center
CB2	Copper Bondpad
CCDF	Complementary Cumulative Distribution Function
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
CPW	Co-Planar Waveguide
CA	Cascode
CS	Common Source
DAC	Digital-to-Analog Converter
DAT	Distributed Active Transformer
DC	Direct Current
DCT	Direct Conversion Transceiver
DDRT	Software Defined Radio Transceiver
DK	Design Kit
DS-UWB	Direct Sequence UWB
DUT	Device Under Test
ECMA	European Computer Manufacturers Association
EM	Electro-Magnetic
ESD	Electro-Static Discharge
FCC	Federal Commission Communication

FDTD Finite-Difference Time-Domain
FEM Finite Element Method
FET Field-Effect Transistor
FIR Finite Impulse Response
FoM Figure of Merit
FSK Frequency Shift Keying
GaAs Gallium Arsenide
GaN Gallium Nitride
GPT General Purpose Transistor
HB Harmonic Balance
HD High Definition
IC Integrated Circuit
IEEE Institution of Electrical and Electronics Engineers
IF Intermediate Frequency
IRF Image Radio Frequency
ISM Industrial, Scientific and Medical
ISSCC International Solid-State Circuits Conference
ITRS International Technology Roadmap for Semiconductors
LDMOS Laterally Diffused Metal Oxide Semiconductor
LRM Line-Reflect-Match
LRRM Line-Reflect1-Reflect2-Match
LNA Low Noise Amplifier
LO Local Oscillator
LOS Line-Of-Sight
LPT Low Power Transformer
LTCC Low Temperature Co-fired Ceramic
MIMO Multiple-Input Multiple-Output
MMIC Monolithic Microwave Integrated Circuit
mmW millimeter Wave
MS MicroStrip
NDF Normalized Determinant Function
NF Noise Figure
NLOS Non-Line-Of-Sight
OFDM Orthogonal Frequency Division Multiplexing
OOK On-Off Keying
PA Power Amplifier
PAPR Power Average to Power Ratio

PCB	Printed Circuit Board
PDF	Probability Distribution Function
PGS	Patterned Ground Shield
PHEMT	Pseudomorphic High Electron Mobility Transistors
PLL	Phase Locked Loop
PPM	Pulse Position Modulation
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QoS	Quality of Service
QPSK	Quadrature PSK
RF	Radio-Frequency
RX	Receiver
SCBT	Single Carrier Block Transmission
SDRT	Software-Defined Radio Transceiver
SGS	Single-Ground-Signal
SGS	Single-Ground-Signal
SHT	Super-Heterodyne Transceiver
SiGe	Silicon Germanium
SiO2	Silicon Dioxide
SiP	System in Package
SNR	Signal-to-Noise Ratio
SoC	System on Chip
SOLT	Short-Open-Load-Through
SR	Software Radio
SRF	Self-Resonant Frequency
SW	Sine Wave
TEM	Transverse Electromagnetic
T-lines	Transmission lines
TRL	Through-Reflect-Line
TX	Transmitter
UCLA	University of California
UWB	Ultra-Wideband
VCO	Voltage-Controlled Oscillator
VNA	Vector Network Analyzer
WCDMA	Wide band CDMA
WLAN	Wireless Local Area Network
WiFi	Wireless Fidelity
WPAN	Wireless Personal Area Network

List of Notations

$ACPR$	Adjacent Channel Power Ratio
BER	Bit Error Rate
C	capacitance
C_{ds}	Drain to Source Capacitance
$Choke - L$	Choke Inductors
C_{gs}	Gate to Source Capacitance
C_{gd}	Gate to Drain Capacitance
C_p	Parasitic Capacitance
D	Diameter
E_c	Critical electric field
E_g	Gap Energy
$EIRP$	Equivalent Isotropically Radiated Power
EVM	Error Vector Magnitude
f_{max}	Maximum Frequency of Oscillation
f_t	Transition Frequency
G	Gap
G_{av}	Available gain
$GBps$	GigaByte per second
G_c	Compression Gain
G_{op}	Operating gain
G_{tr}	Transducer Gain
g_m	Transconductance
h	Height
IL_M	Minimum Insertion Loss
J_c	Current Density
k	Thermal Conductivity
K	Coupling Factor
L	Inductance

L_d	Drain Inductance
L_g	Gate Inductance
L_s	Source Inductance
$MBps$	MegaByte per second
N_C	Number of Cells
N_F	Number of Fingers
NSh	Non-Shielded
OBO	Output Back-Off
$OCP1$	Output 1dB Compression Point
PAE	Power Added Efficiency
P_{in}	Input Power
P_{DC}	DC power consumption
P_{out}	Output Power
P_{outAV}	Average Output Power
P_{Peak}	Peak Power
P_{sat}	Saturated Power
PBO	Peak Back Off
Q	Quality Factor
λ	Wavelength
r	Impedance Transformation Ratio
R	Resistance
R_d	Drain Resistance
R_g	Gate Resistance
R_s	Source Resistance
S	Distance
Sh	Shielded
SiO_2	Silicon Dioxide
T_r	Rise Time
$tg(\delta)$	Loss Factor
V_{sat}	Saturated Velocity
V_k	knee Voltage
w	Width
W_F	Finger Width
W_T	Transistor Width

Z_c	Characteristic Impedance
Z_{in}	Input Impedance
Z_{opt}	Optimum Impedance
Z_{out}	Output Impedance
Z_L	Load Impedance
Z_s	Source Impedance
Z^*	Conjugate Impedance
η_d	Drain Efficiency
ϵ_r	Effective dielectric constant
δ	Skin Depth
μ	Mobility
μ	Mobility
ϵ_r	Relative Permitivity
γ	Complex Propagation Constant
γ_{in}	Input Reflection Coefficient
γ_{out}	Output Reflection Coefficient

Introduction

Telecommunication industry claims for increasing data rate in wireless communication systems. Nowadays, current data rates of radio communication systems are limited to some 100Mbps. This limitation is the result of the high saturation and the coexistence of wireless standards in frequency bands below 10GHz. Despite of the domination of Radio Frequency (RF) wireless devices, mature standards such as Wi-Fi, Bluetooth and UWB can not anymore support both high data rates and strong power specifications.

The major demand of high data rate applications concerns a large panel of home multimedia exchanging data especially for the uncompressed HD data transfer. A particular interest is to operate beyond RF domain to target that demand. Operating at millimeter-Wave frequencies (mmW) frequencies becomes attractive because of the availability of large free frequency band without any close neighbor standards. The 7GHz band around 60GHz is free of use and fulfills the short range gigabit communication requirements.

Semiconductor foundries are getting involved in wireless HD products to ensure a data rate superior to 1Gbps. Based Gallium Arsenide (GaAs) or Silicon Bipolar technologies are well suited to mmW applications and were adopted for first designed products. Those wireless HD products target a large number of consumers. They are subject to cost, size and performances constraints. Their use is costly which prevents from targeting a large scale market.

CMOS technology is known to be the best process for designing digital circuits. More than 80% of the total amount of integrated circuits are designed with that technology. This is the major reason why semiconductor foundries investigate in CMOS technologies even for the design of analog circuits. It drives a fast time to market with a low cost for high integration volume. Hence, a fast improvement in CMOS technology has been seen during the last decade. In this context, emerging CMOS technologies enable for operating at mmW frquencies promising to be competitive against III-V technologies. IBM, IMEC, STMicroelectronics and other companies are now developing complete CMOS technology transceiver operating above 60GHz.

This thesis work is in the frame of the *NANOCOMM* ANR project and the European *QSTREAM* project. A 65nm CMOS technology is provided by STMicroelectronics. Those projects aim at realizing low-cost, highly-integrated CMOS transmitter prototypes sending data up to 1 Gbps in a range up to 1 meter to target 60GHz WPAN applications.

The design of 65nm CMOS technology on bulk Power Amplifier (PA) dedicated to 60GHz WPAN standard is here investigated. The designed PA aims at being integrated in mobile device. The optimization of power consumption is one of the major requirement to be focused on because of the limited life time of the battery. Moreover, the PA linearity specification must be also optimized because the 60GHz WPAN standard uses OFDM modulation scheme. The use of the emerging 65nm CMOS technology makes the PA design challenging to meet a good linearity-power consumption trade-off. Indeed, the technology downsizing leads to a reduction of the breakdown voltage and thus sets a low voltage supply. Hence, a high current density is required to provide high output power causing an important dissipated power especially with technology on bulk.

Chapter 1 exposes an overview of PA dedicated to 60GHz WPAN standard. The main applications and the characteristics of the physical layer such as the frequency plan, the modulation and the data rate of the WPAN standard are reminded. As the PA structure also depends on the system architecture, different transceiver architectures are exhibited. The PA fundamentals are depicted to highlight the technological bottleneck and the modulation issues. A state of the art enlists 60GHz CMOS PA realizations detailing their respective novelties.

Chapter 2 presents the characterization and the optimization steps of passive devices before PA design. Working at 60GHz requires a good knowledge of the 65nm CMOS technology from STMicroelectronics before being adopted in the design. *mmW* physical phenomena are quoted and their consideration using HFSS simulator are detailed. As the 65nm CMOS passive components have never been characterized above 60GHz, their electrical behavior at RF and *mmW* frequencies is studied. The impact of layout geometry and substrate to construe simulations and to predict measurements are analyzed. The characterization of T-lines, inductors and RF pads is presented. Optimized structures are proposed.

Chapter 3 focuses on the PA design. It firstly discusses about the defined design flow to design a generic *mmW* PA. Secondly, additional considerations are studied according to issues met during the design of preliminary PAs. Then, two 65nm CMOS PAs realizations

designed with different topologies are described. The first PA is a single-ended topology while the second one is differential. Their respective simulation and measurement results are analyzed. To compare our works, our designed PAs are compared with the ones in a state of the art targeting the same application to highlight the CMOS PAs performances with other competitive technologies. Finally, promising future works are presented.

Chapter

1 Overview of PA design for 60GHz WPAN applications

Contents

Chapter 1 presents an overview of PA dedicated to 60GHz WPAN standard. A low cost fabrication with CMOS technology is adopted to fulfill a large scale market. The first part demonstrates how the 60GHz band is a promising way to reach gigabit data rate. Different transceiver architectures are exhibited. The second part presents the PA fundamentals with a focus on PA design constraints related to technology scaling, high operating frequency and modulation issues. Finally, a state of the art lists 60GHz CMOS PA realizations detailing their novelties.

Key words: 60GHz standard, CMOS, multimedia convergence.

1.1 60GHz WPAN background

1.1.1 Power devices: CMOS, a key for the future

The choice of a technology is related to the constraints of the circuit to be designed. Those constraints are technical, strategical and economical. All these considerations must be analyzed. Designers and managers background is required to determine pro and cons for each process to focus on the most adapted one.

Devices are manufactured on different substrates. Besides acting as mechanical support structures, they directly affect the circuit performances. Two main reasons create the substrate coupling with the circuit. In one hand, the voltage supply to ground commutation in a mixed circuit presents a noise source for the substrate. In the other hand, a non-ideal dielectric leads to current propagation in the substrate. Each material is characterized by the relative permittivity (ϵ_r), the loss factor ($tg(\delta)$) and must ensure process requirements such as a low roughness. For microwave power applications, high thermal conductivity (k) and high resistivity (ρ) (or low mobility (μ)) are highly demanded at high operating temperature. Moreover, the substrate height (h) is a geometric parameter that involves the thermal characteristics. Indeed, a thin wafer is necessary to improve thermal dissipation while keeping the support solid. The most used substrate in this context are GaAs, SiC and Si.

Table 1.1: Physical parameters for Si, GaAs and α-SiC substrates

Material	$k_{@300\,\deg}$ $(W/(K.cm)$	$\mu_{e@300K}$ $(cm^2/(V.s))$	ζ_r	$tg(\delta)_{@10GHz}$
Si	1.5	< 1450	12.7	10^{-3}
GaAs	0.45	< 8500	12.8	$4 * 10^{-4}$
α-SiC	4.2	$420 < \mu_e < 950$	10	–

Table 1.1 reports their electric and thermal characteristic parameters. Globally, the III-V technologies present higher ρ and support higher breakdown voltage compared to the silicon ones. They have been widely used for microwave power applications in the past. They are still more suited to power devices such as base stations and military radars. Nevertheless, silicon technologies benefit from a high K and takes advantages to GaAs in terms of technology maturity with large possibilities for post process such as growing oxides, flip chip bumping and bonding technologies. III-V technologies are expensive and are not adapted to large scale market. SiC enjoys inherent advantages over Si and GaAs for high-temperature sustaining and high thermal conductivity. It includes LEDs and high-power switching devices. However, the disadvantages of this substrate are still the high cost and the process difficulty to growth Gallium Nitride(GaN). SiC substrate is available in several forms such as 4H-SiC and 6H-SiC.

When the substrate is chosen, in most cases, an hetero-junction is integrated to improve power and gain capabilities and thus, the efficiency of a transistor to operate at high temperature and at high frequency. The most relevant physical indicators are:

- The band gap energy (E_g): a high band gap value lowers the intrinsic carrier density even at high temperature limiting the leakage currents in the transistor. The gap sets the critical electric field (E_c) which determines the breakdown voltage and thus the maximum power supported by the device.

- The mobility (μ): electrons and holes are driven when an electric field is applied to a semiconductor. They reach the saturation velocity (V_{sat}) under a significant electric field setting the maximal current density. V_{sat} depends on the interactions in the crystalline structure. Consequently, hetero-junctions are added to reach higher current densities since it confines carriers in a quantum well. Hence, the mobility is greatly increased.

Specific semiconductor technologies are used to answer to PA requirements. Their parameters are reported in Table 1.2 [1]. They impact on Power Amplifier (PA) performances.

Table 1.2: Comparison of the principal materials properties

Transistor	$E_g(eV)$	$E_c(V/cm)$	$\mu_e(cm^2/(V.s))$	$V_{sat}(cm/s)$
Si	1.12	$3*10^5$	< 1450	10^7
$Si_{1-x}Ge_x$	$1.12-0.41x+0.008x^2$	$< 3*10^5$	$1450-4325x$	–
$GaAs$	1.43	$4*10^5$	< 8500	10^7
GaN	3.43	$5*10^6$	< 1000	$2*10^7$
$Al_xGa_{1-x}As$	$1.424+1.247x$	$5*10^5$	$8000-22000x+10000x^2$	–
$Al_xGa_{1-x}N$	$6.026x+3.39(1-x)$	$1.4*10^6$	$300x+1000(1-x)$	–

- Gallium Arsenide (GaAs) based Pseudomorphic High Electron Mobility Transistors (PHEMT) and Hetero-junction Bipolar Transistor (HBT): their use is widespread for cellphones since they offer promising capabilities for high linearity applications. For X band (10GHz) applications, the measured power density in a PA reaches $3W/mm^2$ and only $0.5W/mm^2$ for the HBT GaAs and PHEMT GaAs respectively [2]. Their major drawback is the high thermal resistance that limits the maximum dissipated power in a defined area.

- AlGaN/GaN HEMT on SiC: most of the promising results for GaN are achieved. They demonstrate very high power densities achieving (6-9 W/mm^2) at 10GHz. The relative technology immaturity of GaN with respect to Si and GaAs leaves unanswered issues like longterm reliability. According to the International Technology Roadmap for Semiconductors (ITRS), the GaN HEMTs are said to become the reference technology for power applications at operating frequencies until 40GHz [3].

- Laterally Diffused Metal Oxide Semiconductor (LDMOS) transistor: it is derived from low cost MOSFET device. It benefits of good electrical and thermal characteristic ensuring high power level. This technology is used for cellular systems from 400MHz to 3.5GHz. It supports up to 32V voltage supply. It presents a serious competitor for GaAs PA device. This technology is not yet suited for frequencies beyond 10GHz and not alone for a high integration level since their large area comparing with bipolar transistors.

In parallel, the fast improvement in Complementary Metal Oxide Semiconductor (CMOS) scaling enables designing high speed circuits with small die size to reduce significantly the cost. Indeed, CMOS process is the best process to design digital circuits (processor, memory) which presents more than 80% of the total amount of Integrated Circuits (IC)(Figure 1.1) [4]. This is the major reason that influences semiconductor foundries to fabricate chips only with CMOS

technology. It drives a fast time to market. In addition, digital and analog designers communicate more often avoiding big conflicts when assembling analog and digital part in transceiver.

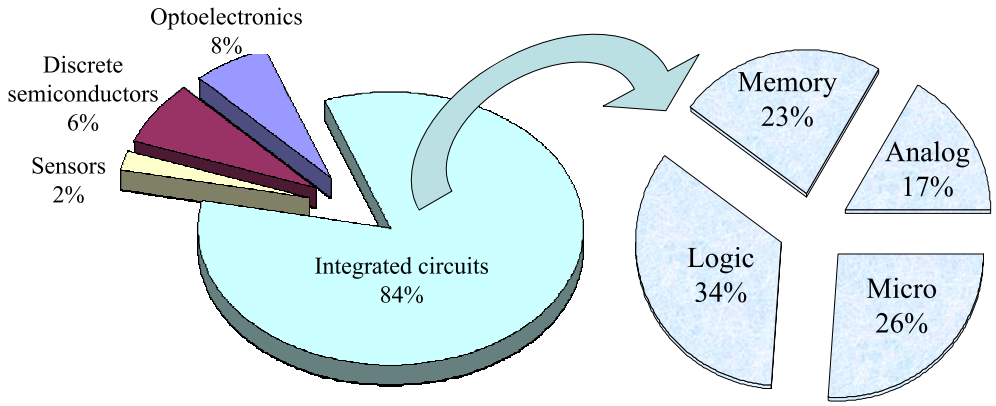


Figure 1.1: Semiconductor market share

Consequently, several research axes have been initiated to design PAs with CMOS technologies. In [5] a 65nm CMOS PA dedicated to Wireless Local Area Network (WLAN) applications reaches 31.5dBm P_{sat} with a maximum PAE (PAE_{max}) of 25% under 3.3V of supply voltage. Other works presented in [6] [7] and [8] exhibit PAs operating at 17GHz, 24GHz and up to 140GHz respectively. The use of hetero-junction Si/SiGe is a good alternative when the system design does not require high density logic and high-performance analog. It allows having a higher Transition Frequency ($f_t > 200$GHz) and a higher gain while remaining on Si (Figure 1.2) [9].

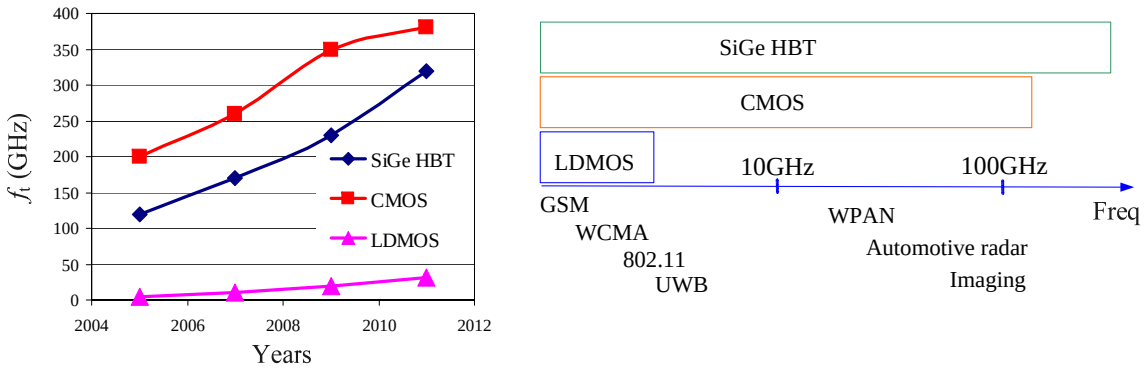


Figure 1.2: Silicon ability to target millimeter Wave applications

The ultimate goal is to find the CMOS technology limits for analog part, disregarding their less performances compared to the common power technologies, previously described.

1.1.2 60GHz band overview

The low power system standards based on Bluetooth IEEE 802.15.1 and Zigbee IEEE 802.15.4 standards have reached the maturity in terms of performances and marketplace. However, they are expected to ensure low throughput communications [10]. Designers adopt some techniques to improve the data rate, as following.

The first mean to increase the data rate is the use of the attractive Multiple-Input Multiple-Output (MIMO) technique. It allows a spatial diversity and multiplexing to increase the channel capacity within a limited frequency band [11]. It uses different antenna patterns for multiple users. It supports higher throughput to ensure classical Wireless Local Area Network (WLAN) applications by transmitting independent data streams with the same bandwidth. In addition, many algorithms are proposed to realize a beam-forming system which performs adaptive spatial signal processing with an array of antennas (Figure 1.3) [12][13]. This technique is limited due to the lower operating frequency that sets the antenna size. In this context, integrating up to two antennas in the transceiver is reasonable. The evolutionary IEEE 802.11.n standard improves the previous IEEE 802.11.a/b/g/n standards known as WiFi. The data rate is increased from 20MBps to 100MBps achieving an operating range of 100 meters.

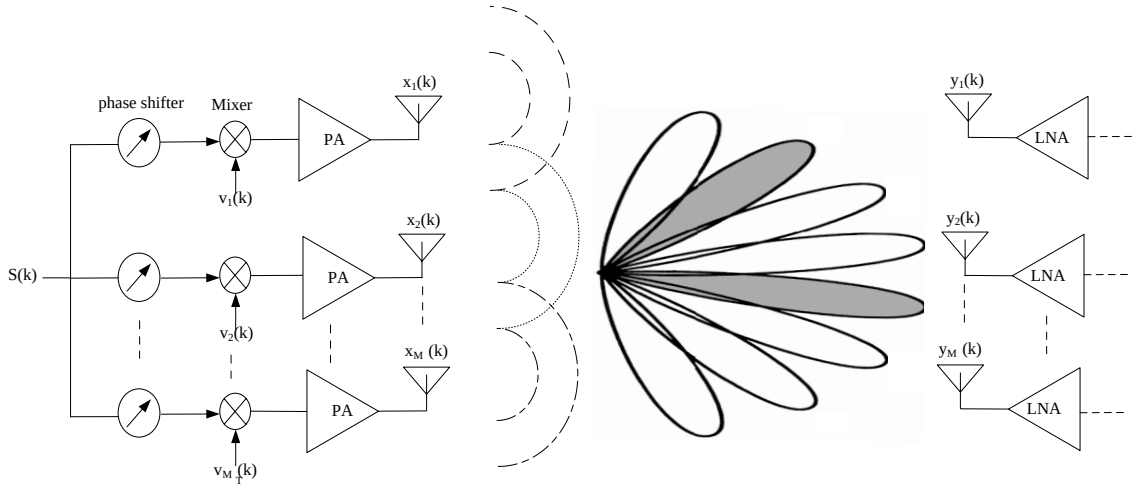


Figure 1.3: System combining MIMO and beam-forming techniques

The second mean to obtain higher data rate is to increase the channel bandwidth. This is not possible due to the standard regulations and cluttering in the Industrial, Scientific and Medical (ISM) band in 2.4GHz or 5GHz band. The available bandwidth are 70MHz and 500MHz for the 2.4GHz and the 5GHz bands respectively. This is the major limiting factor for this standard.

The other competitive standard to narrow band systems is the Ultra Wide Band (UWB). It was most often used before in confidential research in military radars development. The Federal Commission Communication (FCC) has authorized the unlicensed [3.1-10.6]GHz band to answer to the large demand for short range rapid communication standard in 2002 [14]. A fundamental difference between UWB and the traditional systems exists. Instead of transmitting a modulated Sine Wave (SW) signal, a time pulse is generated. Thanks to time-frequency domain duality, the pulse width offers a large bandwidth. The pulse encodes data with a conventional modulation like On-Off Keying (OOK), Pulse Position Modulation (PPM), Phase Shift Keying (PSK), etc. Those modulation schemes are based on Direct Sequence-UWB (DS-UWB) coding approach. This approach is attractive for its easy implementation that can be designed with low cost process. The second approach is the Pulsed-OFDM-UWB. It improves data rate communication in Non-Line-Of-Sight (NLOS) channel conditions. The [3.1-10.6]GHz band is divided into 14 sub-bands of 528MHz wide . Each sub-band contains 128 sub-carriers [15]. With this modulation scheme, data rate achieved 1.92GBps. This approach leads to expensive and complex systems. Additionally, a drastic power limitation (less than -41.3dBm/MHz) is imposed by the FCC to avoid interference issues with standards occupying the same frequency band like WiFi standard.

Figure 1.4 shows a comparison of wireless competitive standards considering the data rate, the range and the Equivalent Isotropically Radiated Power ($EIRP$).

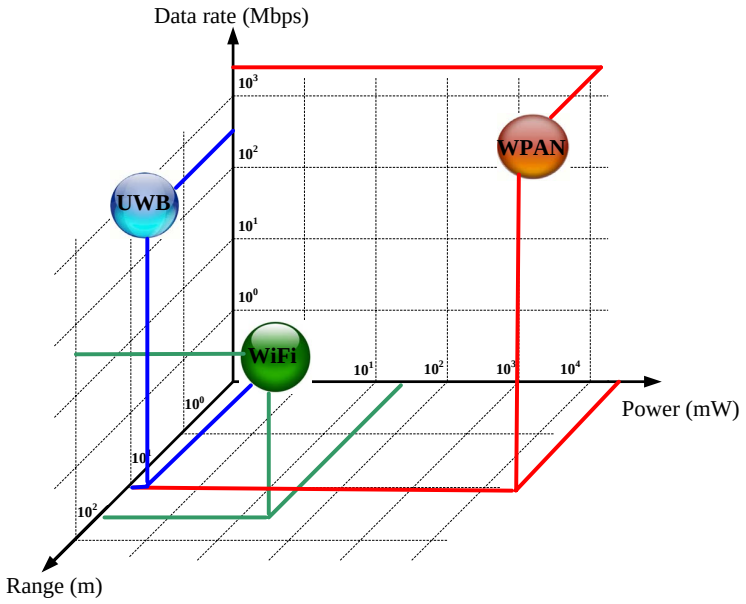


Figure 1.4: Comparison of wireless standards-setting

Somehow or other, a gigabit link is hardly feasible, even with complex modulations or with MIMO techniques. It is due to the presence of various standards operating at frequencies below 10GHz. Indeed, the ISM band hosts a multitude of standards dedicated to data and multimedia transmission. The budget link of each standard is not efficient to ensure gigabit data transmission. This is why new researches are investigating for available large bands even if they are at very high frequencies. Consequently, the unlicensed 7GHz band around 60GHz is targeted to fulfill the demand of high data rate short range communications. The emerging 60GHz standard is a very promising way to reach gigabit links.

Working at 60GHz requires new considerations especially related to technology scaling and high propagation losses in channels. The next section introduces the motivations and the context of this frequency range.

Available broadband

As discussed before, the IEEE 802.11a/b/g/n and UWB standards do not answer to gigabit data rate specifications. Those standards can be improved only by adopting complex modulations schemes requesting high cost which prevents from targeting a large scale market. A solution consists in operating in an empty wide-band without close neighbor standards to avoid coexistence issues and power constraints. The 7GHz band around 60GHz is a matter of concern and free of use and well suited to high data rate for indoor Wireless Personal Area Network (WPAN) applications. The FCC sets aside this band in 2001 [16]. The neighbor millimeter Wave (mmW) applications occupy the 24GHz and 77GHz bands, dedicated to radar applications (Figure 1.5). Consequently, there is no interference issues between these mmW applications. Moreover, they operate in different environments namely the indoor environment for WPAN communications and the car environment for radar applications.

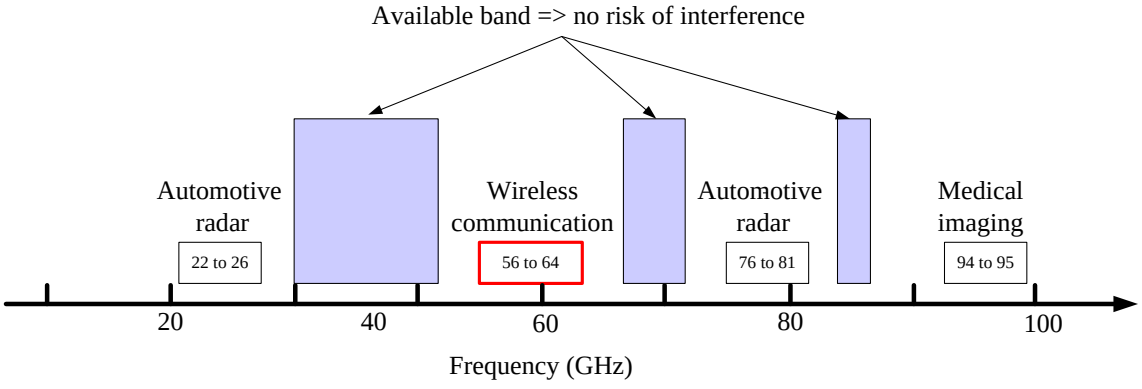


Figure 1.5: Millimeter-wave applications

Scaling components

The requirements for microelectronics industry is striving to reduce die size. The main motivation to operate towards high frequency is the technology down-scaling. Reaching higher frequency is one of the best way to integrate all components at least in a small die area and why not, in a single chip. Thus, System in Package (SiP) and System on Chip (SoC) integrations are a promising trend. Indeed, lumped passive devices are more compact. The size of passive devices as Transmission lines (T-lines) and antennas are set in function of the wavelength. At 60GHz, the wavelength is only 2.5mm in the Silicon Dioxide (SiO_2). Hence, the integration of network containing 4 or 8 antennas becomes realistic to improve the antenna's directivity. Likewise, MIMO systems are more suitable at high frequency since two adjacent antennas are separated by a low distance. Finally, the die area gain exists due to the transistor scaling.

Oxygen absorption

A particular interest of the band around 60GHz is due to a natural phenomenon. The oxygen molecule absorbs the electromagnetic energy at this specific frequencies. This absorption is the cause of a 13dB/km attenuation (Figure 1.6) [17]. That is why this band is targeted also for satellite-to-satellite communication data link. In WPAN context, this attenuation enables a high secure communication for short range distance. The 60GHz data link operates within a small geographic area without any interference with other standards or with other users working at the same frequency.

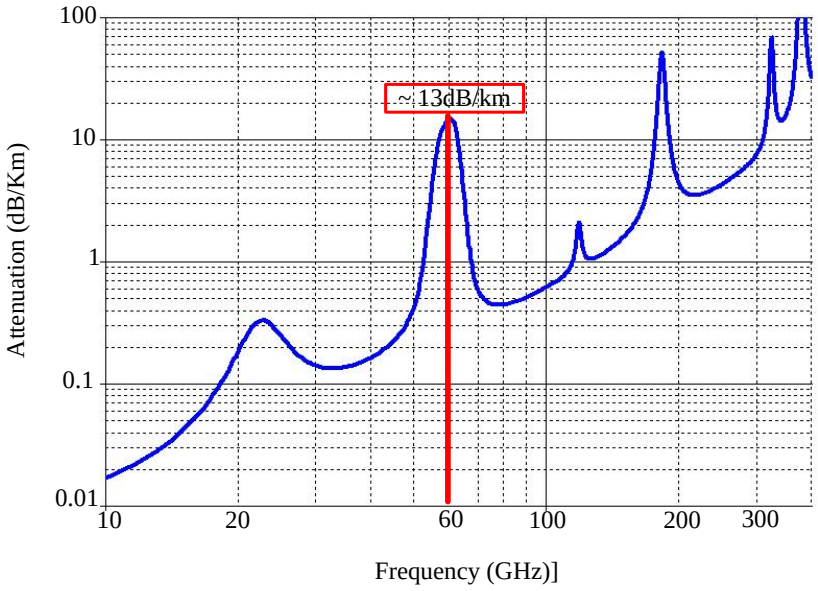


Figure 1.6: Oxygen absorption at 60GHz

60GHz channel

Dimensions of wireless link are determined by channel properties. According to the Friis propagation loss formula given by Eq. 1.1, the free-space losses are proportional to the frequency square. For instance, an additional 20dB loss is expected for a system operating at 60GHz compared to another one operating at 6GHz. These losses can be compensated by the design of a high gain and directive miniaturized antenna array to limit the number of multi-paths propagation.

$$P_r = \frac{P_t \cdot D_r \cdot D_t \cdot \lambda^2}{4 \cdot \pi \cdot R^2} \tag{1.1}$$

Where,

- P_r and P_t present the received and the transmitted power.
- D_r, D_t present the directivity of the received and the transmitted antennas.
- R presents the distance between the receiver and the transmitter.
- λ presents the wavelength.

In addition, the transitivity of the electromagnetic wave decreases at higher frequency. Consequently, walls and human body are the most common obstacle and present sources of reflection in indoor environments. Hence, the link budget study depends on the communication scenario: LOS or NLOS. The high free-space losses and low wave penetration at 60GHz confine the communication data link in one room. Table. 1.3 lists the amount of insertion losses caused by obstacles in indoor environment. A concrete wall attenuates the signal more than 40dB.

Table 1.3: 60GHz channel insertion loss

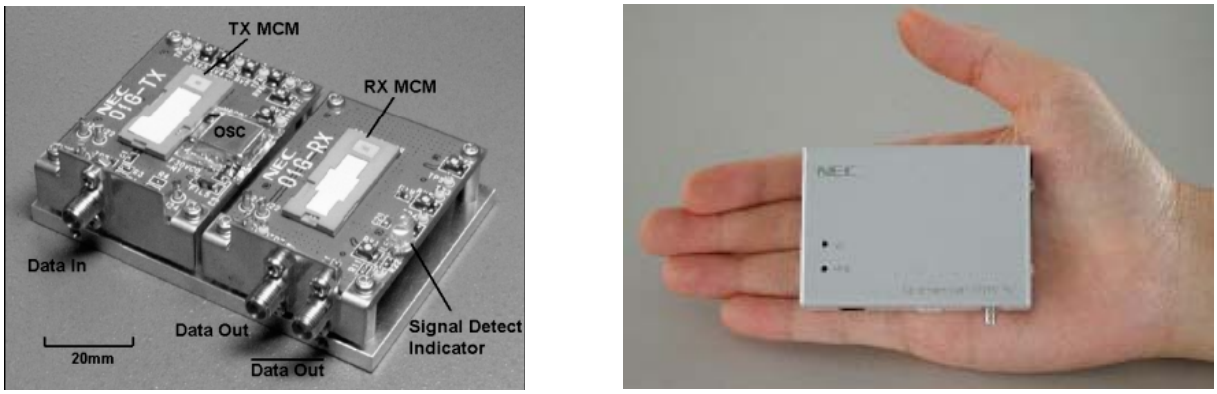
Material type	Insertion loss (dB)
Human body	20
Concrete wall	> 40
Plywood	6
Dry wall	11
Full wall	26

1.1.2.1 Standardization of the 60GHz WPAN standard

Brief history

The standardization of the 60GHz WPAN standard is the result of several works demonstrated all over the world. Academic and industrial researchers have initiated their investigations in the 60GHz band 20 years ago. The goal was to reach the maximum data rate for asynchronous transfer mode networks [18]. The most important actors who had driven ambitious projects to develop this standard are presented as follows:

In Japan, the government was probably the first to investigate in 1984 to use the mmW frequencies for WLAN applications. The main researches began in the communication research laboratory in 1992 [19]. The first 60GHz demonstrator has hardly ensured a 51MBps data rate [20]. This work has participated to regulate the 60GHz WLAN in 2001 [21]. A licensed [54-59]GHz band and an unlicensed [59-66]GHz band are authorized for high-speed data communication. NEC company was one of the most active partner publishing in 2002 a 1.25GBps 60GHz transceiver device using a Amplitude Shift Keying (ASK) modulation [22] with a $0.25\mu m$ AlGaAs/InGaAs hetero-junction FET technology (Figure 1.7).



TX and RX MCMs and transceiver module

(b) Photo of encapsulated transceiver module

Figure 1.7: NEC's AlGaAs/InGaAs transceiver module

In USA, the FCC assigned [57-64]GHz frequency band as unlicensed band for short-range high-speed communication in 2001 [23]. In 2005, an alternative group 802.15.TG3C was formed to develop a mmW based alternative standard to the 802.15.3-2003 standard to WPAN applications. Berkeley Wireless Research Center (BWRC), University of California (UCLA) and IBM were the relevant actors that investigate in this domain. IBM has presented a 60GHz chip set in 2006 [24] [25]. The TX/RX are packaged together in a chip on board assembly as depicted

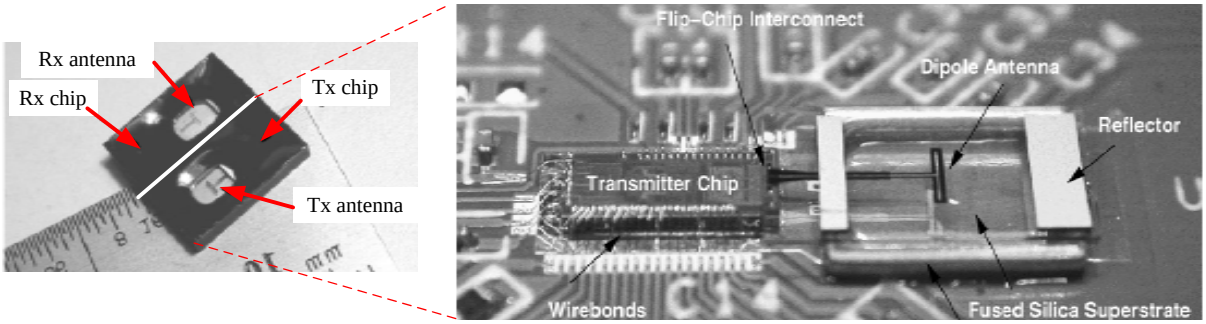
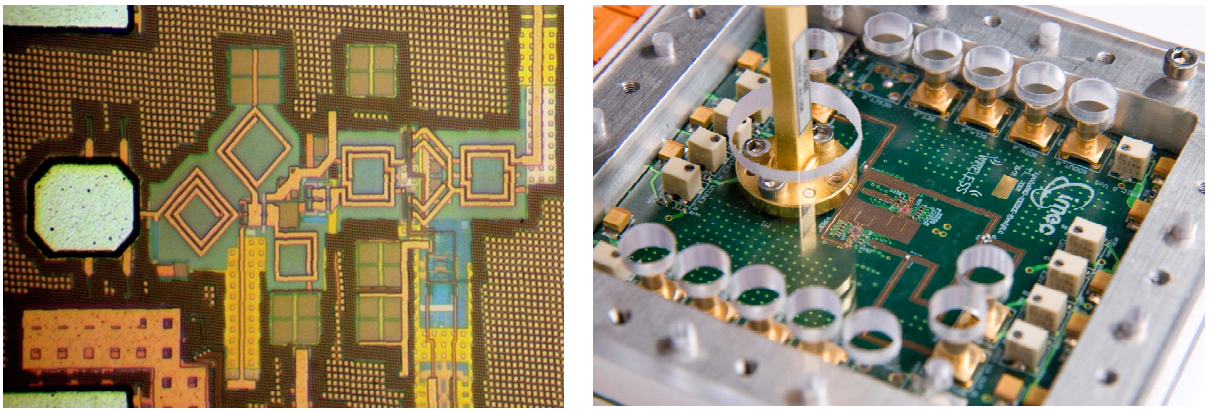


Figure 1.8: IBM's SiGe single-chip 60GHz transceiver

in Figure 1.8. The process adopted was $0.13\mu m$ SiGe technology. The transceiver achieved a 630MBps data rate over 10 meters. BWRC has brought interest to this application and designed all the transceiver. The challenge consisted in the chosen technology. Indeed, their first works were based on $0.13\mu m$ CMOS technology [26]. Recently, a 90nm CMOS transceiver was demonstrated [27].

In Europe, The MEDIAN European project (1994-1997) investigated in WLAN standard providing 150MBps data rate with a Orthogonal Frequency Division Multiplexing (OFDM) modulation. Several projects like BROADWAY, COMMINDOR, MAGNET, WINNER developed physical layer. IMEC is developing single chip 60GHz radios using advanced 45nm CMOS technology. In the International Solid-State Circuits Conference (ISSCC 2009) [28] [29], IMEC reports also a world-first mmW PA and a digitally controlled [57-66]GHz receiver with multiple antenna front-end as shown in (Figure 1.9). STMicroelectronics also brought interest in developing this application.



(a) Receiver front-end die micrograph

(b) Photo of RF front-end IC with antenna interface

Figure 1.9: IMEC's 45nm 60GHz front-end

1.1.2.2 Frequency plan

To set the 60GHz standard, Institution of Electrical and Electronics Engineers (IEEE) and European Computer Manufacturers Association (ECMA) have presented the final draft in 2008 [30] and 2009 [31] respectively. A summary of ECMA frequency plan is presented in Figure 1.10. The physical layer uses the unlicensed 7GHz frequency band around 60GHz. The channel width is set to 2.16GHz with a symbol rate of 1.72GBps for each channel. The mask depends on the targeted device type in the network.

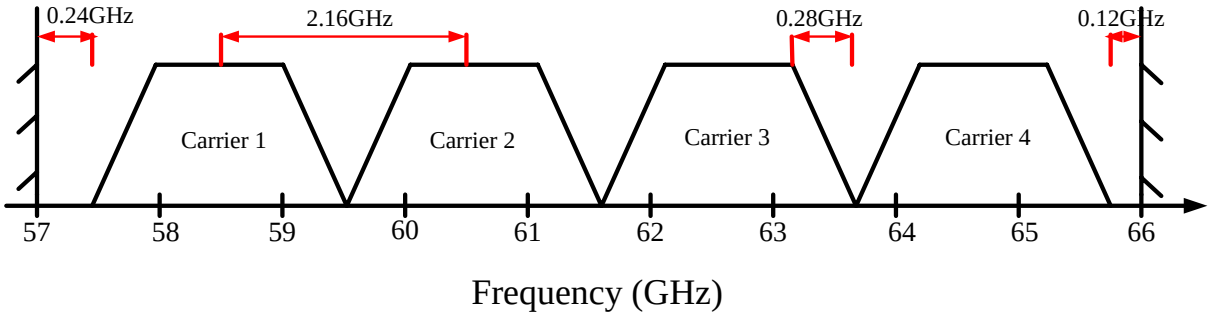


Figure 1.10: WPAN spectrum overview

1.1.2.3 Architecture network and 60GHz features

Main applications of WPAN standard are the HD video streaming and wireless docking station applications (Figure 1.11). The links can be set by point-to-point and by point-to-multi-points communication type. Otherwise, three types of devices can operate independently, cohabit and inter operate in the same area. Figure 1.12 illustrates the possible links between the 3 types of

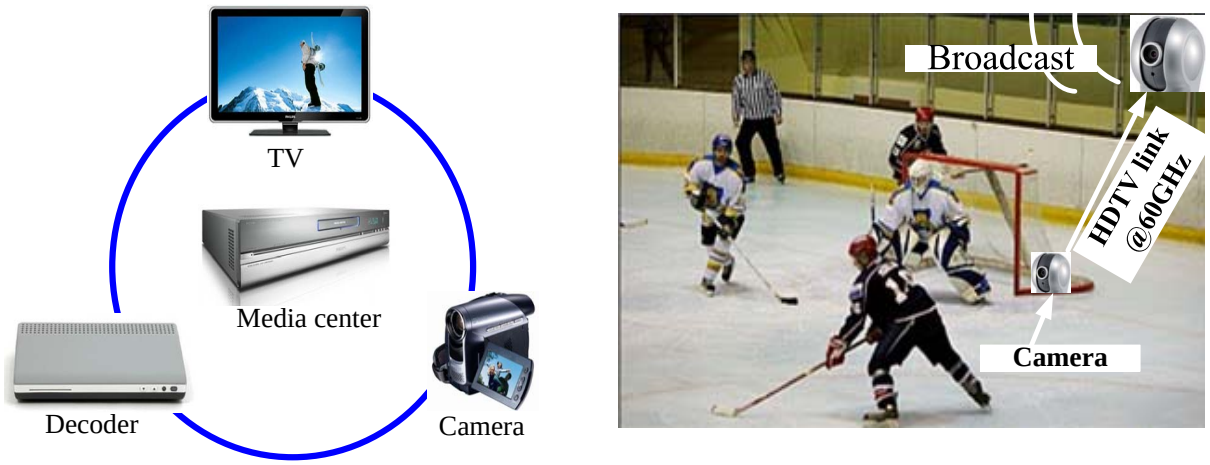


Figure 1.11: 60GHz WLAN/WPAN applications

devices. The data rate and the range of every link are also presented. It is an heterogeneous network composed by:

- Device type A: it ensures principally the uncompressed or lightly compressed video streaming over a range of 10 meters. Both LOS and NLOS scenarii are envisaged. This type of device has the highest performances. It operates following two modes:
  - with a Single Carrier Block Transmission (SCBT) mode employing BPSK, QPSK and 16QAM modulation schemes. The data link must support a data rate from 0.794GBps to 6.35GBps.
  - with an OFDM mode, data are splitted into several sub-carriers with QPSK and 16QAM modulation schemes. The data rate varies according to the adopted scheme from 1GBps to 1.588GBps.
- Device type B: it aims at transferring data, pictures and video over a shorter range from 1 to 3 meters. The communication is a point-to-point-link (LOS). It enables a lower cost implementation and a lower power consumption than type A device. Device type B uses a simplified SCBT with a 3.175GBps data rate.
- Device type C: it offers only a transmission data for LOS link. The distance between TX/RX does not exceed 1 meter without Quality of Service (QoS) guarantee. This device is considered as the less constrained and ruled device. This type uses OOK mode with a data rate up to 1.6GBps.

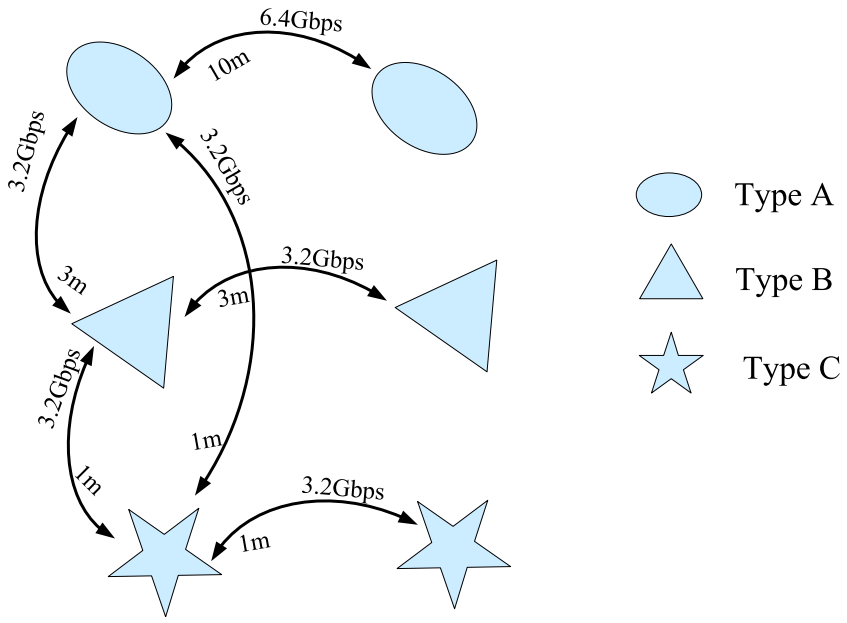


Figure 1.12: Heterogenous devices in the 60GHz WPAN

1.1.3 60GHz transceivers

Systems are built as a function of the requirements of the targeted standards. Mainly, the adopted technology node sets the cost and the performances of the transceiver. FoM must be studied before each realization (linearity of the PA, Signal to Noise Ratio (SNR), Noise Figure (NF) of the Low Noise Amplifier (LNA), selectivity of different filters or reconfigurability ...).

The classification of transceivers differs by their mean of down-conversion. Operations in the receiver are the dual of the ones with the transmitter. Three families of transceivers are reported in a realization example dedicated to the 60GHz WPAN standard.

- Super-Heterodyne Transceiver (SHT).
- Direct Conversion Transceiver (DCT).
- Software Defined Radio Transceiver (SDRT).

1.1.3.1 Super-Heterodyne Transceiver (SHT)

The SHT is the most common one. It is identified by the use of several down-converters to operate at Intermediate Frequencies (IF) before translating signal to base-band. High performances are achieved at the expense of highly selective required filters. Figure 1.13 depicts the building blocks of a SHT. The two filters located at the front end chain reject the Image Radio Frequency (IRF) and the one located at the IF chain selects the IF. The main issue consists in the necessity of several encumber components. Hence, a high integration level on chip is difficult with this traditional topology. In spite of that, this approach is useful for high-tier communications.

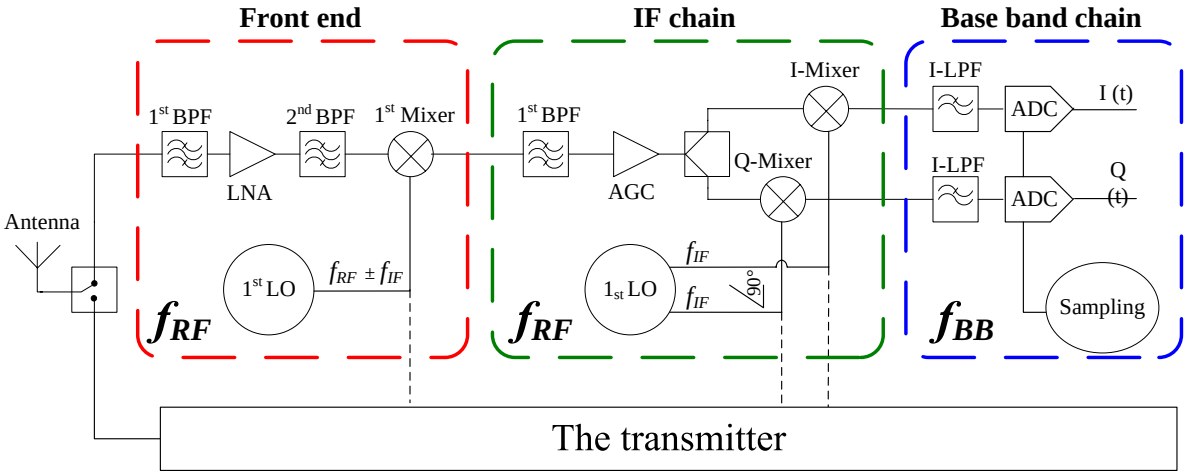


Figure 1.13: Building blocks of a SHT

For instance, [32] presents a 60GHz SHT. The TX and the RX are designed separately in 90nm CMOS technology (Figure 1.14). The digital part is integrated in the same chip. It includes an Analog to Digital Converter (ADC), a DC-offset canceler and a Finite Impulse Response (FIR) to support the heavy constraints imposed by the OFDM modulation schemes. It achieves a data rate of a 7GBps with a QPSK and a 15GBps with a 16QAM modulation scheme. The antenna is co-integrated in a low cost FR4 substrate. To avoid aliasing matters, IF must be as high as possible, from 7GHz to 13GHz. A push-push Voltage Controlled Oscillator (VCO) and a double-balanced quadrature Gilbert-cell mixer are implemented to down-convert the modulated signal to IF. The PA provides a gain of 17dB with a P_{out} of 5.1dBm.

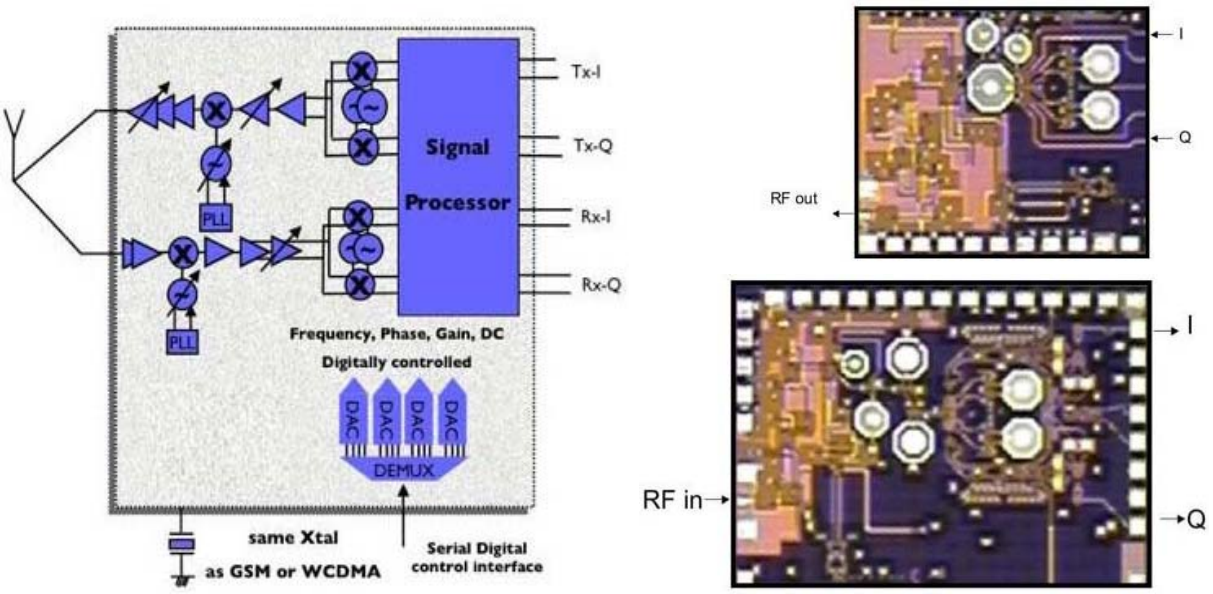


Figure 1.14: 60GHz CMOS single chip radio block diagram based on SHT

1.1.3.2 Direct Conversion Transceiver (DCT)

Figure 1.15 depicts the building block of a DCT. The front-end is simplified in this configuration. Only one Local Oscillator (LO) is used to down-convert the modulated signal to base band. In this frequency range, $1/f$ noise and DC-offset are present. The mixer must have a large dynamic range. The low pass filter located before the ADC must be designed to select the useful channel. Contrary to SHT, I/Q splitting is mandatory to not have aliasing issues. This kind of transceiver is suited for mid-tier communications.

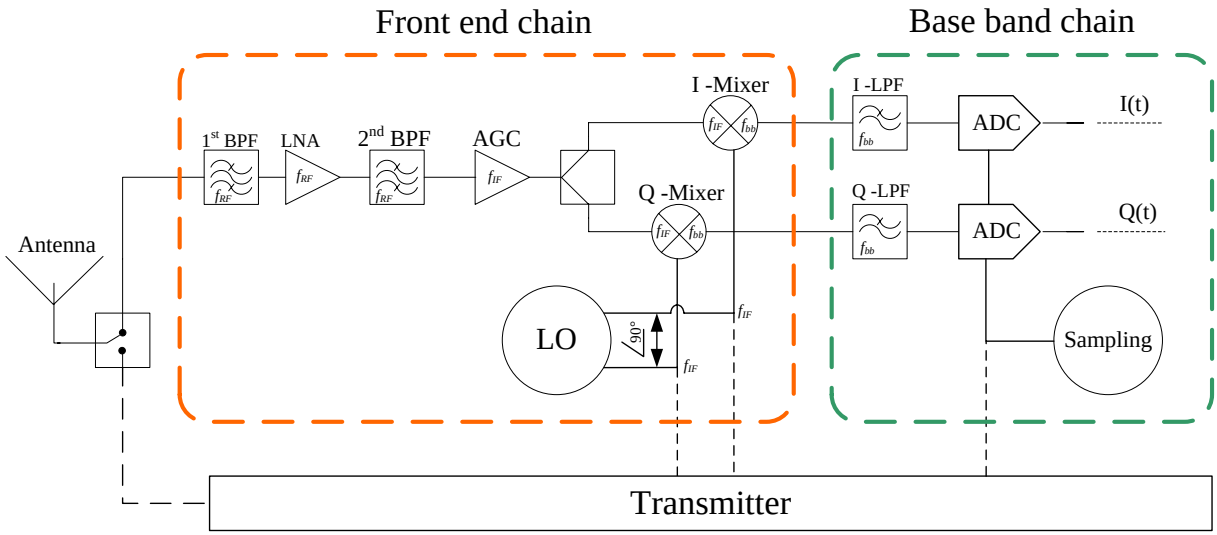


Figure 1.15: Building blocks of a DCT

For instance, [27] presents the design of a 90nm CMOS low power 60GHz DCT with its base band circuitry (Figure 1.16). The wireless link achieves a 10GBps data rate with a QPSK modulation scheme. A fully differential combined Digital to Analog Converter (DAC)-mixer structure is used for the modulator. The difficulty in this transceiver is to ensure good matching between the input of the PA and the low output impedance of the modulator. In the receiver, the LNA amplifies the received signal before being down-converted to base band. A digitally-programmable analog phase rotator is used to synchronize in phase the TX and the RX. The

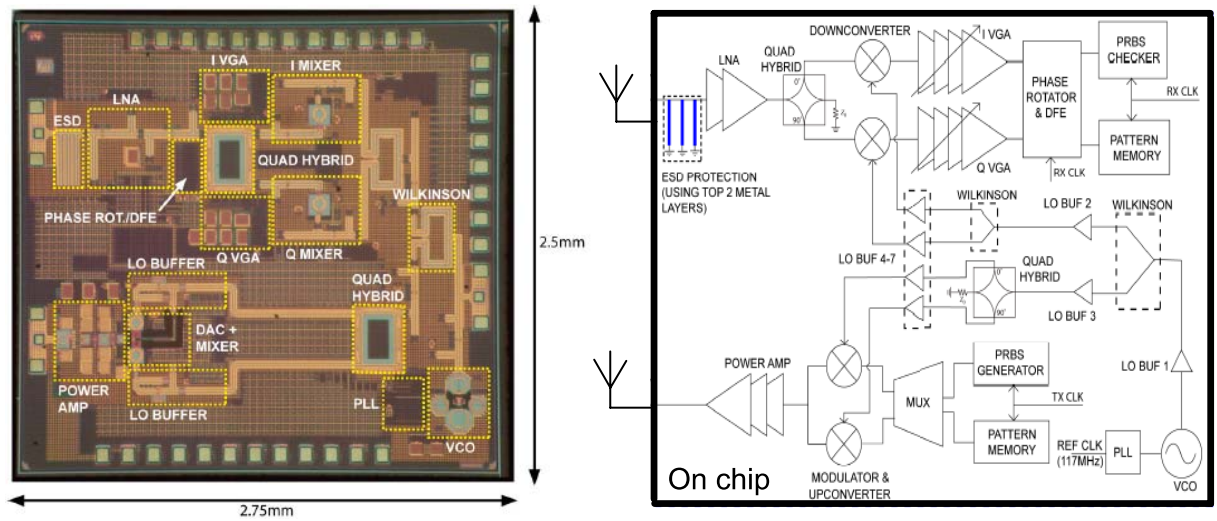


Figure 1.16: Block diagram and die micrograph of a 60GHz DCT

Phase Locked Loop (PLL) is designed at 30GHz with push-push topology to operate at 60GHz without any frequency divider. One power splitter in phase and another one in quadrature share the VCO between the TX and the RX to generate I and Q paths with a difference phase of 90deg.

A mix of the SHT and the DCT is the Low IF transceiver. It is the less common topology. It uses an IF equals to the spacing channel to release the implementation constraints. However, the transceiver requires a complex poly-phase filter. This approach is well suited for low cost communications [33].

1.1.3.3 Software Defined Radio Transceiver (SDRT)

SDRT aims at being a flexible transceiver to integrate various standards on a single chip. The concept of Software Defined Radio (SDR) paves the way to challenge this idea. Joseph Mitola exposed for the very first time the concept of Software Radio (SR) in 1995 [34], replacing the major part of dedicated analog front-end in a transceiver by a fully digital implementation monitored by software (Figure 1.17). The digital part is getting as close as possible to the antenna. Until now, this approach must support a large dynamic range of a wide diversity of standards and leads to a dramatic high power consumption. Those issues prevent from designing a full Software Radio system (SR) and constraint researchers to explore new RF architecture to fulfill SDR specifications.

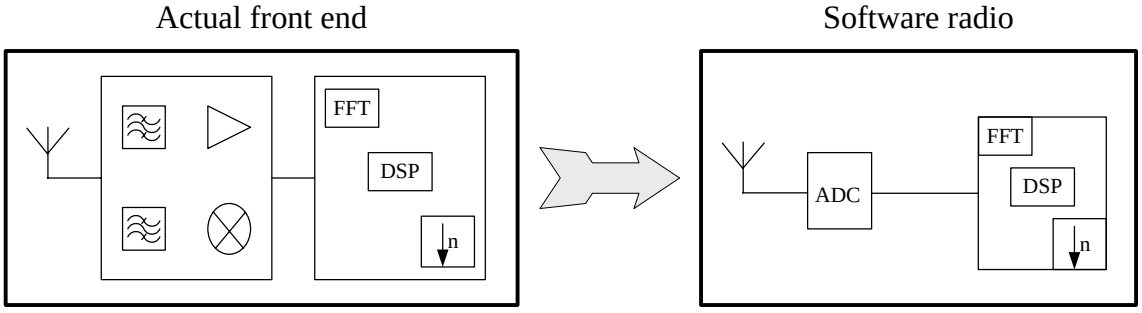


Figure 1.17: The SDRT principle

For instance, Figure 1.18 presents a 60GHz SDRT. It is fabricated with 130nm CMOS technology from TSMC [35]. The innovation in this transceiver is that a six-port receiver replaces the analog part. Implementing the six-ports in the receiver requires a low LO power compared to the required one for a typical mixer. Each amplifier used in the receiver and in the transmitter provides a high gain of 20dB to improve the link budget. The transceiver has been tested with a BPSK modulation scheme achieving a data rate of 4GBps.

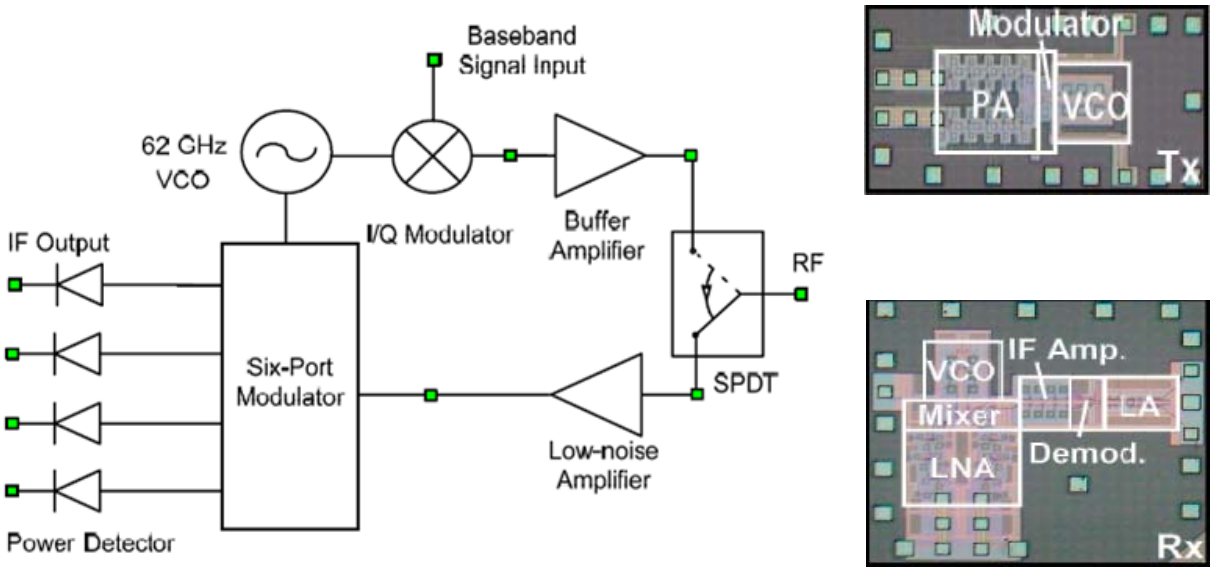


Figure 1.18: Chip micrograph of the 60GHz six-port transceiver based on SDRT

Table. 1.4 shows the FoM of the main elementary circuits of the presented transceiver examples. The SHT exhibits good link budget achieving a high data rate. However, it suffers from high power consumption and a large die area due to the separated design of the TX/RX parts.

DCT consumes the same power as the SHT. It is justified by the high output power generated by the PA. Despite of that, it does not achieve a better data rate than the SHT.

SDRT presents an innovative architecture. It benefits from a small area because of the use of the six-port receiver. But its power performances are lower than the previous transmitters ones even with the use of a simple BPSK modulation scheme.

In every cases, the antenna is not implemented in the same chip. It uses other low loss substrate such as FR4. Indeed, antenna on silicon suffers from very loss efficiency (lower than 15%). In this context, most of transceivers adopts SiP packaging with Printed Circuit Board-Monolithic Microwave Integrated Circuit (PCB-MMIC) chip interface [36] [37] or with Low Temperature Co-fired Ceramic-MMIC (LTCC-MMIC) chip interface [38] [39].

Table 1.4: Measured performances summary of SHT, DCT and SDRT

Topology	**SHT**	**DCT**	**SDRT**
Frequency(GHz)	57 to 65	59.6 to 64	60 to 64
Technology(nm)	90	90	130
Amplification			
PA			
Psat (dBm)	8.4	10.6	-
P1dB (dBm)	5.1	9	-2
Gain (dB)	17	14	20
LNA			
Gain (dB)	32	-	20
Sensitivity			
Noise figure (dB)	8	-	8
Phase Noise (1MHz)(dBc/Hz)	-95	-95	-92
Power consumption (mW)			
PA	54	-	36.9
LNA/Mixer/IF Amplifier	70	-	31
VCO+PLL	30+30	12+18	30
IQ Modulator/Demodulator/QVCO/PLL	36+42+40	-	
Base band	-	12	-
Total power consumption (mW)	362	369	-
Link Budget			
Modulation schemes	QPSK	QPSK	BPSK
Data rate (Gbps)	7	4	4
Die area (TX+RX) (mm^2)	$2.62 + 3.82$	6.87	2.47

1.2 60GHz WPAN PA design issues

1.2.1 PA fundamentals

The PA design is said to be complex because of the simultaneous consideration of criteria that characterize the PA performances. PA FoM is given by saturated power (P_{sat}), linearity, efficiency, frequency response, gain, stability and die area. All those parameters govern the design during every steps. Indeed, the PA is one of the most critical element in a RF front-end design. In one hand, it is the most current hungry component in the chip. In the other hand, it can be considered as a non-linearity source. Typical parameters used in this work are given by Figure 1.19:

- P_{in} and P_{out} are the input and the output power.
- Z_{in} and Z_{out} are the input and the output impedances of the PA.
- Z_s is the source impedance of the generator (typically 50Ω).
- Z_L is the load impedance of the PA.

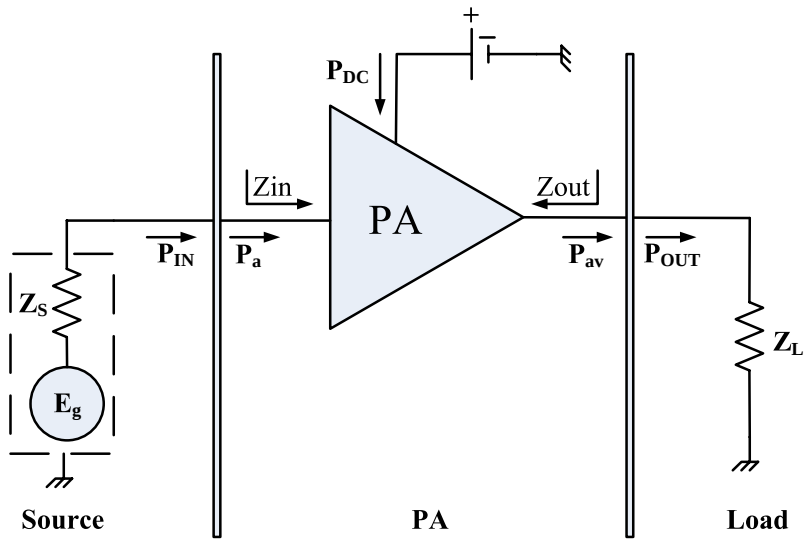


Figure 1.19: Characteristic parameters of a PA

Gain: Several reflections are present due to mismatching problems while the signal passes through the PA from the generator to the load. This phenomenon has power gain penalties and leads to different gain definitions: the operating gain (G_{op}), the available gain (G_{av}) and the transducer gain (G_{tr}). Their respective expressions are given in Eq. 1.2, Eq. 1.3 and Eq. 1.4.

$$G_{op} = P_{out}/P_a \tag{1.2}$$

$$G_{av} = P_{av}/P_{in} \tag{1.3}$$

$$G_{tr} = P_{out}/P_{in} \tag{1.4}$$

Where P_a is the accepted input power and P_{av} is the available output power.

The transducer gain is the most realistic one since it is the one measured considering every mismatching effects. Others gain definitions based on S-parameters are used in small signal domain to analyze gain and stability issues. Those aspects will be detailed in the transistor characterization.

Efficiency: The power consumption of the PA must be optimized as much as possible to guarantee a long battery life. This is why the efficiency is one of the most important FoM in a PA design. The efficiency considers directly the DC power consumption (P_{DC}) and the portion of the alternative signal when the current is flowing through the transistor. Two definitions are set: the drain efficiency (η_d) (Eq. 1.5) and the Power Added Efficiency (PAE) (Eq. 1.6).

$$\eta_d = P_{out}/P_{DC} \tag{1.5}$$

$$PAE = (P_{out} - P_{in})/P_{DC} \tag{1.6}$$

η_d is frequently used for high-gain GaAs and Bi-CMOS PAs and is also used for a single PA stage. In the context of 60GHz CMOS PA, the gain is expected to be low and P_{in} can not be neglected. Thus, the PAE will be the FoM of efficiency since it considers all input powers and the gain.

The principles of transistor matching, stability and modeling for PAs applications will be detailed in chapter 3. The next part highlights the issues in PA design related to the 60GHz WPAN standard with a 65nm CMOS technology.

1.2.2 Modulation issues

The PA characterization differs from and depends on the nature of the signal applied to the input of the PA. A complete PA design takes into account the impact of the modulated signal. Two cases are distinguished:

- Constant envelope signal.
- Non-constant envelope signal.

Constant envelope signal

The first step in the PA design consists in applying a source swept in power. P_{out} versus P_{in} is the most frequent power characteristic. Two operating modes are distinguished (Figure 1.20):

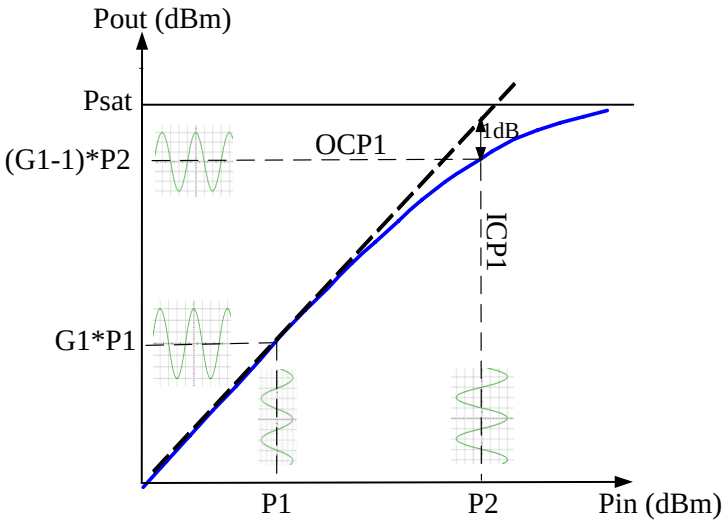


Figure 1.20: P_{out} versus P_{in} with a SW signal

- A linear regime is defined when the output signal is intended to be the same than the input signal and amplified to the desired level.
- A non linear regime is defined when the gain decreases. The Output 1dB Compression Point (OCP_1) is defined when the gain falls by 1dB. The PA operates in a non linear regime from this point.

Only magnitude and phase distortions due to multiple harmonics are analyzed with a sine wave analysis. That characterization does not bring enough information concerning linearity to be as accurate as required for broadband signal.

Non-constant envelope signal

Advanced standards use non constant envelope signal by choosing a multi-carrier approach to improve data rate. In this context the instantaneous P_{in} applied to the PA varies in time. Two parameters are defined from the modulated signal to set the linearity constraints: Power Average To Power Ratio ($PAPR$) and Output Back-Off (OBO).

*$PAPR$***:**

Contrary to a SW signal, the OFDM signal is a result of the coherent sum of several carriers varying in time (Eq. 1.7). Hence, the OFDM signal has a non constant envelope. In order to quantify the envelope fluctuations, the $PAPR$ is defined as the ratio between the peak power (P_{Peak}) and the average power (P_{Av}) of the signal during an interval of time (Eq. 1.8) (Figure 1.21). It differs from a standard to an other.

$$S(t) = A \sum_{k=-\infty}^{\infty} \sum_{i=0}^{N-1} x_{\mathrm{i,k}} \cdot w(t - kT) \cdot e^{j2i\pi\Delta f(t-kT)} \tag{1.7}$$

Where:

- $w(t - kT)$ is the window function,
- N is the number of channels,
- x is the symbol of sub-carrier i at time k,
- Δf is the distance separating two carriers,
- A is the magnitude of a digit.

Table. 2.1 shows the most common signals used for wireless communication with their respective $PAPR$. OFDM signals have the highest $PAPR$.

Table 1.5: PAPR for different modulated signals

Signal	$PAPR$ (dB)
GSM	0
CDMA	$5 - 9$
WCDMA	$3.5 - 6$
OFDM	$10 - 17$

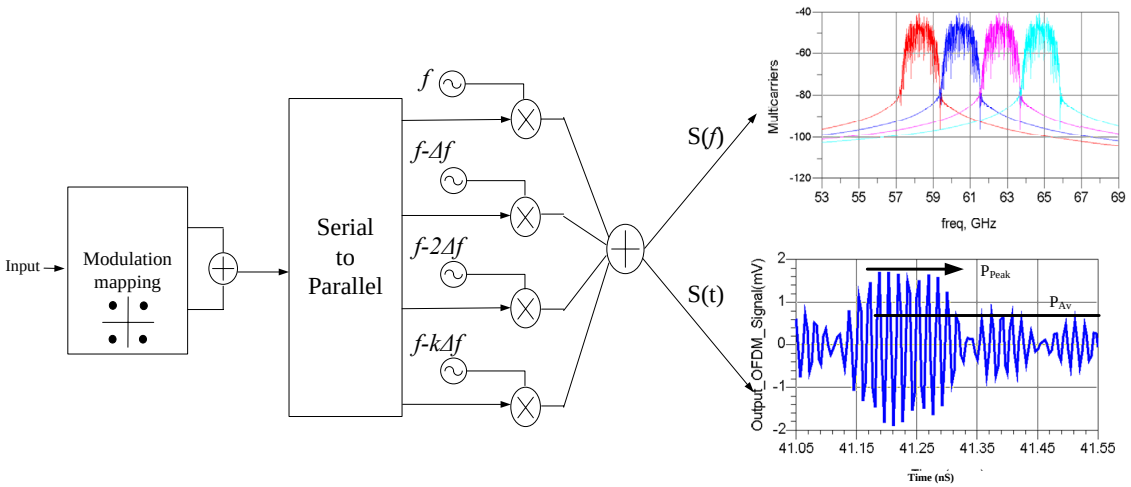


Figure 1.21: OFDM signal generation

The OFDM signal is described statistically by a Complementary Cumulative Distribution Function ($CCDF$) that determines the probability that the magnitude crosses a certain threshold [40]. Typically, the peak power is reached infrequently (Figure 1.21). The probability that the magnitude crosses 90% of the peak of the signal is around 5%. In spite of the few presence of high power level in time, the PA must be at least linear when the highest level of power is applied to keep the PA linear.

$$PAPR = \frac{P_{max}}{P_{av}} = \frac{max_{[0,T]}|S(t)|^2}{\frac{1}{T}\int_0^T \cdot |S(t)|^2.dt} \tag{1.8}$$

OBO:

It is defined as the ratio between P_{sat} of the PA and the Average Output Power (P_{outAV}). Furthermore, the Peak Back-Off (PBO) is used to set the difference between P_{sat} and the peak instantaneous output power for a given standard. Therefore, the PA operates with some OBO in order to obtain desired linearity. It can be noticed that PA respects the standard requirements if it behaves linearly at the maximum output power. Figure 1.22 illustrates the $PAPR$ and the OBO in a PA transfer characteristic with a non constant envelope excitation.

$$OBO(dB) = 10 \cdot \log(\frac{P_{sat}}{P_{Av}}) \tag{1.9}$$

$$PBO(dB) = OBO(dB) - PAPR(dB) \tag{1.10}$$

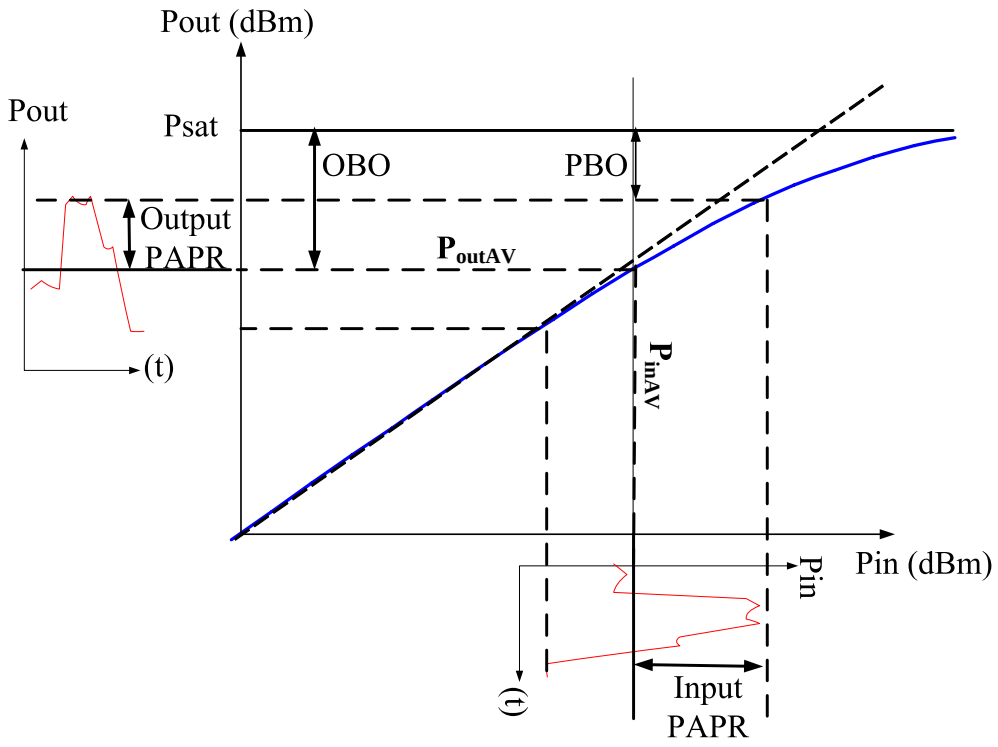


Figure 1.22: P_{out} versus P_{in} with a modulated signal

The link between the $PAPR$, OBO and linearity is direct. For a high $PAPR$, a large OBO is required to ensure good linearity but the PA operates inefficiently in this case. The linearity-efficiency trade-off is pointed out here. OFDM modulation scheme is adopted for 60GHz WPAN standard. Consequently, the linearity FoM is the major interest in our PA design. It is analyzed in the useful band by calculating the Error Vector Magnitude (EVM) and at the neighbor band by calculating the Adjacent Channel Power Ratio ($ACPR$) (Figure 1.23).

EVM is defined as the distance between the desired and actual signal vectors by projecting the received symbols in I/Q plan constellation. This FoM depends strongly on the adopted digital modulation. It sets the maximum data rate at a given Bit Error Rate (BER) for a wireless communications.

$$EVM_{RMS} = \sqrt{\frac{\frac{1}{N}\cdot\sum_{k=1}^{n}|S_{Ideal,k}-S_{Simulated,k}|^2}{\frac{1}{N}\cdot\sum_{k=1}^{n}|S_{Ideal,k}|^2}} \tag{1.11}$$

$ACLR$ is an important linearity criterion in the neighbor bands. As illustrated in (Figure 1.23), in addition to the amplified power $(P(f))$ in the useful bans (B_0), the PA non-linearities generate spectral side lobes in the neighbor channels (B_1) and (B_2) defined by a frequency offset (f_0). A transmitter that fulfills the specifications must not disturb neighbor channels used by other transmitters. High $ACPR$ creates interference issues with neighbor standards. If it is impossible to reduce the side lobes power, the designer must take care by designing additional filter to eliminate those non-linearities.

$$ACLR = \frac{2\int_{B_0}|P(f)|df}{(\int_{B_1}|P(f)|df) + (\int_{B_2}|P(f)|df)} \tag{1.12}$$

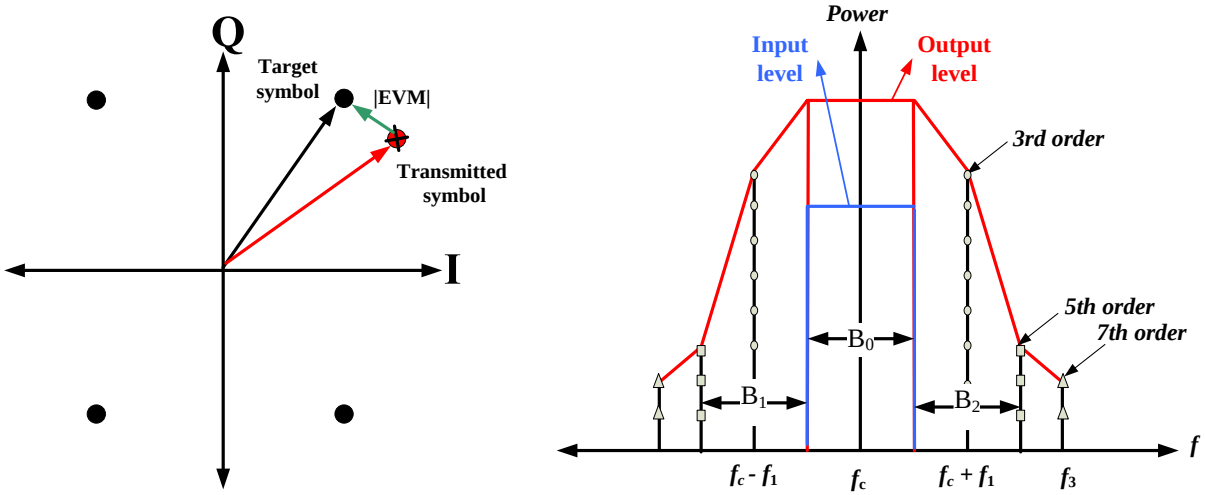


Figure 1.23: System linearity FoM of a communication system

1.2.3 Scaling technology issues

The 65nm CMOS technology should benefit from scaling. In fact, the reduction of the gate length improves frequency and gain performances of the transistor. However, there is a trade-off between the transistor power gain and its stability due to the bad voltage-gate control of the transistor channel. Moreover, the technology downsizing is very aggressive for PA design. Indeed, the reduction of the breakdown voltage sets a lower maximum voltage supply since the drain voltage can reach twice the voltage supply. It leads to drive high current density in the circuit to reach high P_{out}. Hence, an important dissipated power is responsible for a low PAE. Those aspects will be detailed in PA design description.

An other challenge concerns the use of emerging digital technology for analog applications. The non-idealities must not be neglected in physical core and model architecture of the transistor. For instance, the transistor model used for a 130nm CMOS technology is BSIM3 [41]. It considers the geometrical parameters and the physical dimensions. Figure 1.24 lists the main features of the BSIM3v3 model.

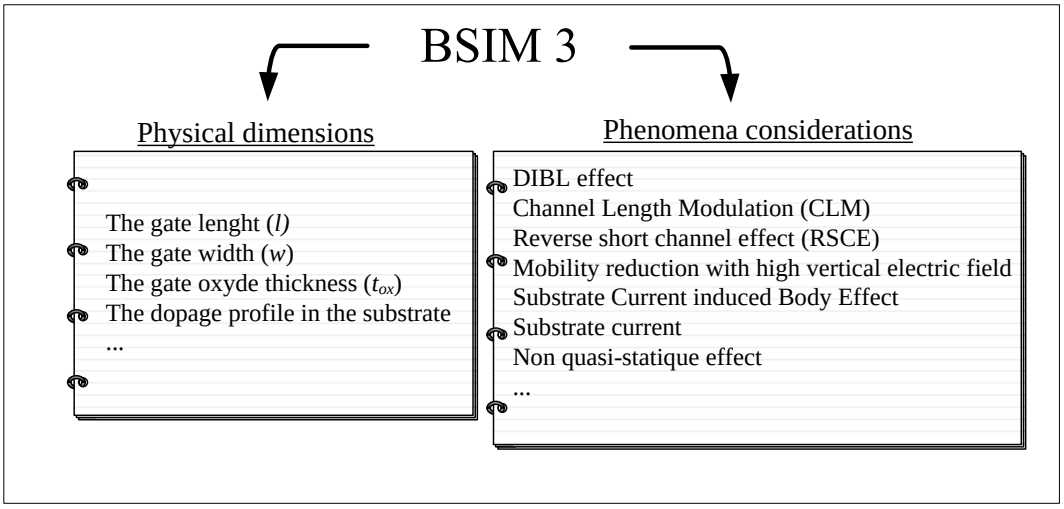


Figure 1.24: BSIM3 model considerations

Although, the transistor model has some drawbacks when *mmW* applications are targeted. Indeed, the gate resistance and the resistive losses in the substrate are not well modeled. Consequently, the gain and noise figure of the transistor are overestimated. Several high quality models like BSIM4 [42], SP2000 [43], HiSIM [44], EKV [45], ACM [46] and USIMP [47] models have emerged to meet the requirements of advanced Sub-100nm process [48].

The 65nm CMOS RF transistors provided by STMicroelectronics are based on BSIM4.6.0 MOSFET Model as an extension of BSIM3 model. The major modeling improvements that concern a PA design are:

- An accurate new model of the intrinsic input resistance,
- Flexible substrate resistance network for RF modeling,
- A versatile geometry dependent parasitic model for various source/drain and multi-finger connections,
- A new temperature model.

For the passive devices, the issues are directly related to the dimensions of the Back-End Of Line (BEOL). As said before, the technology associated to this work is the 65nm CMOS bulk technology ($\rho = 10\Omega.cm$). This technology has a thin BEOL and is under $5\mu m$ with thin metalization levels compared with Bi-CMOS BEOL (Figure 1.25). Those characteristic parameters influence directly the passives performances by:

- An emphasis of the electro-migration problem.
- An increase of the capacitive and resistive losses.
- A decrease of the quality factor of passives.
- High substrate losses due to its proximity to RF signals.

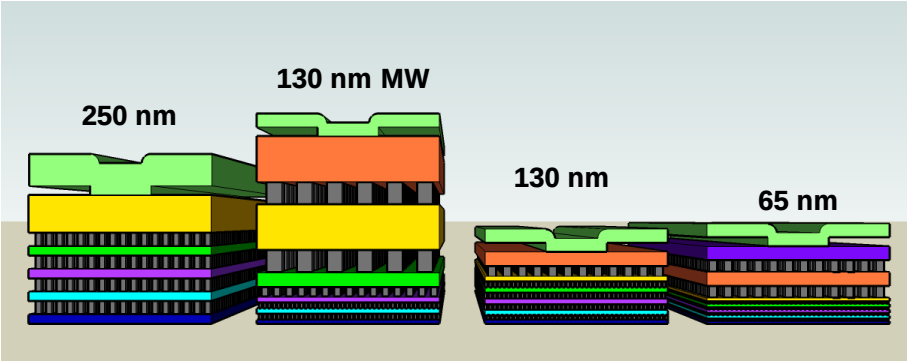


Figure 1.25: BEOL of different silicon technologies

1.2.4 High frequency issues

Active and passive devices need extensive modeling at high frequencies. Generally, empirical and physical data are combined to make compact models. The active devices do not behave similarly in small signal domain and large signal domain. This is due to the non-linearity of the intrinsic parameters as the capacitance junctions, the RF resistances, etc.

The major issue at high frequencies is the low resistivity of the Si substrate. The losses in the substrate are important and lead to adopt new design techniques. Moreover, the metallic losses increase proportionally with the frequency due to the skin depth effect. The PA response is penalized in gain and linearity with the parasitic considerations. Also, a shift in frequency is observed in such investigation. This is why an accurate modeling is mandatory to predict accurately the performances. The use of Electro-Magnetic (EM) simulator is a good way to consider parasitics. Chapter 2 details passive and active 65nm CMOS device modeling.

1.3 60GHz CMOS technology PA

Historically, PA were initially designed with III-V technologies after the availability of the 60GHz band. Indeed the first transceiver was fabricated with GaAs technology and demonstrated by NEC in 2001 [22]. In parallel, because of the continued scaling in the SiGe hetero-junction bipolar transistor, this technology achieves high f_t and high operating voltage. In addition, it has a high BEOL which helps to reduce the dissipated power and leads to obtain both high gain and high output power (P_{out}). IBM has investigated this application with the 130nm BiCMOS technology and demonstrated a transceiver in 2004 [24].

Contrary to III-V technologies, CMOS technology was not dedicated to PA design and let-alone used for mmW applications. This idea is changing over the time with the fast improvement of this technology. Indeed, few realizations have been demonstrated in literature [49] [50]. Figure 1.26 shows the design progress during the past few years at 60GHz, illustrating the topology of adopted design. Until 2009, 130nm and 90nm CMOS technologies were widely exploited [51] [52] [53] [54]. The 65nm CMOS PAs have been investigated since 2009 [55].

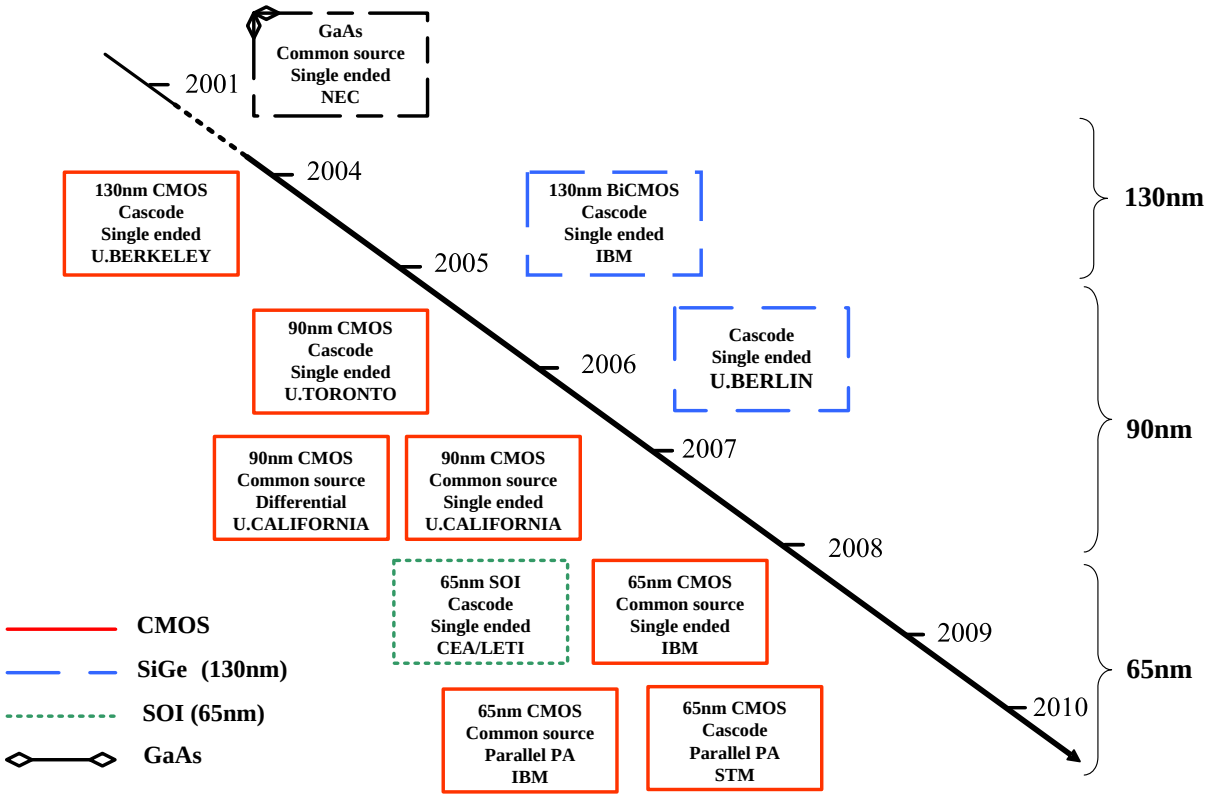


Figure 1.26: 60GHz PA realizations in time

1.3.1 State of the art

This thesis work is focused on PA design using CMOS technology and operating at 60GHz. The design trend of PAs is justified in function of the power requirements and the technology imposed in the design. Several means can be driven and an exhaustive state of the art is exhibited. The methodology is highlighted as follows:

- **A single structure with distributed T-lines**
  The first PA to operate at 60GHz was fabricated with a 130nm CMOS technology [56]. Figure 1.27 shows the schematic and the die photography of the PA. Applying a $0.1\mu A/\mu m$ current density leads to (f_t, f_{max}) around (70, 100)GHz. The targeted 60GHz band is close to f_t and f_{max}. Hence, the power gain is expected to be poor (lower than 8dB). That is why the PA is composed by three cascaded stages designed with a CA topology. The CA topology is preferred to achieve higher gain and to improve the isolation between the input gate and the output drain of the CA transistor.

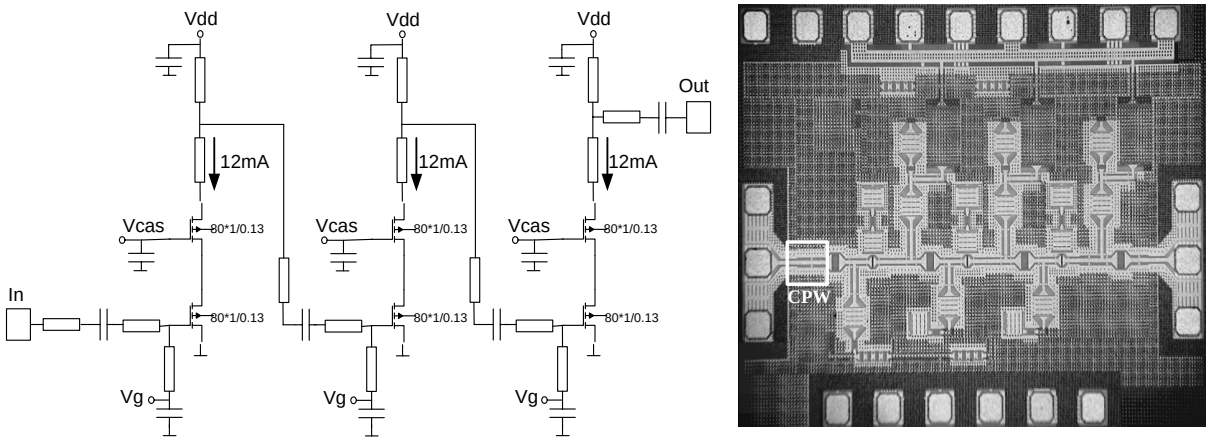
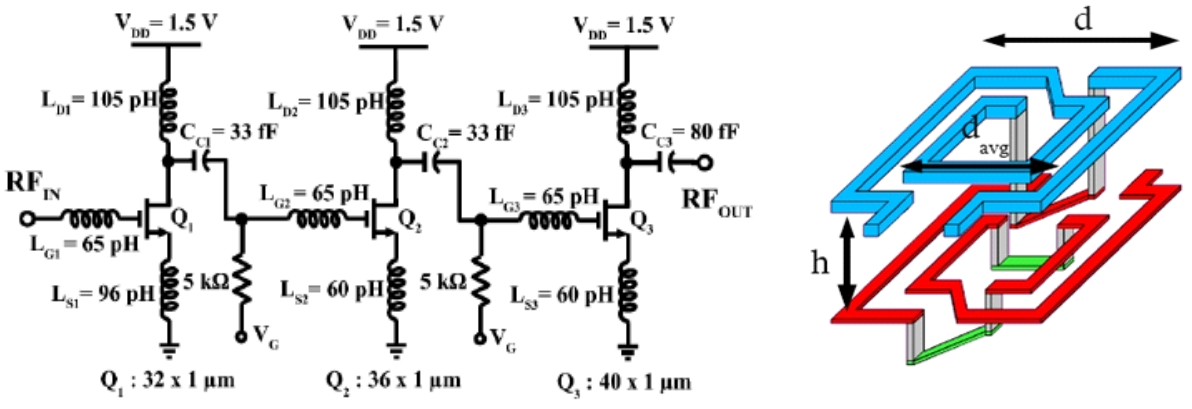


Figure 1.27: 60GHz PA in 130nm based on T-lines

The PA achieves a peak power gain of 12dB. A large 3dB bandwidth from 51GHz to 65GHz is demonstrated due to the use of distributed elements based on Co-Planar Waveguide (CPW) T-lines. It can be noticed that there is no classical active bias circuit based on current mirror. The biasing is only performed with T-lines. This technique is feasible because of the wavelength scaled at mmW frequencies. However, this PA suffers from a low OCP_1 of 2.0dBm since the low voltage excursion in CA structure. In addition, it is impossible to keep high linearity with a 12mA current driving in the power stage. This first realization has widely contributed to further PA designs.

- **A single structure with lumped inductor**

  This PA uses ring lumped 3D inductors for matching instead of T-lines [57]. The PA is a three Common Source (CS) stages fabricated with a 90nm CMOS technology (Figure 1.28). In spite of CA advantageous, the CS configuration is more suited for linearity. The first stage is biased at $0.2mA/\mu m$ current density to maximize f_t and hence to maximize the gain. The second and the power stages are biased at $0.28\text{mA}/\mu m$ to operate in class A to optimize the linearity. Moreover, inductive source degeneration is added to prevent the gate-source junction from becoming non-linear. This inductor drops the PA gain to 5.2dB. The use of a smaller $40\mu m$ transistor compared to the $90\mu m$ transistor used in [56], enables the PA achieving a P_{sat} of 9.3dBm with a good linearity. Indeed, OCP_1 is equal to 5.2dB with a PAE of 7%. The use of optimized lumped inductors offers higher quality factor and smaller size than T-lines but increases the risk of coupling with neighbor components. Hence, the effect of EM coupling must be considered.



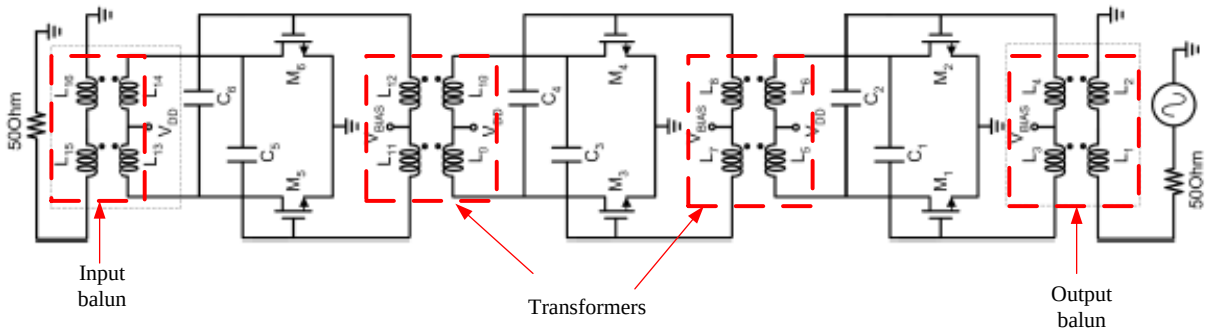
(a) Schematic of the PA

(b) 3D lumped inductor

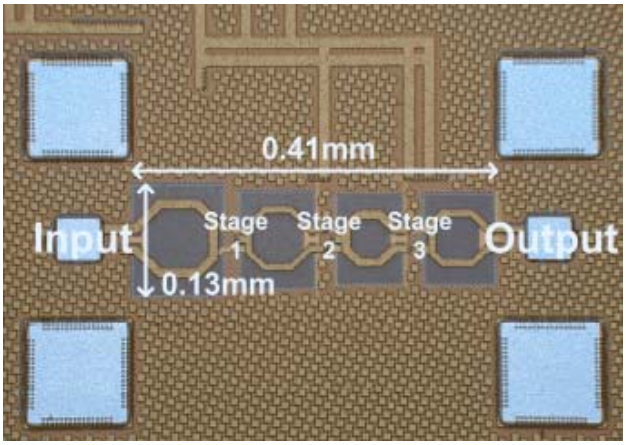
Figure 1.28: 60GHz PA in 130nm based on 3D lumped inductors

- **A differential PA using baluns and transformers**

  Contrary to previous PAs, a differential PA is realized to obtain high P_{out} [58] (Figure 1.29). It is fabricated with a 65nm CMOS process from IBM. Each half-PA operates in phase opposition thanks to input balun which is responsible for the single-to-differential mode conversion. The interstage matching is ensured by transformers that preserve also the balanced mode. An output balun is required to return to single mode for Single-Ground-Signal (SGS) probing. The input and the output baluns perform the input and the output matching by adding a parallel capacitor. It can be noticed that the use of baluns and transformers lifts the need of coupling capacitors. This PA achieves a P_{sat} of 11.5dBm



(a) Schematic of the PA



(b) Die photograph of of the PA

Figure 1.29: 60GHz PA in 65nm based on baluns

and a good PAE of 11% but suffers from low OCP_1 under 3dBm. This low linearity is probably the consequence of a bad single-to-differential mode conversion. The unbalanced to balanced mode conversion is the major FoM of balun in addition to its own insertion losses as listed here:

- If an important amplitude imbalance is observed between the two differential stages, the first half stage operates in the compression region while the second half stage remains in the linear region, degrading the PA linearity.
- If the balun has an important phase imbalance, the total signal is distorted at the output.
- In both cases, a penalty in linearity is observed if the balun is not well optimized.

- **A parallel PA**

  Previous PAs have an output linear power level under 10dBm. The main obstacle in modern deep submicron CMOS process is the low breakdown voltage. Indeed, with a low breakdown voltage technology, it is mandatory to drive a high current at the expense of a low PAE to obtain high power. Hence, power and efficiency trade-off is limited in a single PA configuration. Consequently, other circuit topologies and system architectures are required to overcome the linearity challenge. Thus, designing PA in parallel is a good alternative. The difficulty is to optimize the power path that divides and combines power while taking care to linearity and stability issues.

  Two means are distinguished to spread the power in multiple PAs: combining the voltage or combining the current. Figure 1.30 exhibits the principle of each method. An example of 60GHz PA realization is detailed for each case:

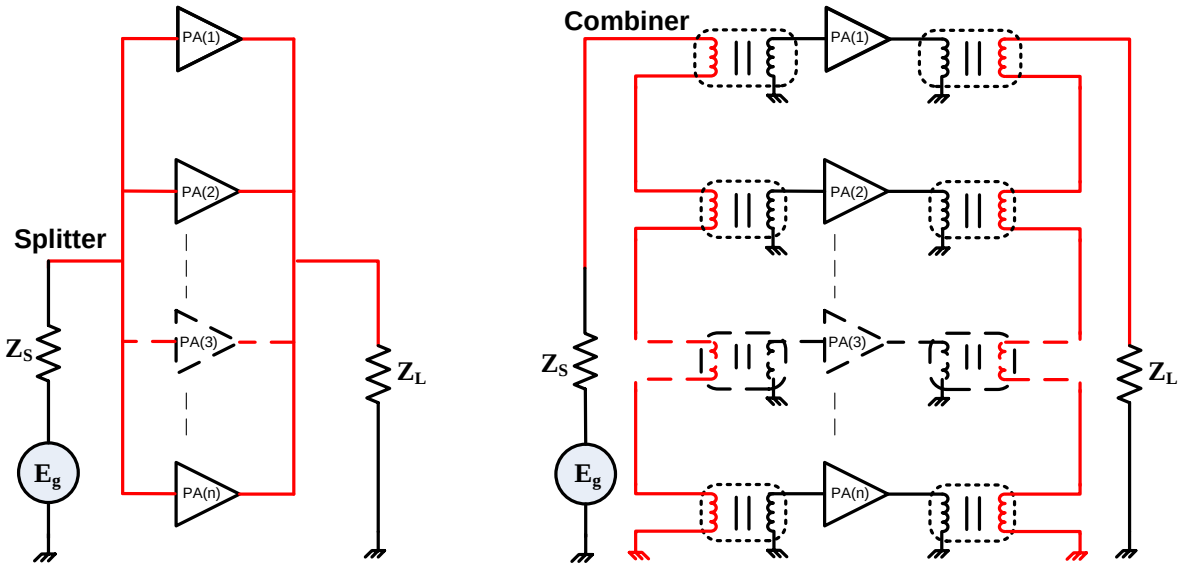


Figure 1.30: PA in parallel topologies

Current Combining:

The power splitter and combiners must preserve the signal phase at the combining node. With this electric configuration, the voltage is set and is equal for each elementary PA. A high current is summed at the node introducing insertion loss. Based on the Wilkinson structure, various splitters are demonstrated in literature. This topology has pro and cons:

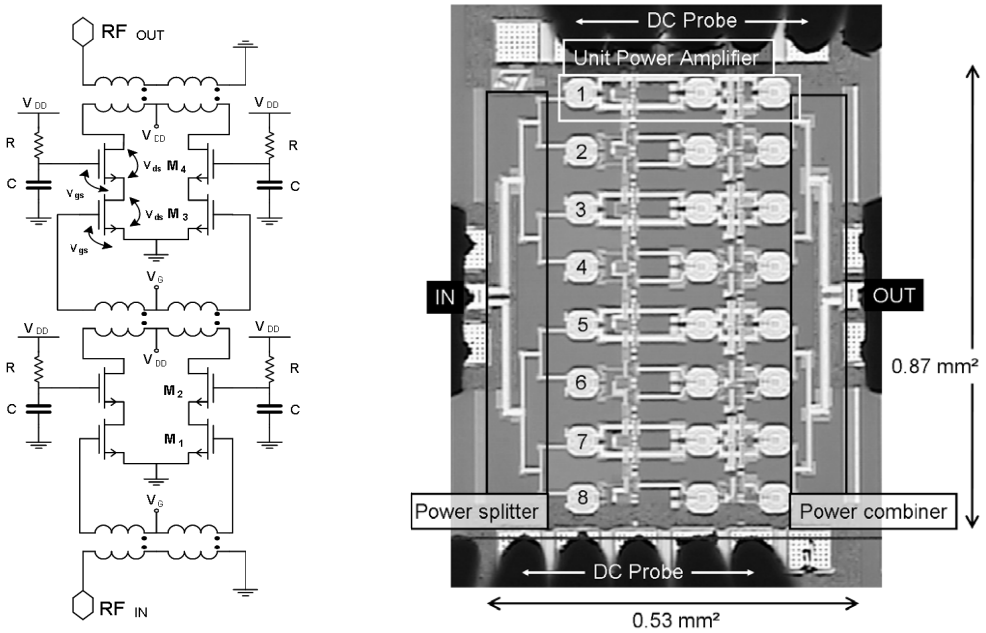
– Pro :

  * There is no risk to reach high voltage excursion. It ensures good reliability.

– Cons :

  * This method is based on current summation. Consequently, a high loss matching is mandatory to ensure the impedance transformation from high impedance to 50Ω at the input or at the output of the circuit.
  * The structure is set for only one operating mode. Indeed, turning-off one elementary PA to improve the efficiency affects drastically the matching and drops considerably the gain.

For instance, a PA with 8 differential power-combined ways and CA topology in a 7-metal-layer 65nm CMOS process is presented in [59]. Figure 1.31 shows a simplified schematic of one unit PA and the chip micrograph and its power performances. The 8 PAs are connected together with a zero-degree power splitter/combiner at the input/output. This solution is chosen instead of Wilkinson or hybrid combiners that require quarter-wave T-lines causing a large area. The splitter is based on microstrip T-lines and exhibits only 1dB of insertion loss.



(a) Simplified schematic of the 2-stages unit PA

(b) Chip micrograph of the PA.

Figure 1.31: Chip micrography of a current combining PA

The presented circuit operates at a voltage supply of 1.2V or 1.8V and achieves a P_{sat} of 16.6dBm and 18.1dBm respectively. The 3dB bandwidth of the PA covers a 53GHz to 68GHz frequency band. The PA has a modest PAE under 5%.

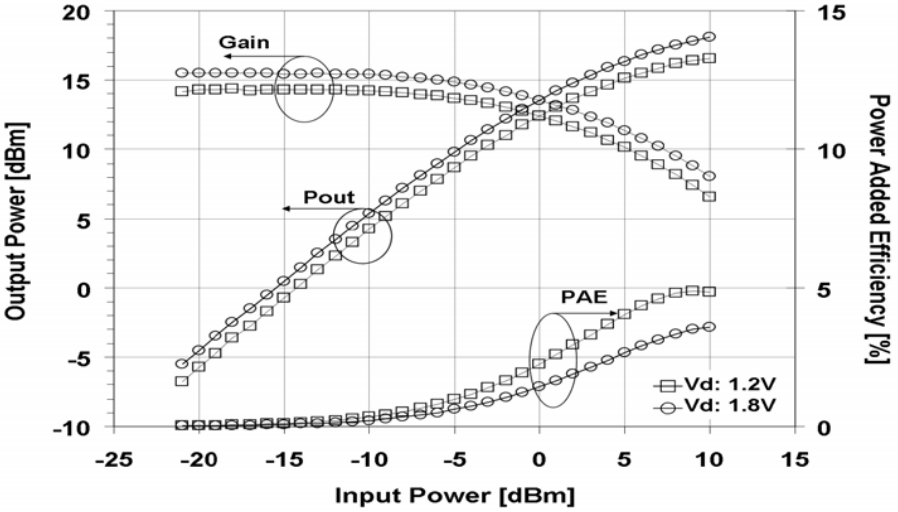


Figure 1.32: 60GHz PA measured large signal parameters

Voltage Combining:

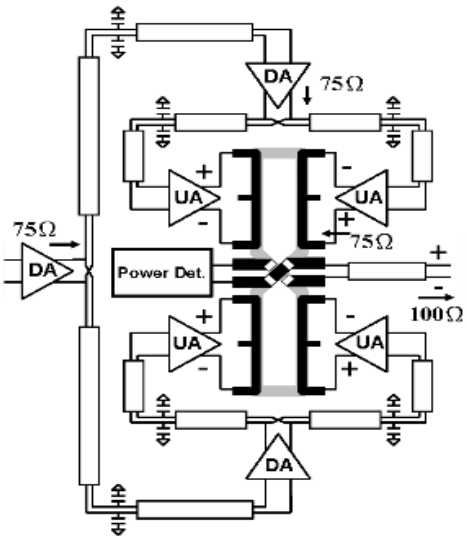
The voltage combining is performed by a Distributed Active Transformer (DAT). The first one is integrated in a PA circuit for cellular phone applications presented in [60]. The DAT topology provides high efficiency power combining and impedance transformation at the same time. The DAT is composed by several primaries (one for each PA) and one secondary. The primaries of the DAT are driven with a low voltage supply applied for each elementary PA. The secondary is driven by a high voltage equals to the sum of all elementary PA voltage swings. Pro and cons of this method are :

- Pro :
  - The DC current is provided through virtual grounds. Hence, The PA becomes insensitive to the bias network.
  - Each PA works independently. If one PA is turned off to operate in low power mode, Z_{out} is lightly affected.
  - The secondary does not drive a DC current. Consequently, the secondary does not care for electro-migration phenomenon and the power dissipation is reduced.

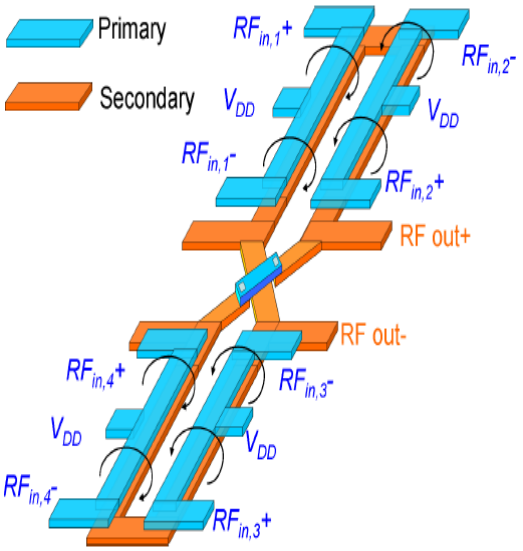
– Cons :

∗ The secondary of the DAT has a long path. It has a high inductor with a low resonance frequency. In addition, metallic and substrate losses are important.

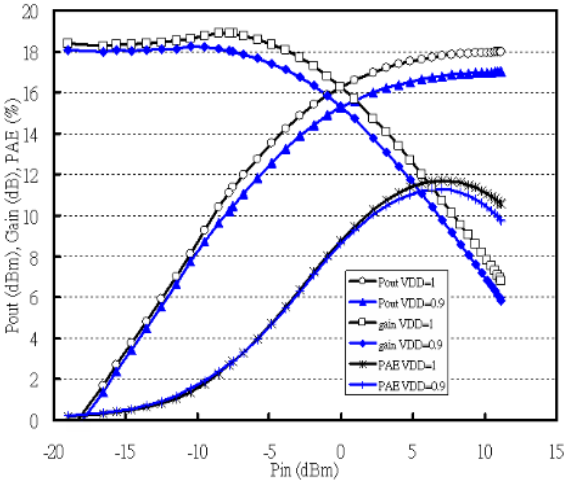
A 65nm 60GHz PA composed by 4 identical elementary PAs designed with CS structure is presented in [61]. The PA prototype is fabricated with a 1V 65nm CMOS-10 metals process with 10 Cu-metal levels provided by IBM. At the output, a transformer-based serial power-combining technique is used. The structure of the combiner is optimized by



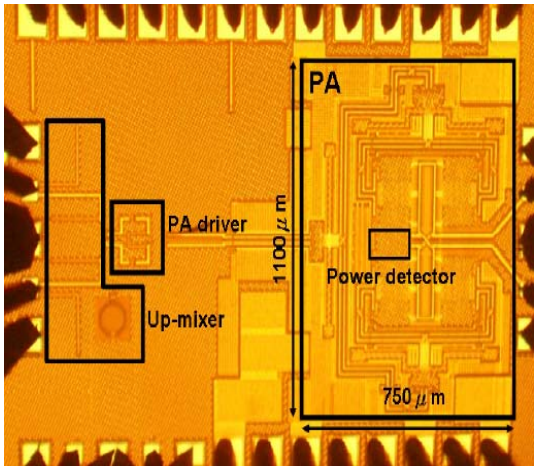
(a) Circuit schematics of the proposed power-combining PA



(b) 3D view of the mm-Wave transformer power combiner



(c) Measured power performances of the PA at 61.5GHz



(d) Chip photo of the transmitter front-end circuit.

Figure 1.33: Building bloc of a power-combining PA based on mmW transformer power combiner

analyzing its polarity. In fact, the negative coupling lower the quality factor of the DAT in typical compact square combiner. The metal stripes of primary and secondary windings are overlapped to constitute transformer. The DAT presents only 1dB of losses. It achieves a P_{sat} of 17.9dBm and an OCP_1 of 13dBm. The peak PAE at 1V VDD is 11.7%. The PA die photography and the DAT layout with its electric polarity are depicted in Figure 1.33.

Table 1.6: Comparison of PAs dedicated to 60GHz WPAN standard

[Ref] Tech Node[nm]	Design	Gain (dB)	P_{sat} (dBm)	PAE (%)	OCP_1 (dBm)	BW_{3dB} (GHz)	consumption mA@Volt	size mm^2
[56] CMOS 130nm	3*CA T-Lines	12	NC	NC	2	25	38@1.5	2.3
[57] CMOS 90nm	3*CS Inductor	5.2	NC	7	6.4	13	36@1.5	0.15
[62] CMOS 90nm	2*CS T-Lines	8	NC	20	6.7	6	21@1.2	NC
[54] CMOS 90nm	3*CS Differential	4.5	12.5	19.3	10.2	5	70@1.2	0.15[1]
[63] CMOS 90nm	2*CS C. Combiner	4.2	14.2	5.8	12.1	12	145@1	1.2
[55] CMOS 65nm	1*CS T-Lines	4.5	8.5	8.5	6	9	23@1	0.27
[58] CMOS 65nm	3*CS Differential	15.8	11.5	11	2.5	NC	43@1	0.05[1]
[59] CMOS 65nm	2*CA C. Combiner	14.3	16.6	4.9	11	15	NC@1.2	0.462[1]
[61] CMOS 65nm	2*CS DAT	19.2	17.7	11	15.1	6	NC@1	0.825[1]
[64] SOI 65nm	2*CS T-Lines	14.2	10.3	22.3	7.2	NC	21@1	0.57
[65] SiGe 250nm	2*CS DAT	18.8	15.5	19.7	14.5	5	NC	NC
[66] SiGe 130nm	2*CA T-Lines	18	23	6.4	13	NC	300@4	NC

1.3.2 Conclusion

Table 1.6 exhibits performances of PA realizations dedicated to 60GHz WPAN standard. Different technologies are adopted :

- With a 130nm BiCMOS technology [66] [65], active device achieves higher f_t and f_{max} thanks to the hetero-junction SiGe. In addition, passive devices benefit of good quality factor thanks to a thick BEOL and a thick metalization level. Those reasons lead to obtain the best performances in terms of linearity and P_{out}.

- With a CMOS SOI technology [64], transistors keep the same RF performances as the ones in a CMOS on bulk technology. The fundamental advantage of CMOS SOI technology is a high resistivity substrate. This substrate behaves almost like an GaAs substrate. It reduces the coupling with the RF signal and increases the quality factor of passives. This technology was dedicated to design low power active devices as switches and LNA because of its low thermal evacuation. This is not anymore a constraint because of the low P_{out} required in the WPAN standard. A world record with 22% of PAE is held in [64]. The linearity and power issues still face to the same challenges as CMOS on bulk technology.

- With a CMOS on bulk [56] [45] [62] [54] [55] [58], single-ended and differential structures are demonstrated using distributed T-lines or lumped elements for passive device. The challenge of providing higher output linear power is critical. Indeed, the maximum OCP_1 equals to 10dBm is achieved at the expense of very low gain. Gain-linearity, linearity-efficiency are limited trade-offs with a single structure. Therefore, other techniques are required to improve the power performances. In [63] [59] [61], multiple PAs in parallel are designed using a current or a voltage combining. With this technique, PAs exhibit high linearity at the cost of insertion losses of the power divider/combiner reducing the PAE.

[1] Without pads

1.4 Thesis contribution

chapter 1 introduces the 60GHz WPAN context. Up to now, no proven technical alternatives achieving a gigabit data rate to ensure wireless uncompressed high-definition video streaming and kiosk-downloading were demonstrated. This is why a particular interest is focused on a free 7GHz around the [56-64]GHz band. The use of OFDM modulation schemes constraints PA linearity FoM. WPAN applications target a large scale market. Consequently, a low cost CMOS technology is adopted.

Downsizing CMOS technology enables implementing 60GHz CMOS transceivers. According to the PA state of the art, the PA design is still a challenge because of :

- The reduction of breakdown voltage drives strong current to obtain high P_{out}. It leads to high dissipated power and thus a poor gain and PAE.
- The thin 65nm CMOS technology BEOL increases inductive, resistive and capacitive parasitics.
- The low resistivity of the Si substrate lowers the quality factor of passive devices. This is critical at high frequencies.
- The lack of knowledge on CMOS power behavior at high frequencies.

The thesis work aims at designing a 65nm PA operating at 60GHz for WPAN applications. Before designing the PA, active devices and passive such as MiM, MoM capacitors and inductors must be modeled and measured. chapter 2 details those components characterization to predict their behavioral simulation at 60GHz frequency range.

chapter 3 focuses on the PA design. A single PA must be optimized before investigating parallel PAs design. The design flow is described in each case. Measurements results are exhibited.

Chapter

2 Passive device optimization

Contents

Chapter 2 presents the early steps consisting in designing and optimizing passive devices before designing PA. The first part details mmW physical phenomena and approximations that must be taken into account to analyze passive devices during simulation and measurements procedures. The second part reviews the silicon monolithic components analysis describing their electrical behavior at RF and mmW frequencies. The impact of layout geometry and substrate are detailed to construe simulations and to predict measurements. Every component must be differently analyzed because of their different functions. Hence, the characterization of each element is presented separately namely T-line, inductors and RF pads.

Key words: Electromagnetic fields, T-lines, RF-pads and inductors.

2.1 Design flow process

The previous chapter overviews different 60GHz PAs realizations implemented in CMOS technology. Our work focuses in PA design with the 65nm CMOS technology provided by STMicroelectronics. Figure 2.1 illustrates the supported design flow process before designing PA.

At the beginning of our work, the 65nm CMOS Design Kit (DK) was immature. It provides a library of passive and active devices models that are only accurate in RF frequencies. Consequently, the primary purpose is to develop an improved DK library listing behavioral models and 60GHz functional components, before designing any PA.

The *mmW* physical phenomena must be defined and understood. In this context, the choice of the software is crucial. EM software can be customized to take into account those phenomena. Moreover, they allow analyzing electric and magnetic fields of a defined structure pointing out its critical areas. Consequently, RF component structures are exported from Cadence to be analyzed with EM tool at *mmW* frequencies. HFSS software is chosen because of its robustness in such investigations. The frequency domain data are collected to be simulated with parasitic considerations. However, those data are not readable for time domain simulation. Thus, DC and transient simulation results are not reliable. To solve this issue, two methods are followed:

- Transforming frequency data components into lumped models,
- Using software with a robust convolution solver to transform frequency domain data to time domain data. Nexxim and Golden gate calculators are suited for that operation.

The first solution is adopted because of the unavailability of suitable software. ADS software is used for device modeling. It has the advantage of possessing a matrix computation that handles the use of Z, Y and ABCD matrices. As the performances of passive devices are sensitive to any parasitic elements added in the layout, their structures are optimized by iteration. In most of time, an inaccurate modeling of passive devices is responsible for a frequency shift or for a gain drop in PA design. Consequently, this chapter discusses about the response of passive devices and their optimization to be functional at 60GHz. At the end of this work, an improved 65nm CMOS DK is available and can be simulated in both frequency and time domains. The relevant components are inductors and RF-pads. T-lines are not available in the 65nm CMOS DK. Hence, they are characterized and added to the improved DK. The next part details mmW physical phenomena that help for passive device modeling. They are considered during simulation and experimental steps.

2.1.1 High frequency considerations

As frequency increases, an AC current has a particular distribution when crossing over a metal. This distribution is more complex in the presence of two close metals. The most important effects are called the skin and proximity effects. They affect respectively the resistance and inductance values of a strip.

Skin depth:

When a current crosses over a conductor, its density at the surface is greater than the one at its core. This phenomenon called *skin depth* (δ) presents the most important parameter that causes metallic losses. Moreover, as the current is concentrated only around the surface of the conductor, the internal inductance decreases. δ is defined as the distance from the metal surface to the metal level over which the magnitude of the crossing current is reduced by $1/e \approx 37\%$ [67]. Figure 2.2 plots the variation of δ as a function of the frequency. It is calculated as follows:

$$\delta = \sqrt{\frac{\rho}{\pi \cdot \mu \cdot \sigma \cdot Freq}} \tag{2.1}$$

Where ρ is the resistivity expressed in $\Omega.m$ and μ is the permeability of the metal. With this frequency-dependent behavior, δ is equal to 8.5mm at 6GHz while it decreases to $0.29\mu m$ at

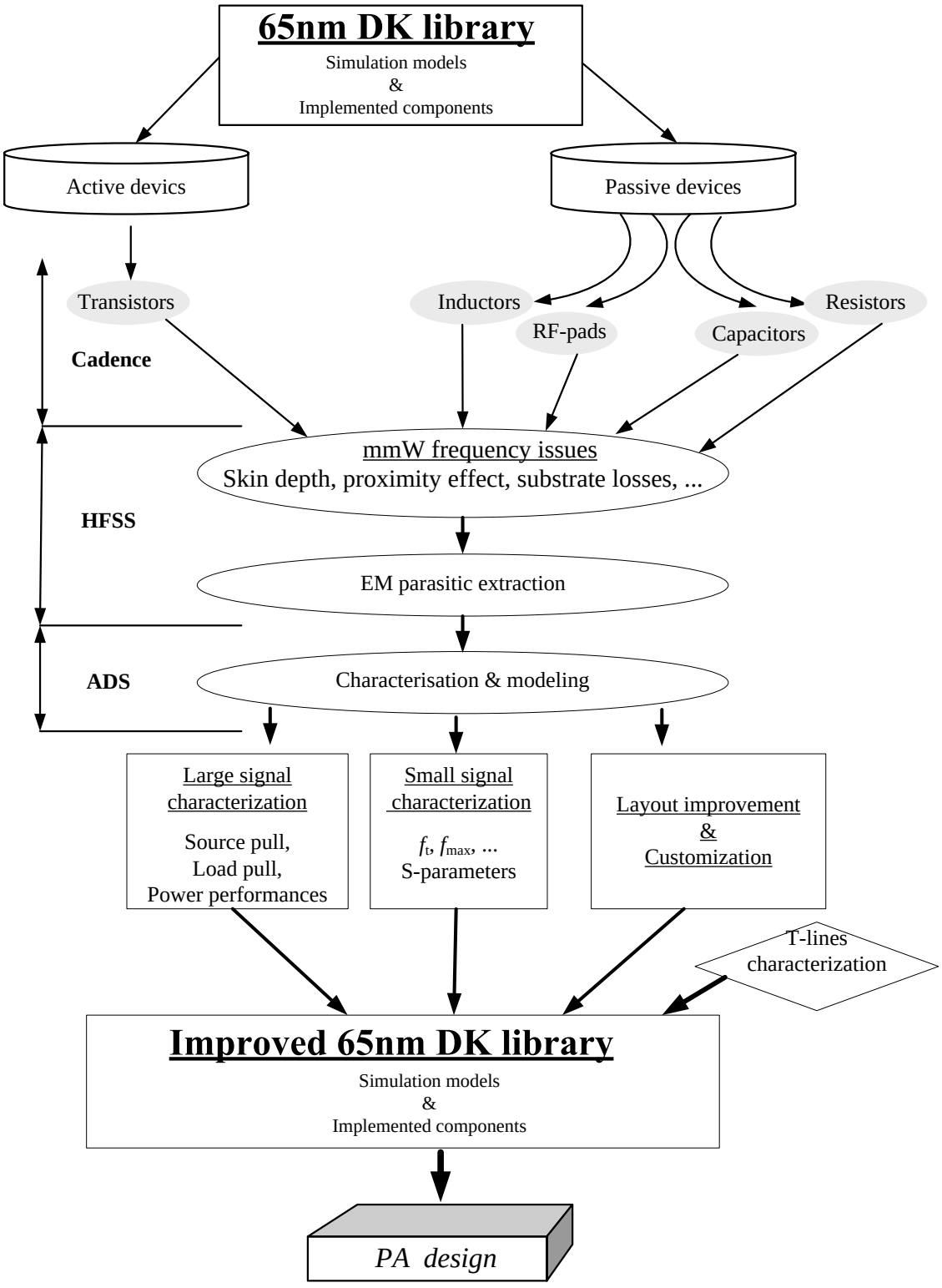


Figure 2.1: Design flow process of passive device characterization

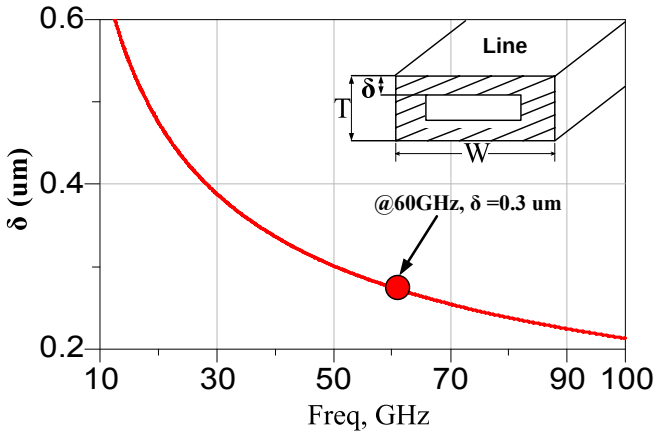


Figure 2.2: Skin depth effect vs. frequency

60GHz. Consequently the strip resistance becomes significantly greater than the DC resistance (Eq. 2.2).

$$R \approx \frac{\rho.l}{2\delta \cdot (T + W - 2\delta)} \geq R_{DC} \tag{2.2}$$

Return current consideration:

At RF frequencies, the return current flows through the lowest impedance path. So, a large path is sufficient to lower its resistance. Besides, at high frequencies, the return current is distributed to minimize the current loop size and thus reduces the inductance [68]. Moreover, as the return path flows only close to the RF line, the return current path is concentrated in a narrow path increasing the resistance. Figure 2.3 shows the return current path in both low and high frequencies in a CPW line. This distribution is a simplification of the return current path distribution in a chip environment. Indeed, in this case, a multitude of possible paths exists and it is difficult to modelize it accurately.

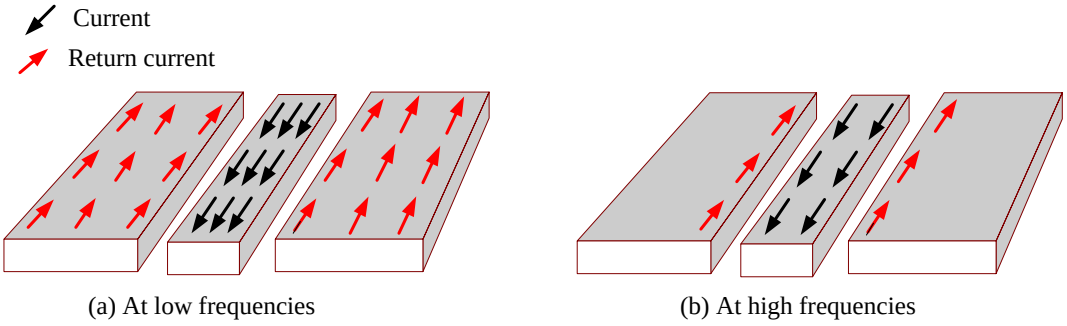


Figure 2.3: Frequency-dependent return current path in a CPW line

2.1.2 Simulation approximations

More elevated levels of metalization, shrunk photo lithography and the use of low dielectrics are some of the other improvements related to the 65nm CMOS BEOL [69]. However, the simulation of simple components integrated in such complex BEOL requires high memory resources. Hence, the simulation setup must be lighted.

As said before, the simulation of passive devices is required because of the unavailability of models at the beginning of our work. Before detailing simulation setup, a description of the 65nm CMOS BEOL is presented. Figure 2.4 plots the 65nm CMOS BEOL structure with the stacked metal levels and the dielectrics. The metallic part is composed by:

- 5 thin copper levels (from Metal 1 to Metal 5) which carry low power signals as for gate biasing.
- Metal 6, Metal 7 thick copper levels and the alucap level are used to carry high power. This is due to their higher thickness and their higher distance from the substrate leading to a better isolation and lower losses.

The metals are bathed on a silicon oxide which is used since its chemical properties limiting the diffusion of copper in the oxide. The silicon oxide is based on silicon nitride, low K-dielectric and a passivation layer. All of them are laid on a silicon substrate.

- The silicon nitride and the low K-dielectric benefit from a low thermal budget and a flexible stress tuning [70]. They have a low relative permittivity. It limits the capacitive coupling ensuring a better signal transmission. The drawback of those layers is that the circuit has no immunity to radiations caused by discontinuities, bends and current loops in circuits.
- The passivation layer is based on high relative electric permittivity dielectric leading to act as a trap for the electric field in the structure. Moreover, it protects the chip from electromagnetic disturbance.
- The silicon substrate has a thickness equal to $275\mu m$ without metallic ground plan [71]. The bulk has an average resistivity of $10\Omega.cm$. It can be noticed that the resistivity is lower at the top area of the substrate because of the non-uniform doping profile of the substrate (Figure 2.4).

3D EM HFSS simulator is used to characterize each passive device. It is based on Finite Element Method (FEM). The simulated structure is subdivided on tetrahedral-volume elements.

Hence, the structure is meshed in a flexible way in comparison to a cubic discretization used with Finite-Difference Time-Domain (FDTD) computation, especially in curvilinear or circular shaped boundaries. The solver operates in frequency domain and thus is suited to calculate S-parameters, especially for narrow band applications (resonators, filters). The major constraint of a 3D software is the requirements of a long computation time and high memory resources. The purpose is to have the possibility to simulate structures (inductors, T-lines, ...) implemented in this BEOL. The high number of dielectric layers makes the simulation setup complex. To improve those issues, some approximations in the geometry of the BEOL structure must be done:

- Substrate merging: in 65nm CMOS BEOL, there are more than 20 dielectrics stacked in a height (h) of $4\mu m$. The size of each dielectric layer is lower than the wave-length. So, it is not necessary to define them separately in order to reduce significantly the memory resources. Consequently, the BEOL is divided into three different equivalent dielectrics. A first one fits the thin metal levels together. A second one fits the high metal levels together. A last one fits the passivation layer. The equivalent dielectric is calculated for each two neighbor dielectrics using the Kraszewski formula (Eq. 2.3) [72]:

$$\xi_{eq} = (\sqrt{\xi_n} + \frac{h_{n-1}}{h_{n-1} + h_n} \cdot (\sqrt{\xi_{n-1}} - \xi_n))^2 \tag{2.3}$$

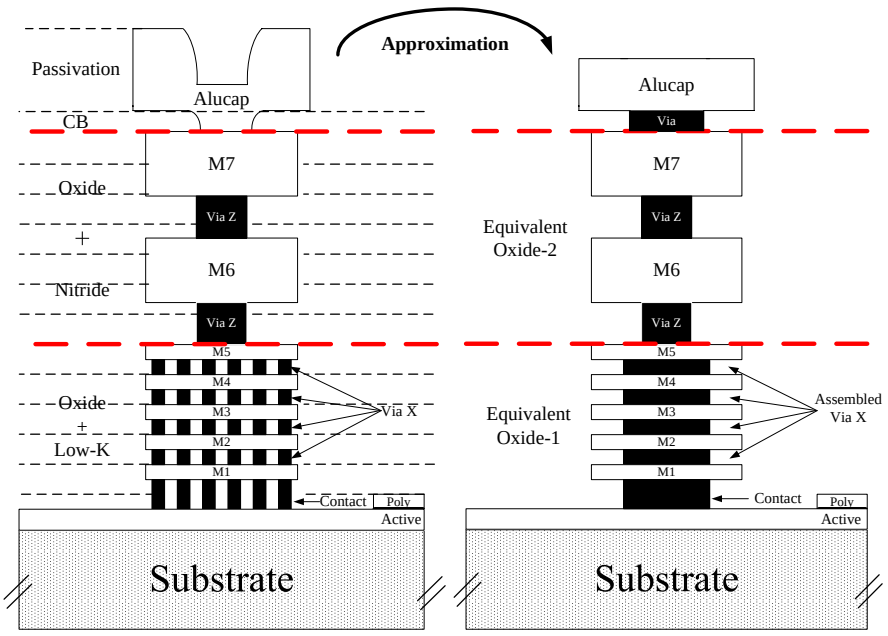


Figure 2.4: A 65nm CMOS BEOL structure

- Merging vias: the biggest via has an area of $3\mu m * 3\mu m$. It presents a small area compared to dimensions of a typical structure. Moreover, a large number of vias are mounted in parallel to ensure a low resistive connection between two metal levels. Consequently, their equivalent resistance can be neglected. This is why a group of vias can be merged to form one via block without significant change in simulation results. This approximation is also used in 2.5D software otherwise the structure is not simulated.

- A cubic alucap: the shape of the alucap is assumed rectangular. Its novel shape has the same volume as before to preserve the same resistance.

Having knowledge of the BEOL and software is our first investigation to perform rapid simulations to realize a first 60GHz PA in CMOS. It remains to be careful during measurements to make an appropriate comparison between predicted and measured results. The next paragraph discusses about measurement procedures.

2.1.3 Measurement setup

Measurements are carried out with an Agilent E83612 Vector Network Analyzer (VNA) to measure S-parameters from 10MHz to 110GHz (Figure 2.5). In fact, it has the flexibility of both

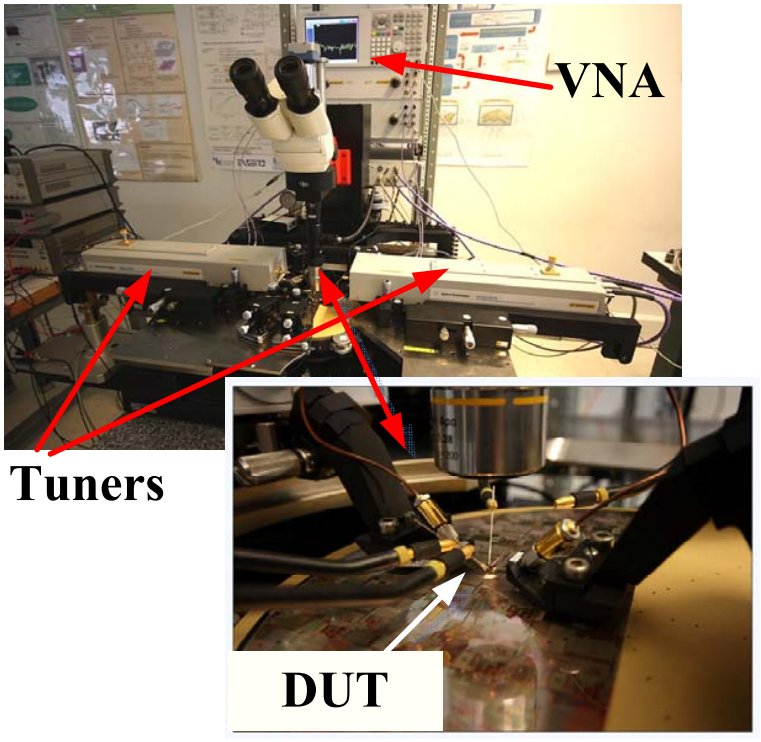


Figure 2.5: Agilent *mmW* VNA (10MHz to 110GHz) photography

a 10MHz to 67GHz VNA and *mmW* heads covering 67GHz to 110GHz. The VNA and the *mmW* heads are combined thanks to a controller. Hence, the VNA offers a broadband and high performance 110GHz system. During characterization, the Device Under Test (DUT) is excited with a -20dBm small signal power.

The *mmW* measurements require to pay attention during operations. Some parameters as serial resistance, inductance of a small DUT are comparable to parasitics of the measurement environment (cables, probes, ...). Two procedures are required to setup parasitic-free measurements. The DUT performances are accurately characterized after a calibration procedure and a de-embedding procedure. Those procedures are detailed as follows:

Calibration procedure:
The calibration computation is based on incident and reflected waves at a given reference plan. It aims at calibrating the VNA till the end of probes. Several calibration methods exist. All of them aim to well estimate a two-port error model. Line-Reflect-Match (LRM) [73], Through-Reflect-Line (TRL) [74] and Short-Open-Load-Thru (SOLT) [75] are the most common ones. Every method uses a non-perfect test structure which are well known in order to compensate their error in the matrix calculator.

Each method exhibits pro and cons. For instance, TRL calibration procedure requires different line lengths to cover a frequency decade. The SOLT technique is adopted since it needs only one T-line structure to have a good estimation of error matrix in a broadband [76]. The SOLT technique uses a 50Ω coplanar resistor as a reference impedance. Parasitic inductance and capacitance are estimated from the short and open impedances. Those parameters are correctly calculated only in a single reference plan. Figure 2.6 depicts the test structure die photographies.

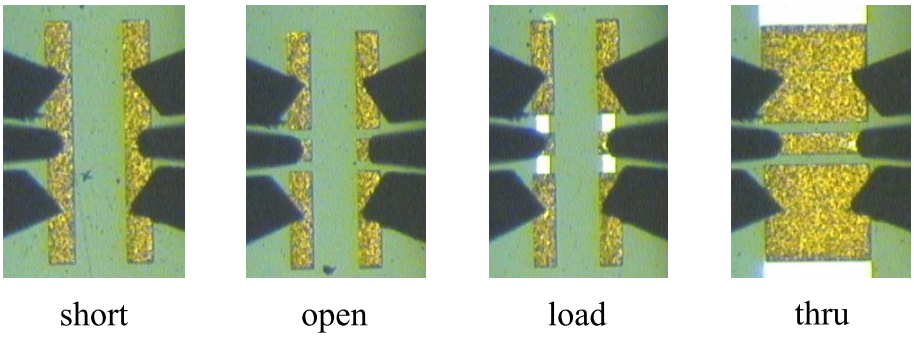


Figure 2.6: SOLT method circuits photographies

De-embedding procedure:

After proceeding measurements, de-embedding procedure must be performed. It aims at subtracting any additional parasitics located in the structure like I/O RF-pads and the access lines. The purpose is to consider only the DUT characterization. A correct de-embedding enables removing away the reference plan from the probes plan to any desired reference plan.

The choice of a method of de-embedding depends on the nature of the DUT (T-line, transistor, inductor, balun) and on the configuration of the design (wire bonding, bumps, ...). In our case, only measurements on wafer are performed. Open and open short corrections are the most used to characterize transistors or T-lines.

The parallel parasitics are dominated by the pads capacitance. The serial parasitics are dominated by the resistance and the inductance of the access lines. In a first part, configurations and formulas of both methods are illustrated. In a second part, a comparison between them is performed to highlight mmW measurement issues .

- **Open correction**: this correction removes the parallel parasitics (Figure 2.7). Hence, the capacitance of the RF-pad and the access lines are subtracted. The admittance matrix is used (Eq. 2.4). This operation does not remove resistive and inductive parasitic as shown in Figure 2.7.

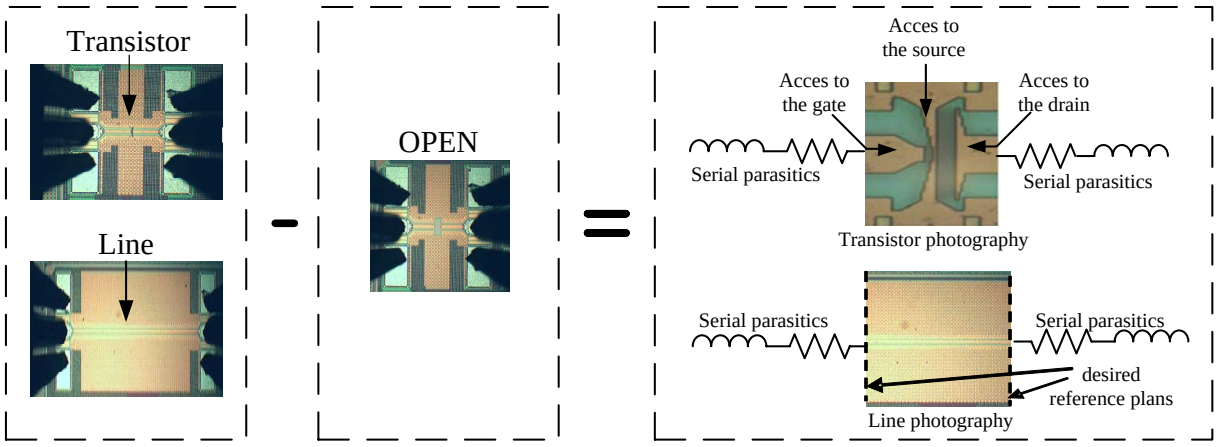


Figure 2.7: Open method parasitic extraction

$$\begin{aligned}[Y_{DUT}] &= [Y_{Meas}] - [Y_{Open}] \\ [S_{DUT}] &\longleftarrow [Y_{DUT}]\, to\, [S_{DUT}]\end{aligned} \tag{2.4}$$

- **Open-short correction**: this correction considers the serial parasitic in addition to the parallel ones (Figure 2.8). The procedure is described as follows :

$$\begin{aligned}[Y_{DUTOpen}] &= [Y_{Meas}] - [Y_{Open}] \\ [Z_{DUTOpen}] &\longleftarrow [Y_{DUTOpen}]\, to\, [Z_{Open}]\end{aligned} \tag{2.5}$$

$$\begin{aligned}[Y_{DUTshort}] &= [Y_{Meas}] - [Y_{short}] \\ [Z_{DUTshort}] &\longleftarrow [Y_{DUTshort}]\, to\, [Z_{DUTshort}]\end{aligned} \tag{2.6}$$

$$\begin{aligned}[Z_{DUT}] &= [Z_{DUTopen}] - [Z_{DUTshort}] \\ [S_{DUT}] &\leftarrow [Z_{DUT}]\, to\, [S_{DUT}]\end{aligned} \tag{2.7}$$

At RF frequencies, an open structure is sufficient to characterize a DUT subtracting the parallel parasitics. At mmW frequencies, resistive and inductive parasitics impedance become significant. Consequently, the open-short de-embedding procedure gives more accurate measurements.

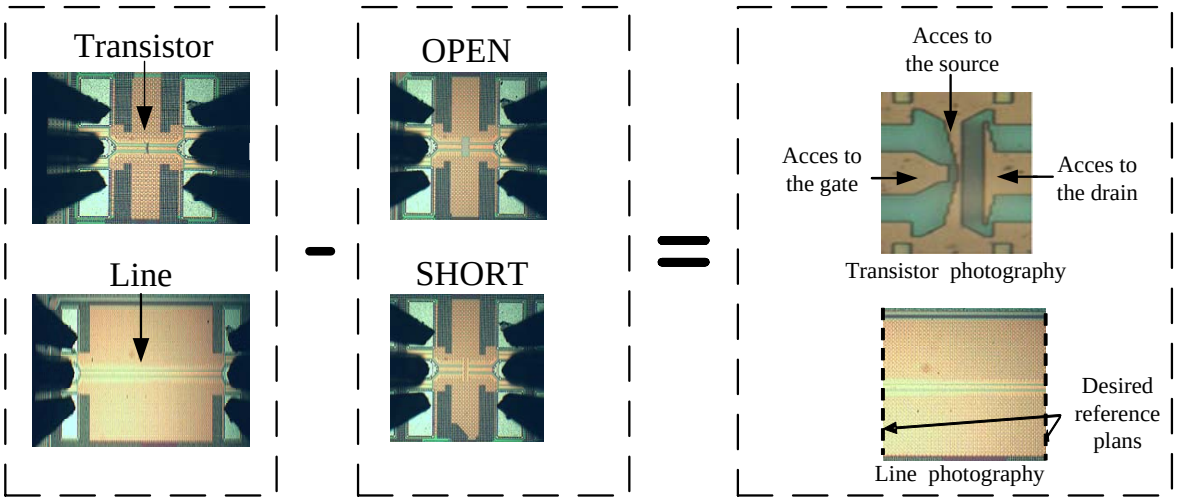


Figure 2.8: Open short method parasitic extraction

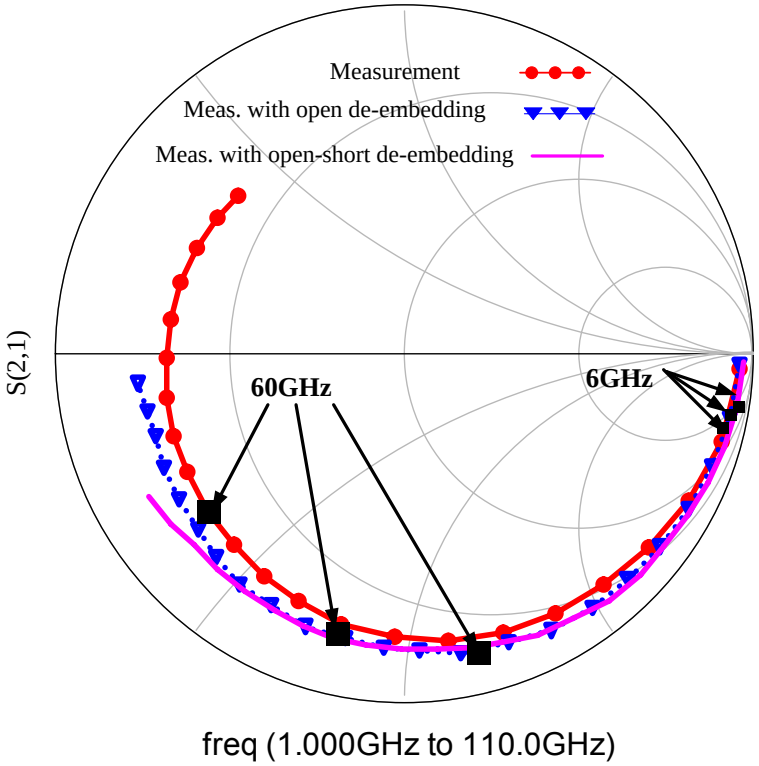


Figure 2.9: Impact of de-embedding methods on T-line measurement results

Figure 2.9 shows a comparison between those two methods illustrated by the S_{21} transmission parameter of a $500\mu m$ T-line, plotted in a Smith chart.

At 6GHz, de-embedding procedure is not mandatory. Nevertheless, with the frequency rise, the de-embedded measurements curves do not fit with the measurement results. The open-short procedure provides more accurate results in magnitude and phase.

Setting up de-embedding structures must be appropriate to DUTs. Indeed, open-short correction is adopted for long T-line and transistors. However, this is not efficient when the serial resistance of the DUT is comparable to the serial resistance of the short structure. The open-through de-embedding method presents an alternative method. It is used in a through devices such as T-line and inductor.

2.2 Passive Device Characterization

2.2.1 Transmission lines

T-lines are responsible for carrying and confining electromagnetic energy in one direction. Each T-line has characteristic parameters namely, the characteristic impedance (Z_c) and complex propagation constant (γ). Specific parameters such as losses and dispersions can be deduced from Z_c and γ. They are obtained using formula extracted from approximation functions and curve-fitting with quasi-static equations in frequency domain [77]. T-lines benefit from a broadband frequency behavior. Designing circuits with T-lines avoids ambiguities in return current path study and modeling because of the proximity of the signal path to the ground plan [9]. Thus, the frequency response of T-lines is characterized from DC to its cut-off frequency. For this reasons, T-lines are widely used to design circuit functions such as filters, coupling structures, power dividers and combiners. Moreover, they benefit from frequency scalability, high isolation and thus they are more suited to high frequency design.

A first part describes different T-lines topologies with their main applications. A second part aims at comparing the performances of two T-lines structures at 60GHz. This work is based on EM simulation data. The last part presents the experimental results of the adopted T-lines to be used in our PA design.

2.2.1.1 Transmission line topologies

4 main topologies of T-lines are distinguished. Many of derived forms exist. Figure 2.10 summarizes different topologies of T-lines. They are briefly described in the next paragraph.

- **Microstrip line (MS)**: it is the most popular one in RF domain. It consists in a conducting strip of width (w) and thickness (t) suspending on a dielectric of height (h) separating the signal path from the ground plan. The electric field has the property to be concentrated on the dielectric having the highest electric permittivity [78]. Hence, the major part of electric field is concentrated between the RF line and the ground plan. A little part of the electric field is concentrated in the interface between the dielectric and the surrounding air supporting quasi-Transverse Electromagnetic (TEM) mode of propagation. The characteristic impedance is function of the ratio (w/h).

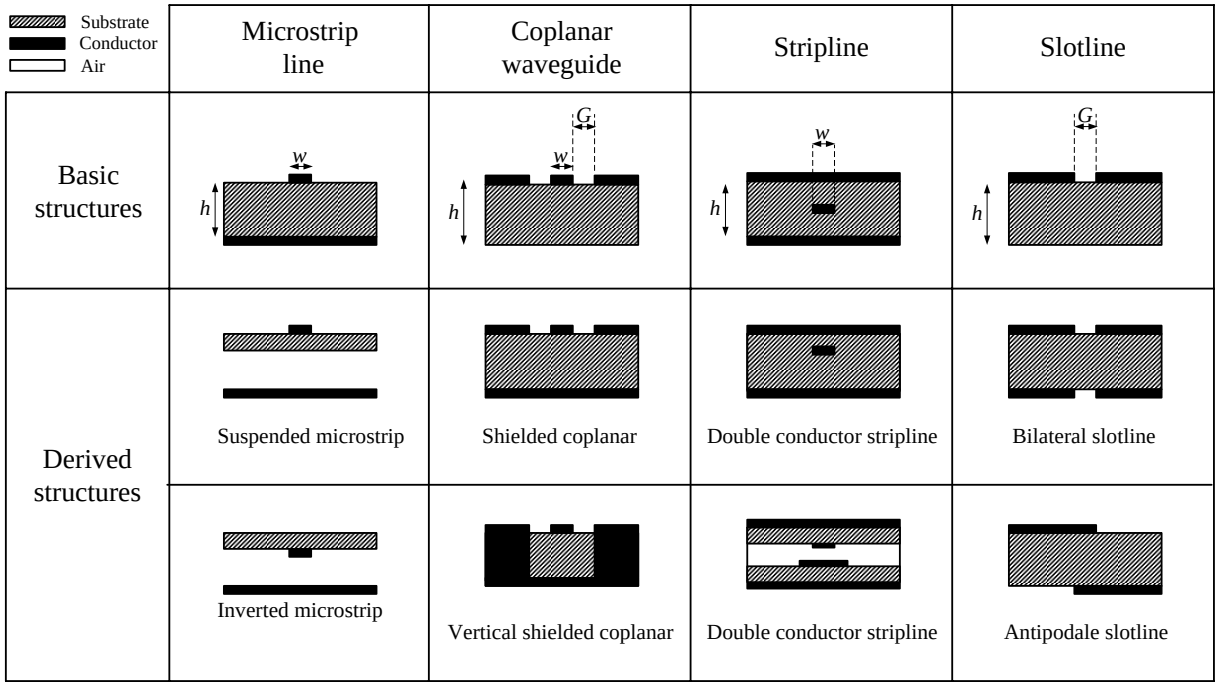


Figure 2.10: Main T-lines structures

- **CoPlanar Waveguide (CPW) line**: it consists in a center strip of width (w) separated by a gap (G) to an adjacent ground plan in each side. Most of electric field is concentrated between the RF line and the ground plan supporting TEM mode of propagation. The amount of electric field that spreads over the substrate is dependent on substrate resistivity. The characteristic impedance is function of $(w/(w+2G))$ according to [79]

- **Stripline**: it consists in a strip of width (w) located between two parallel ground plans. The stripline structure is considered as the only line that supports a real TEM mode of propagation with low losses [80]. It is insensitive to electromagnetic disturbances due to the non-exposed structure to the air. The calculation of the characteristic parameters is easier since the constant effective dielectric of the structure (the same as the one of the dielectric). Hence, it is more often used to ensure a stable source of antenna or to ensure stripline-coaxial junction transition. This topology is not recommended in CMOS technologies which have thin BEOL since there is a large capacitive coupling between the two ground plans. In addition, bottom metal levels do not have the same resistivity. Thus, the structure becomes asymmetric and difficult to be modeled.

- **Slotline**: it is a dual structure to microstrip structure [81]. It consists in a slot in a ground

plan. It has a small number of models. Moreover, it exhibits significant radiation losses and it is more often used as a source of radiation, not as a transmission line. Indeed, the radiated energy appears as energy loss if looked from pure circuit design. Thus, it is not adopted in the PA design where the goal of T-lines is to carry energy.

As explained before, the stripline and slotline structures are not suited to our application. The choice of the adopted structure is limited to MS line or CPW line. It is not possible to assert a better T-line structure. Each one exhibits its pro and cons. The choice of T-lines depends on:

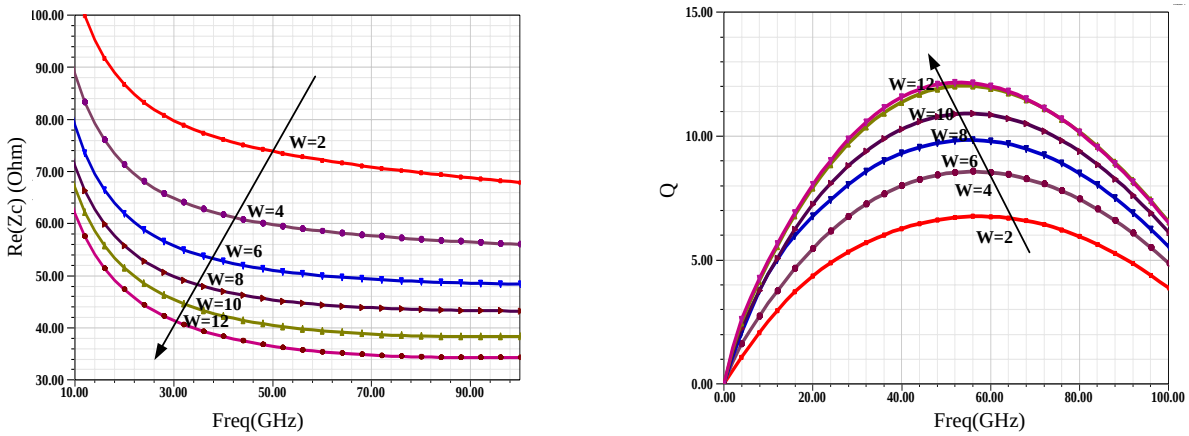
- **Targeted application**: the major constraint in PA design is the necessity to design wide strips to sustain high values of DC current. For instance, a line width of $9\mu m$ is mandatory to support a DC current of 100mA.

  The return current path in MS lines is located underneath the RF signal path. Hence, this constraint is also critical in the design of the MS line ground plan for class A PA. Typically, the ground plan is designed with Metal 1 and Metal 2. However, those low metal levels sustain less current than the high metal levels. Moreover, the 65nm CMOS BEOL sets a short distance of $4\mu m$ between the ground plan and the RF signal designed on Metal 7. So, w is a trade-off between a low serial resistance and a low capacitive coupling.

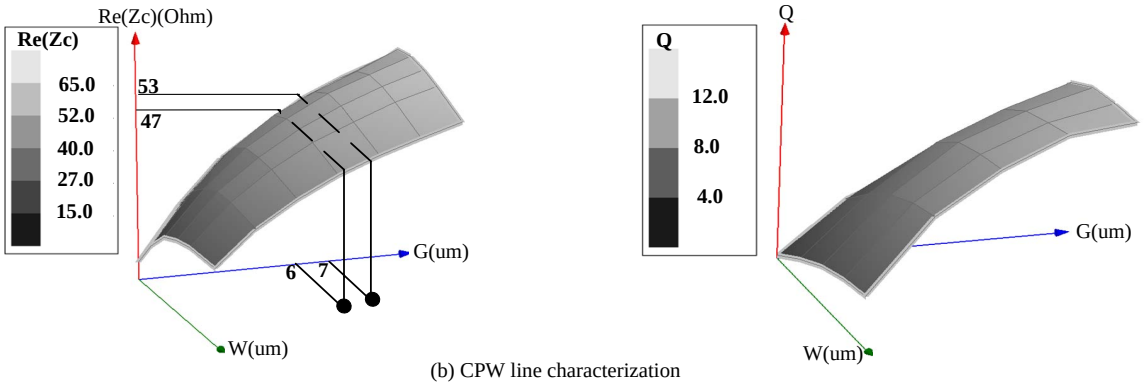
  With CPW line, the return current path passes throw a negligible resistance. In fact, a vertical ground plan is designed and it is distributed in all metalization levels from Metal 1 to Metal 7. Additionally, the absence of a ground plan under the RF signal in CPW line reduces the metallic capacitive coupling of the line with the ground improving the quality factor (Q). Nevertheless, the coupling with the substrate must be considered.

- **Sizing degree of freedom**: the most important role of T-lines in PA design is to perform impedance matching. MS lines have only w as a degree of freedom. For CPW line, two-variables (w, G) can be optimized to respect both sustaining high current and high Z_c. The two T-line structures are characterized with HFSS simulator. Figure 2.11 depicts the influence of those parameters on Z_c and Q.

  – With MS line, w varies from $2\mu m$ to $12\mu m$. It induces a variation of Z_c from 35Ω to 75Ω. This is promising for impedance matching. However with low w, Q is poor



(a) MS line characterization



(b) CPW line characterization

Figure 2.11: Characterization of a MS line and a CPW line

(less than 10) due to a high serial resistance. According to Figure 2.11, w must be set to $6\mu m$ to achieve a Z_c of 50Ω. This value is critical to sustain a high current and exhibits a low Q. Q increases when w increases. However, varying w from $10\mu m$ to $12\mu m$ does not change significantly Q. Indeed, the skin depth effect forces the current to flow through the surface (not through the volume) of the line. So, increasing indefinitely w does not improve continuously the T-line performances. Q reaches a maximum of 12.

– With CPW line, Z_c is more sensitive to the variation of G. In order to be as close as possible to 50Ω, G must be set between $6\mu m$ to $7\mu m$ with a w larger than $8\mu m$. Notice that Z_c can reach 65Ω with $G > 10\mu m$ but it is not realistic to increase indefinitely the gap. Indeed, the coplanar mode must be maintained between the RF line and the adjacent ground plan reducing as much as possible the electromagnetic fields retrieved in the substrate. w influences the serial resistance and hence the Q of the line. Concerning w, as explained in MS line characterization, it is not necessary

to increase continuously w. Consequently the 50Ω CPW line dimensions are set to $(w, G) = (10\mu m, 6.5\mu m)$. Q reaches a maximum of 12 at 60GHz. In spite of substrate losses in CPW lines, the Q reaches the same value as in MS lines.

- **Area consumption and coupling issues**: CPW lines have more flexibility to reach higher Z_c with low losses. In one hand, CPW T-lines can easily play the role of inductors with a shorter length compared to MS line. In the other hand, it is important to analyze the distance in the cross direction between the line and a neighbor component to avoid coupling issues. It is commonly said that CPW line must have a large ground plan to support as well the quasi-TEM mode of propagation and to be close to a semi-infinite plan used in CPW theory [82]. However, most of electric fields are confined between the RF line and the ground plan. CPW line and a MS line are simulated to demonstrate the coupling effect. Figure 2.12 plots the principal component of the electric field vector probed in different regions, namely at the air level, at the oxide level and at the substrate level (close to the area).

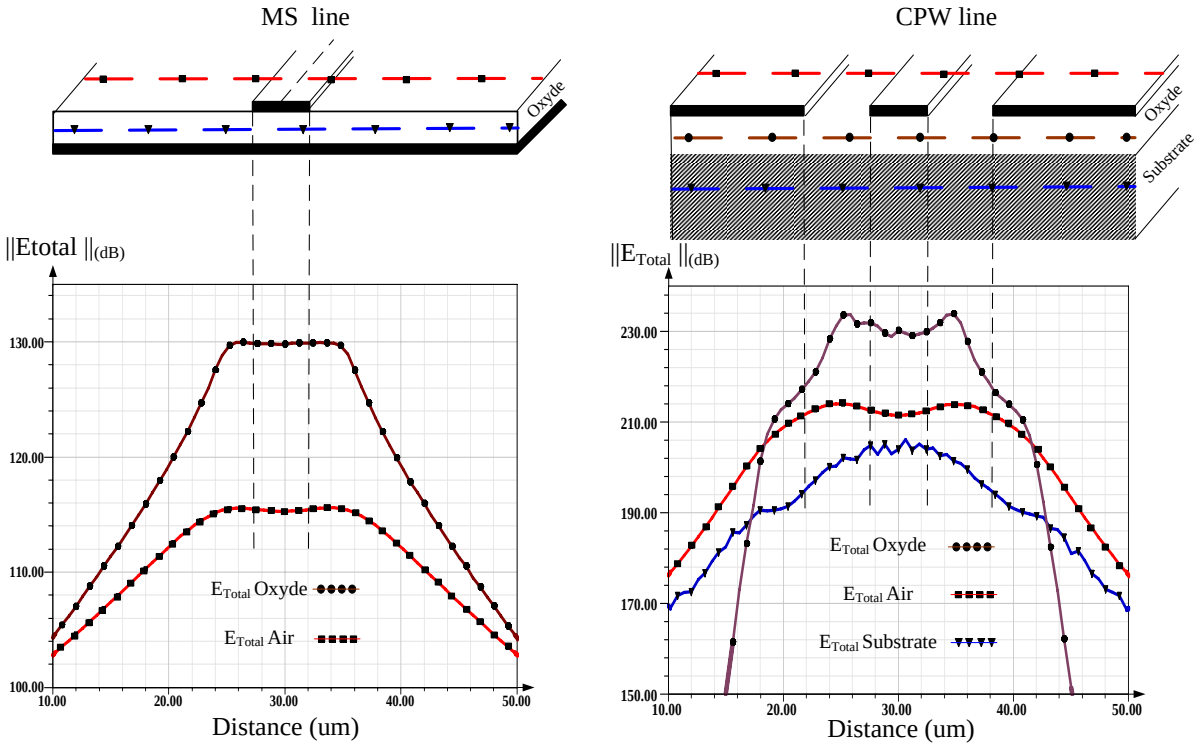


Figure 2.12: Electric field distribution in a MS line and a CPW line

– With MS line, the electric field is concentrated only in the oxide and in the air. The substrate is completely shielded. The capacitance formed by the strip and the oxide is higher than the capacitance formed by the strip by the air. Consequently, most of the electric field is concentrated in the oxide. However, the electric field lines are wide-spread in an area that achieves more than $3*w$ on each side. So, every component routed closer to $3*w$ has an important susceptibility.

– With CPW line, this phenomenon is attenuated since the vertical ground plan is distributed in all metalization levels. This vertical ground plan is equivalent to a wall. Thus, the coupling with neighbor components is reduced significantly. The electric field reaches its maximum magnitude at the side slots. However, the RF line is directly exposed to the substrate. Due to the high ξ_r=11.7 of the substrate, an important amount of electric fields is absorbed. It presents the major source of losses in CPW structure.

Table 2.1 summarizes positive and negative behaviors of MS line and CPW line structures in 65nm CMOS technology.

Table 2.1: MS lines Versus CPW lines

	MS lines	CPW lines
Simplicity of modeling	++	+
Metallic losses	-	++
Substrate losses	+++	–
Coupling	–	++
Quality factor	-	-

The CPW topology is preferred and adopted for designing our PA. The major drawback of using CPW instead of MS is the misreading of the local resistance of the substrate (dope profile, process) whereas the MS line design and analysis ignore completely the substrate.

2.2.1.2 T-line characterization and measurements

When a T-line is excited by a voltage source, $V(z)$ and $I(z)$ are defined according to telegraphist equations [83] [84] by:

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0 \tag{2.8}$$

$$\frac{d^2I(z)}{dI^2} - \gamma^2 I(z) = 0 \tag{2.9}$$

Where γ is the complex propagation constant defined by:

$$\gamma = \alpha + j\beta \tag{2.10}$$

Where β is the imaginary part of the complex propagation constant presenting the phase per unity of length. β is not explicitly calculated. Usually, it is expressed in function of ξ_r.

$$\beta = \frac{2\pi}{\lambda_g} = \frac{2\pi\sqrt{\xi_r}}{\lambda_0} \tag{2.11}$$

And α is the real part of the complex propagation constant. It presents the attenuation constant of the propagated wave. It is expressed in neper/meter. It is the sum of three attenuation sources [85]. Their distribution depends on the T-line topology:

$$\alpha = \alpha_c + \alpha_d + \alpha_g \tag{2.12}$$

Where:

α_c is the conductor losses (skin depth effect)
α_d is the dielectric losses
α_g is the substrate losses

α_c, α_d and α_g are estimated and expressed in function of physical and geometric parameters of the metalization line and the substrate. They are equal to :

$$\alpha_c = 8,696 \cdot 10^{-3} \cdot \frac{\sqrt{R_{DC}^2 + R_{HF}^2}}{2.Z_c} \tag{2.13}$$

$$\alpha_d = 27,3 \cdot 10^{-}3 \cdot \frac{\xi_r}{\sqrt{\xi_{reff}}} \cdot \frac{\xi_{reff} - 1}{\xi_r - 1} \cdot \frac{\tan(\delta)}{\lambda_0} \tag{2.14}$$

$$\alpha_g = 8,696 \cdot 10^{-3} \cdot \frac{G.Z_0}{2} \tag{2.15}$$

α_d is the lowest source of attenuation. α_c and α_g are the dominant sources at mmW frequencies. It is due to the frequency-dependence of the resistance R and the conductance G.

$$R = \frac{\sqrt{\pi\mu\rho \cdot f}}{W} \tag{2.16}$$

$$G = 2\pi \cdot C \cdot tg(\delta) \cdot f \tag{2.17}$$

By replacing the expression of R and G from Eq. 2.16 and Eq. 2.32 in Eq. 2.13 and Eq. 2.15, at high frequencies, dielectric losses are more important than resistive losses. They reflect the leakage current in the substrate. It is generally modeled by a conductance proportional to f while the conductor losses are proportional to $\sqrt{f}$.

The solution of Eq. 2.11 is a sum of forward V^-_{max} and reverse V^+_{max} propagating waves in z direction:

$$V(z) = V^+_{max} \cdot exp^{-\gamma z} + V^-_{max} \cdot exp^{\gamma z} \tag{2.18}$$

T-line characterization:
To characterize any T-line, γ and Z_0 must be determined. Two S-parameter-based methods are demonstrated to calculate them using EM software.

- From the chain ABCD chain matrix:

$$A = \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}} \tag{2.19}$$

$$B = Z_c \cdot \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}} \tag{2.20}$$

$$C = \frac{1}{Z_c} \cdot \frac{(1 - S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}} \tag{2.21}$$

$$D = \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{2S_{21}} \tag{2.22}$$

γ and Z_c are then deduced :

$$Z_c = \sqrt{\frac{B}{A}} \tag{2.23}$$

$$\gamma = \frac{arccosh(A)}{l} \tag{2.24}$$

- from S-parameters directly:

$$exp(\gamma.l) = \frac{1 - S_{11}^2 + S_{21}^2 + \sqrt{(1 + S_{11}^2 - S_{21}^2) - (2S_{11}^2)}}{2S_{21}} \tag{2.25}$$

$$Z_c = 50.\sqrt{\frac{(1 + S_{11}) - (1 - S_{21}S_{12})}{(1 - S_{11})(1 - S_{22}) - S_{21}S_{12}}} \tag{2.26}$$

After determining Z_c and γ, those parameters are used to extract a lumped RLCG model from Eq. 2.27 and Eq. 2.28. T-lines are represented by a distributed ladder network. It includes serial inductors, serial resistance, shunt capacitors and resistors connected as follows (Figure 2.13):

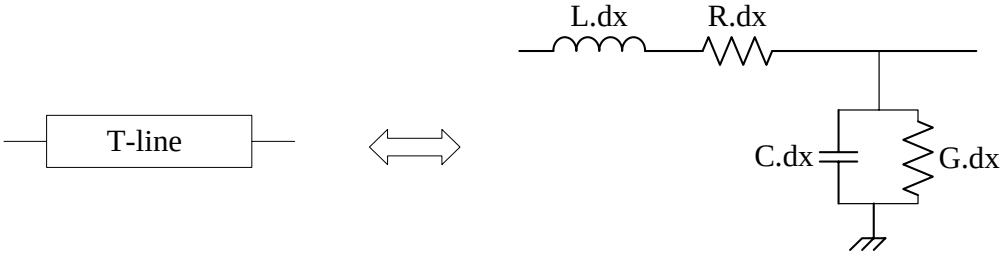


Figure 2.13: A RLCG T-line model

$$Z_c = \sqrt{\frac{R + jLw}{G + jCw}} \tag{2.27}$$

$$\gamma = \sqrt{(R + jLw)(G + jCw)} \tag{2.28}$$

The R, L, C, G values are deduced by using Eq. 2.29, Eq. 2.30, Eq. 2.31 and Eq. 2.32:

$$R = \Re e(Z_c \cdot \gamma) \tag{2.29}$$

$$L = \frac{\Im m(Z_c \cdot \gamma)}{2\pi \cdot freq} \tag{2.30}$$

$$C = \frac{\Im m(\frac{\gamma}{Z_c})}{2\pi . f} \tag{2.31}$$

$$G = \Re(\frac{\gamma}{Z_c}) \tag{2.32}$$

Where:

- R is the resistance per unit lenght (Ω/m)
- L is the inductance per unit lenght (H/m)
- C is the capacitance per unit lenght (F/m)
- G is the conductance per unit lenght (S/m)

R and G are not considered if the dielectric and the conductor are assumed to be perfect. Considering our application requirements, those two parameters must be carefully calculated presenting the principal source of losses including defaults as the finite thickness, the non-ideal conductivity of strips and the non-resistive substrate. The RLCG parameters are frequency dependent from DC to 110GHz. However, it can be assumed to be constant in the useful band namely, from 57GHz to 64GHz. A CPW sized by $(w, G) = (10\mu m, 6.5\mu m)$ is realized. Figure 2.14 shows the RLCG values for this line.

There is a good agreement between simulation results and measurement results. The resistance is negative for frequencies higher than 70GHz. This is not realistic. It is caused by the de-embedding calculation. This issue is often seen in the determination of the serial resistance of a device when its value is comparable to the serial resistance of de-embedding structures.

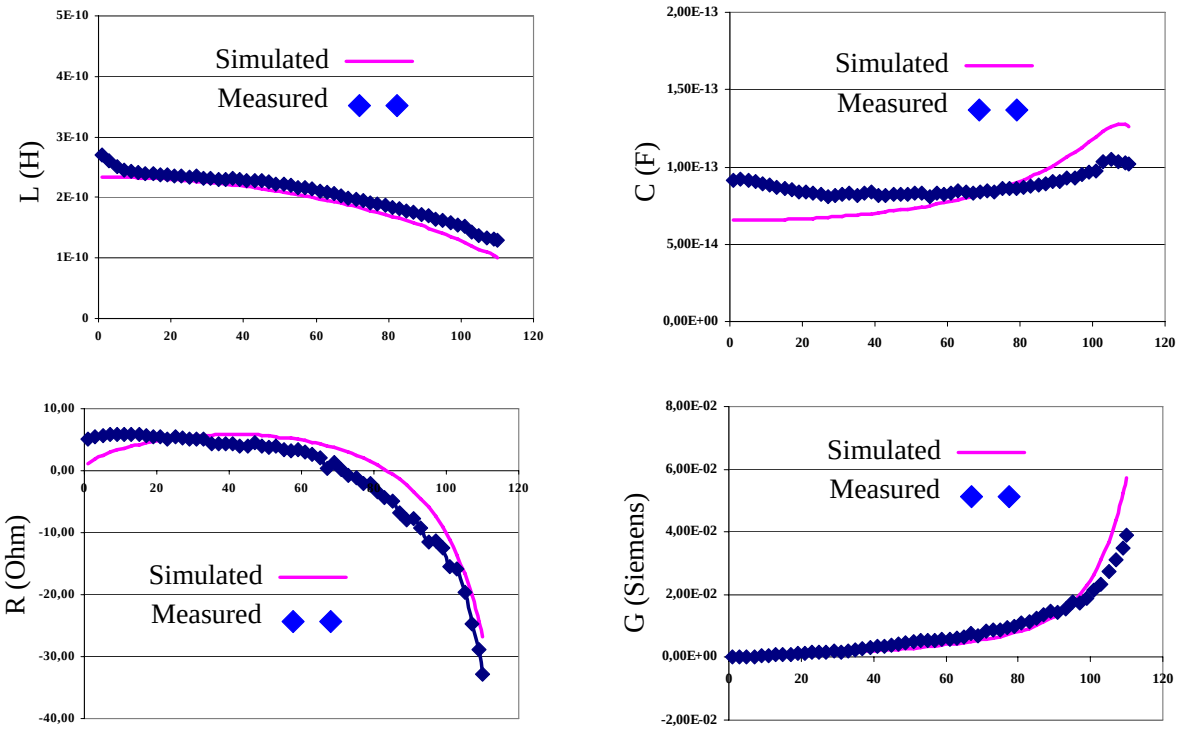


Figure 2.14: Simulated and measured RLCG parameters of a CPW line $(w, G) = (10\mu m, 6.5\mu m)$

After determining RLCG parameters, the model is not yet complete. A first check must be done. The ratio between the T-line (*length*) and λ must be calculated. A T-line must be considered as a lumped or as a distributed element. If $(length/\lambda) < 0.01$ the T-line is considered as a lumped element. Thus, the RLCG model is complete. Otherwise, the line is considered as a distributed element. In this case, the RLCG model must be subdivided in a number of cells $\geq$ N (Figure 2.15). N is the minimal number of elementary RLCG cells given by Eq. 2.33 [86], where T_r is the rise time of the T-line.

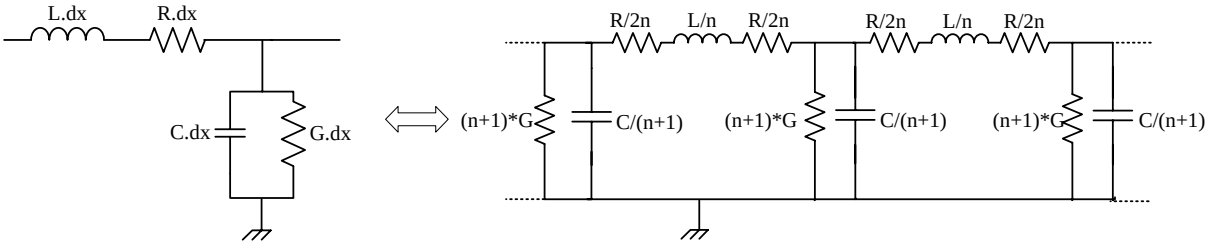


Figure 2.15: A distributed RLCG T-line model

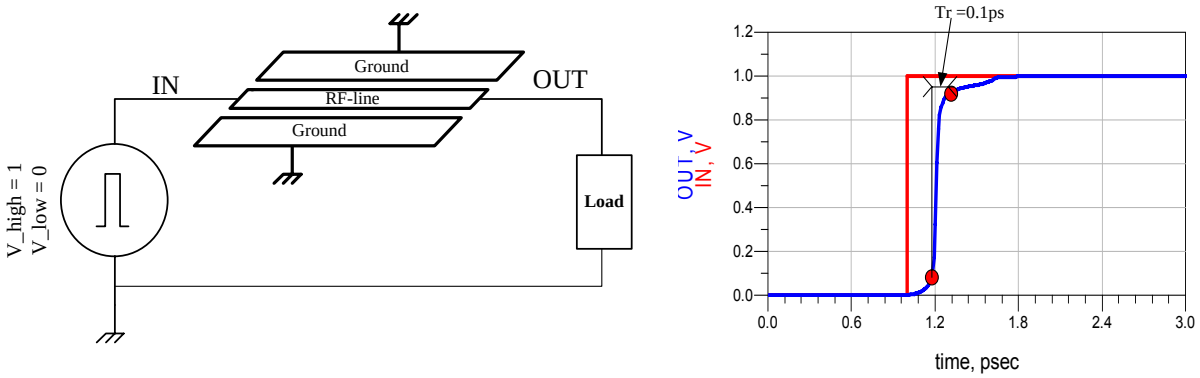


Figure 2.16: Determination of T-line T_r

$$N \geq 5 \cdot \frac{l \cdot \sqrt{LC}}{T_r} \tag{2.33}$$

Figure 2.16 shows the simulation determining T_r (between 10% and 90%). T_r is estimated to 0.1ps. So, the RLCG model is subdivided into N=9 cells. The achieved model is depicted in Figure 2.15.

Measurement results

A $(w, G) = (10\mu m, 6.5\mu m)$ CPW line, a $(w, G) = (10\mu m, 6.5\mu m)$ shielded CPW line and a $(w = 10\mu m)$ MS line are measured. The length of each T-line is equal to $300\mu m$. Z_c is extracted

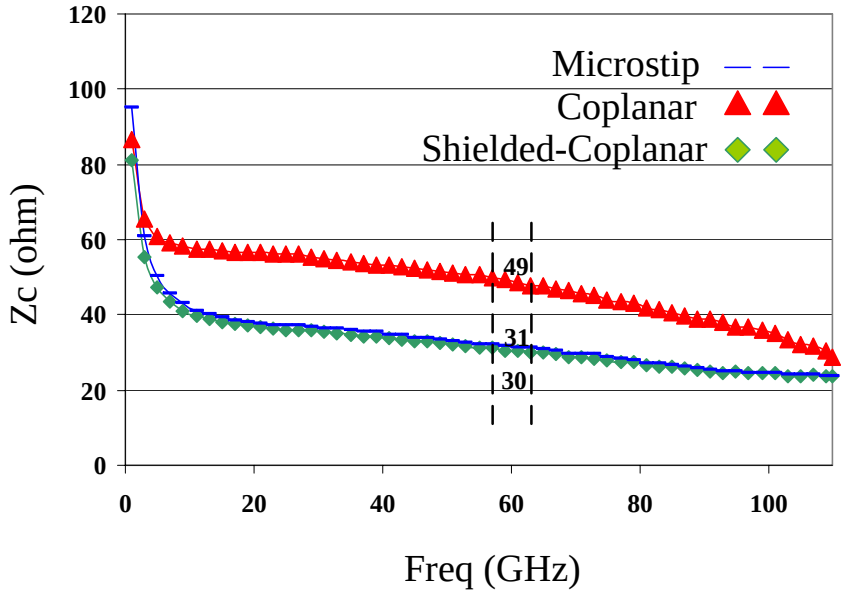


Figure 2.17: Z_c of different T-line structures

using Eq. 2.26. Figure 2.18 shows the Z_c of those three T-lines. The MS line and the shielded CPW line have the same Z_c of 30Ω. Indeed, due to the close proximity of the ground plan to the RF signal, the MS mode of propagation dominates instead of the CPW mode of propagation. The CPW line exhibits a $Z_c = 50\Omega$ at 60GHz, as expected during simulations (Figure 2.11). Z_c decreases with frequency. This is due to the skin depth and the proximity effect described in section 2.1.1.

Figure 2.17 plots the attenuation of a $(w, G) = (10\mu m, 6.5\mu m)$ CPW line from DC to 100GHz. It exhibits an attenuation of 1.6dB/mm at 60GHz. α can be accurately extracted only when the length of the line exceeds $\lambda_g/4$. To limit the die area, only a long CPW line of $625\mu m$ is sent to foundry. The values of α extracted from short lines ($300\mu m$) are not useful.

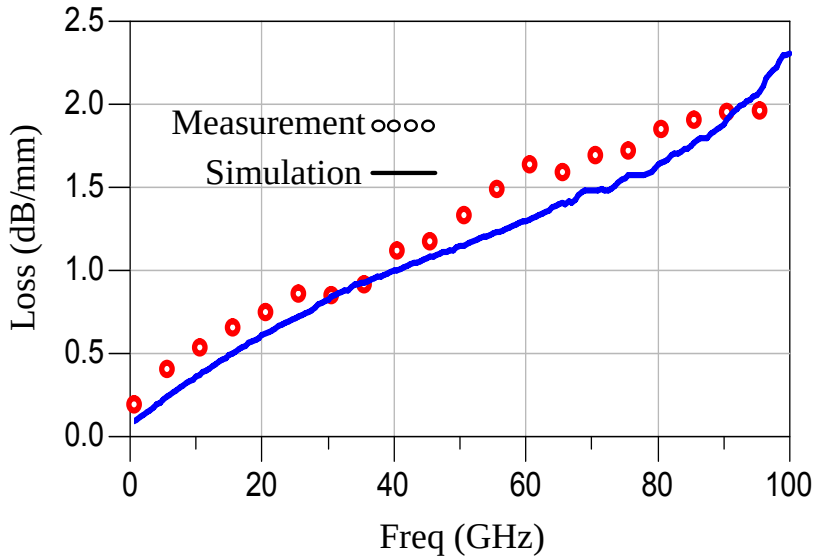


Figure 2.18: Attenuation in a CPW line $(w, G) = (10\mu m, 6.5\mu m)$

2.2.2 Inductors

Inductors are required in passive circuits such as filters and in active circuits such as PAs, LNAs, VCOs, mixers, ... Their most important roles are:

- Impedance matching by tuning out and neutralizing transistor capacitances,
- Operating as a choke inductor to protect transistors,
- Inductive source degeneration to improve linearity in PA design,
- Inductive source degeneration to minimize noise in LNA design,
- Performing a desired coupling in filters and transformers.

At *mmW* frequencies, inductors keep the same roles. However, they have complex behavior which increases the difficulty of the design. Indeed, frequency-dependent lossy substrate and metals make coupling effects difficult to be modeled accurately, especially for broadband applications.

At 60GHz, there is no need for high inductances to perform matching. Typical values are under 150pH. This is convenient to design small inductors limiting the analysis complexity. Their structures are simple namely in square spirals, circular or orthogonal shapes.

Our study aims at understanding the behavior of inductors to reduce as much as possible their losses. Q is the FoM in such investigation. The first part focuses on octagonal inductors which are available in the 65nm CMOS DK from STMicoelectronics. After analyzing their structure and performances, its structure is optimized to operate at 60GHz. The second part deals with square inductors. They are firstly analyzed by EM simulations for quantitative evaluation. Finally, this work is validated by experimental results.

2.2.2.1 Octagonal inductor analysis

The 65nm CMOS DK from STMicroelectronics contains a large number of inductor structures. Furthermore, most of them have an accurate model till 20GHz. Only one type of inductor (ind-low) remains relevant till 50GHz. Figure 2.19 depicts the inductor structure plotted in different views. The RF strip is composed by 4 metals connected in parallel (from Metal 5 to alucap) to reduce the serial resistance. A Patterned Ground Shield (PGS), formed by Metal 1, Metal 2, poly-silicon and buried N+/P+ material are placed beneath the RF strip to isolate the

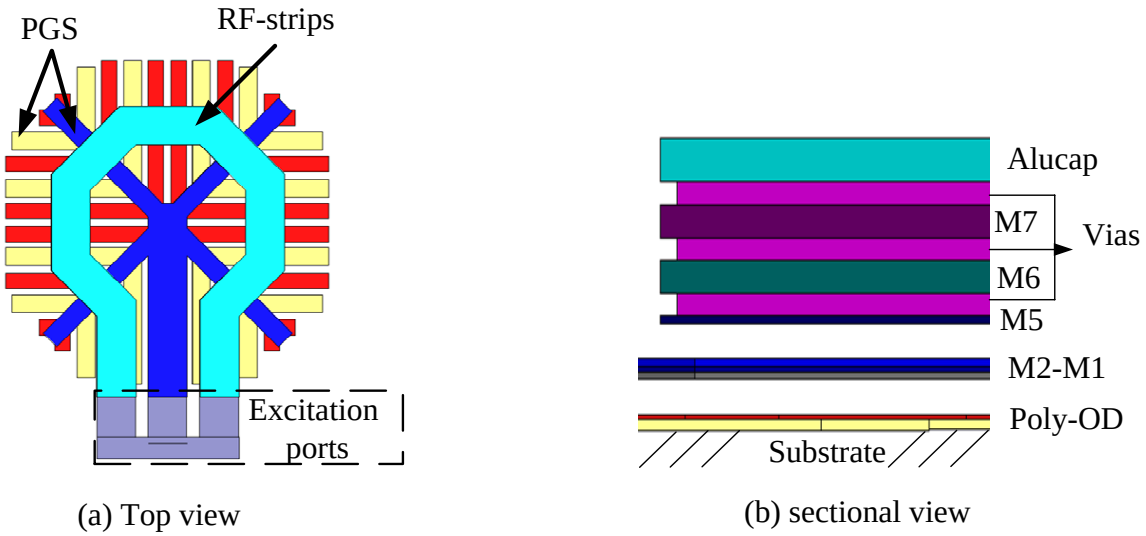


Figure 2.19: Octagonal inductor structure

inductor from the substrate. w and the diameter (D) are equal to $10\mu m$ and $40\mu m$ respectively. Figure 2.20 depicts the inductor lumped model. It is the standard π-model with frequency-independent lumped elements, where:

- C models the inter-winding capacitance between the traces,
- C_{ox} and C_{sub} model the oxide and the substrate capacitors formed by the metal strips,
- L_s and R_s model respectively the serial inductance and the serial resistance of the strips,
- R_{ox} and R_{sub} present respectively the resistance of the oxide and the substrate.

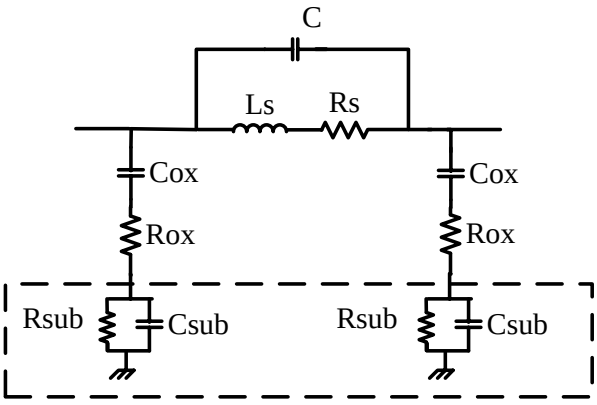


Figure 2.20: Inductor lumped model

This model requires an input frequency to be assumed accurate around this frequency (narrow band). This model does not consider the distributed effects, proximity effects, the skin effect [87]. Moreover, the π-model is a first order model which is not functional for frequencies higher than the first resonance.

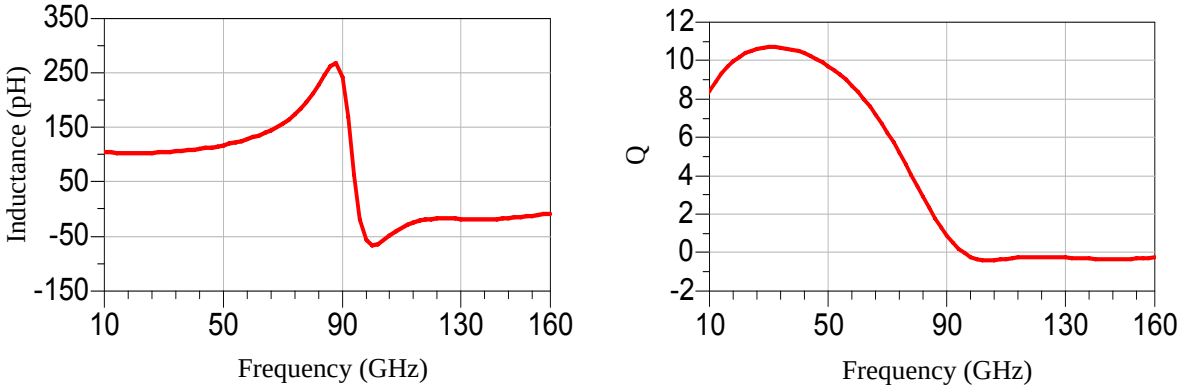


Figure 2.21: Performances of the octagonal inductor model

The simulated L and Q are shown in Figure 2.21. At frequencies below 30GHz, L is close to 100pH ($\pm$5%) whereas Q reaches a maximum of 11 at 32GHz. This inductor can be implemented in a circuit operating at 60GHz, but it exhibits an inductance of 130pH and a Q_{max} of 8. This is due to the close Self-Resonant Frequency (SRF) ($\approx$ 96GHz) to 60GHz. Moreover, a maximum of Q_{max} equal to 11 is a low value. A typical inductor has a $Q_{max} > 20$. Consequently, this structure requires improvements to reach better performances.

In order to support our study, we determine in a first part how resistive and capacitive losses degrade inductor performances. In a second part, we optimize the inductor structure. So, the effect of the PGS pattern effect and the distance separating the RF strip from the substrate are investigated.

Q of an inductor is defined as the ratio of the magnetic energy stored in the inductor to the energy dissipated (Eq. 2.34). Those amounts are hardly quantified. Instead of working with complex electric models, a simplified equivalent energy model is used (Figure 2.22), detailed in [88] and [89], where L_s, R_s, R_p and $C_o = C_p + C_s$ represent the overall inductance, conductor loss, substrate loss and overall capacitance respectively.

$$Q = \frac{PeakMagneticEnergy - PeakElectricEnergy}{EnergyLossinOneOscillationCycle} \tag{2.34}$$

$$E_{Electric} = \frac{V_0^2.C_0}{2}$$

$$E_{Magnetic} = \frac{V_0^2.L_s}{2((wL_s)^2 + R_s^2)}$$

$$E_{Loss} = \frac{2\pi}{w} \cdot \frac{V_0}{2} \cdot (\frac{1}{R_p} + \frac{R_s}{(wL_s)^2 + R_s^2})$$

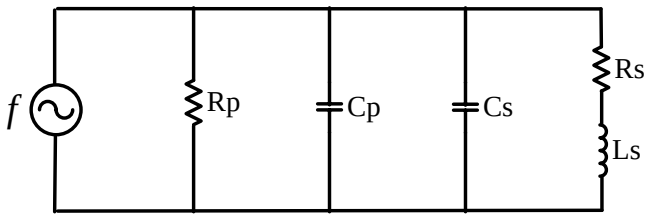


Figure 2.22: Inductor lumped model

According to the energy model, magnetic and electric energies are calculated and reported in (Figure 2.22). Consequently, Q is calculated thanks to Eq. 2.34. It is equal to:

$$Q = \underbrace{\frac{wL_s}{R_s}}_{1} \cdot \underbrace{\frac{R_p}{R_p + [(\frac{wL_s}{R_s})^2 + 1]R_s}}_{2} \cdot \underbrace{(1 - \frac{R_s.C_0}{L_s} - w^2 L_s C_0)}_{3} \tag{2.35}$$

- The first term expresses the magnetic energy stored and the ohmic loss in the conductor.
- The second term represents the energy dissipated in the substrate.
- The last term is the SRF factor describing the reduction in Q due to the increase in the peak electric energy with the frequency rise.

For a given BEOL and inductor size, R_p and C_p are constant. Consequently, only R_s and C_0 varied to influence on Q. R_s is changed by varying the metal resistivity. C_0 is changed by varying ξ_r of the oxide. Figure 2.23 plots the variation of Q in function of R_s and C_0.

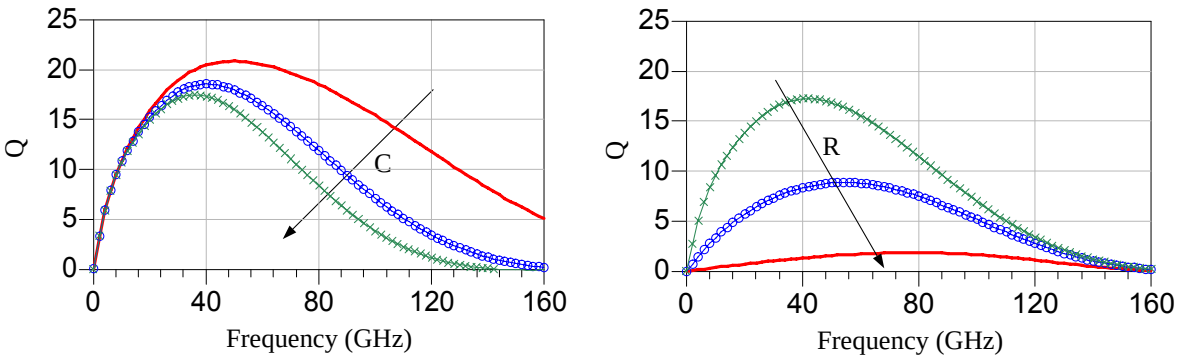


Figure 2.23: Inductor lumped model

The variation of R_s much influences on Q at low frequencies. It acts on the first term of Q. Hence, the increase of R_s degrades Q_{max}. Besides, the variation of C_0 acts directly in the third term inducing a frequency shift in the SRF. The influence of the capacitive effect is not visible at low frequencies. At 60GHz, capacitive coupling with the substrate is our major of interest.

The current flows into the substrate through capacitive coupling. It is induced into the substrate through magnetic coupling. This phenomenon adds losses and reduces the total inductance (negative feedback). To reduce this effect, an efficient method consists in etching the substrate to have a thick oxide layer to isolate the inductor from the substrate [90] [91] [92]. This method is filtered out since it increases process complexity and fabrication cost.

An other technique is extensively adopted at RF frequencies to prevent from the substrate current. It consists in placing a PGS as far as possible from the inductor strip and as close as possible to the substrate (Figure 2.19) [93] [94]. The purpose of the PGS is to end the electric field lines at the PGS level and not at the substrate layer. The slots located between 2 strips should be sufficiently narrow, so the vertical electric field can not leak through the PGS. Additionally, they present an open circuit for the induced current loop. The PGS must be designed in the orthogonal plan of the magnetic current direction to block the current flows.

To analyze the effect of the PGS on inductor performances at mmW frequencies, three inductors are simulated:

- The first one is the available inductor in the 65nm CMOS DK from STMicroelectroics designed with a PGS and with buried N+/P+ material (NP).
- The second one does not contain any NP.
- The last one is composed only by RF strips (without PGS and NP).

Figure 2.24 plots their L and Q. At frequencies below 30GHz, L is close to 110pH for every inductor. However, the SRF is improved from 100GHz to 150GHz by suppressing the PGS. Moreover, Q_{max} is also improved from 11 to 21. Those results demonstrate how the shielding of an inductor at mmW frequencies degrades its performances. Indeed, a PGS is considered to be responsible for increasing the intrinsic capacitance of the inductor. So, the capacitive coupling is more important causing a significant reduction of its SRF. This negative effect remains valid at RF frequencies. However, typical RF inductance is equal to some nH. The additional capacitance of the PGS has less damages on the total inductance of the inductor.

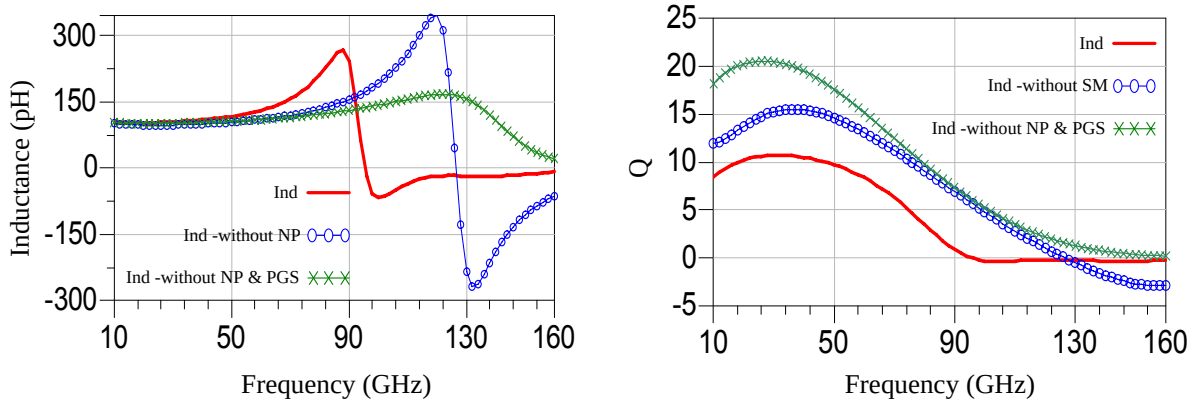


Figure 2.24: Effect of shielding inductor on L and Q at mmW frequencies

The inductor and the PGS can be seen as a transformer where the primary and secondary represent the inductor and the solid ground shield respectively [89]. The main issue is the thin structure of the BEOL. Indeed, the distance between Metal 2 (the secondary) and Metal 5 (the primary) is less than $1\mu m$. Consequently, the high capacitive coupling increases the negative mutual inductance of the secondary reducing the total inductance. The main rule is to avoid negative mutual coupling while minimizing the impedance to ground. With the 65nm CMOS BEOL, it is impossible to avoid high capacitive coupling with a PGS. To conclude, a PGS is not advised in the design of small mmW inductors.

Distance with the substrate:
This part aims at analyzing the effect of the distance separating the inductor strip from the substrate. The PGS is removed to simplify this analysis. To change this distance without modifying the BEOL, it is mandatory to change the number of metal levels in parallel. Thus, the resistance of the inductor strip is modified. Three inductors are simulated:

- A 1^{st} inductor composed by Metal 5, Metal 6, Metal 7 and an alucap level (Ind).
- A 2^{nd} inductor composed by Metal 6, Metal 7 and an alucap level (Ind-without M5).
- A 3^{rd} inductor composed by Metal 7 and an alucap level (Ind-without M5 & M6).

Figure 2.25 plots their L and Q. At frequencies below 30GHz, Ind-without M5 & M6 has the lowest Q. It is due to the high resistive strip compared to the other inductors. When frequency rises, this inductor possesses the highest Q. Indeed, resistive losses become lower than substrate ones. Ind and Ind-without M5 suffer more from substrate losses due to their proximity to the substrate. Consequently, they have a SRF lower than the one of Ind-without M5 & M6.

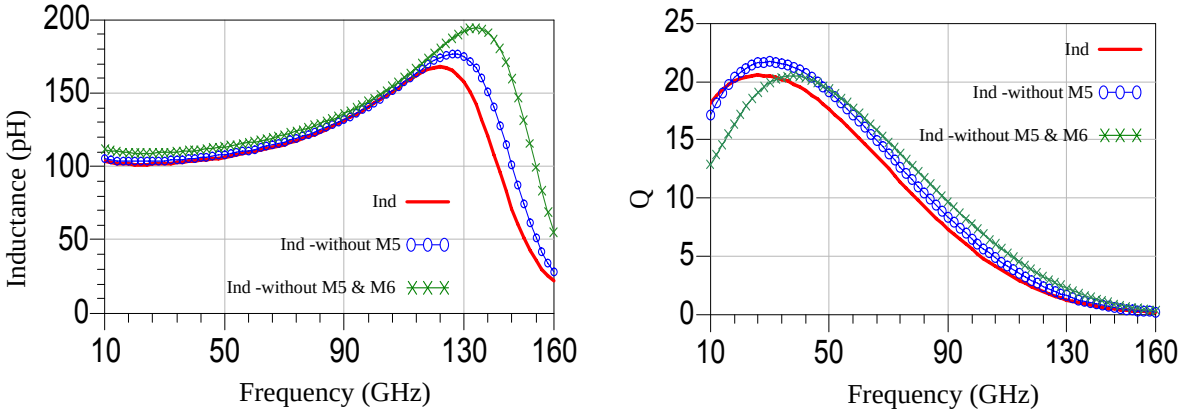


Figure 2.25: Effect of the RF strip design on L and Q at mmW frequencies

Concerning L, Ind-without M5 & M6 exhibits the highest inductance value in all the frequency range. This result is expected because of the low capacitance governed between the strip and substrate. This capacitance participates to reduce the proper inductance. Moreover, this inductor has the thinnest strip that increases the inductance value.

Octagonal inductors are studied and optimized in order to be functional at mmW frequencies. It is demonstrated that Q depends principally on resistive losses at RF frequencies. The combination of low substrate losses and high inductances ($> 1nH$) at RF frequencies makes the PGS advantageous. When growing in frequency, a typical inductance is close to 100pH. The impact of the capacitive parasitics becomes more important degrading both SRF and Q. The PGS is not anymore a solution to improve the inductor performances. Moreover, the inductor strip must be designed only with high metal levels to be as far as possible from the substrate.

2.2.2.2 Square inductor analysis

The main advantage of square inductors is their low area compared to octagonal ones, for a given inductance. Indeed, due to the decoupling of two orthogonal strips, the total inductance is equal to the sum of each inductance strip. This is a correct assumption for big inductors where the negative mutual is negligible compared to positive mutual. Figure 2.19 plots the structure of a square inductor highlighting the current flow direction and the different inductor mutuals. At mmW frequencies, small inductors are required. They can be composed only by one turn. It means that the positive mutual is comparable to the negative one. Thus, the negative coupling can not be neglected anymore.

In this part, we focus on coupling effects of small square inductors (one turn). The calculation

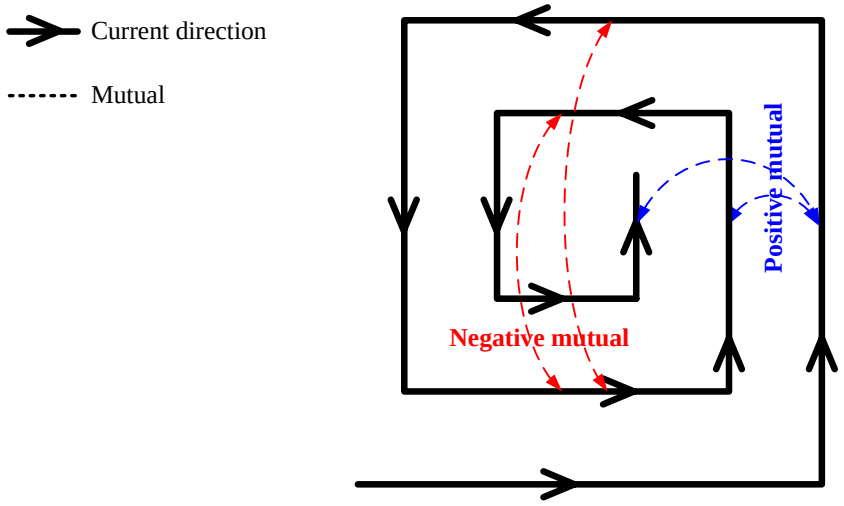


Figure 2.26: Inductive mutuals in a square inductor

of only L and Q of an inductor is sufficient to characterize it but still not enough to predict its behavior in a chip environment. For instance, an uncontrolled return current path in a circuit can induce a gain drop, a frequency shift and interpretation errors.

One turn square inductor is simulated. The skin depth and the substrate conductivity are taken into account. Figure 2.27(a) plots the different currents flowing in the structure. The first return current ($I1$) flows through the path that exhibits the minimum of resistance. It is concentrated around the inductor. The grounding structure has a non-null resistive (R_{gnd}) and a non-null inductance L_{gnd} which are added to the total resistance and inductance. The second current

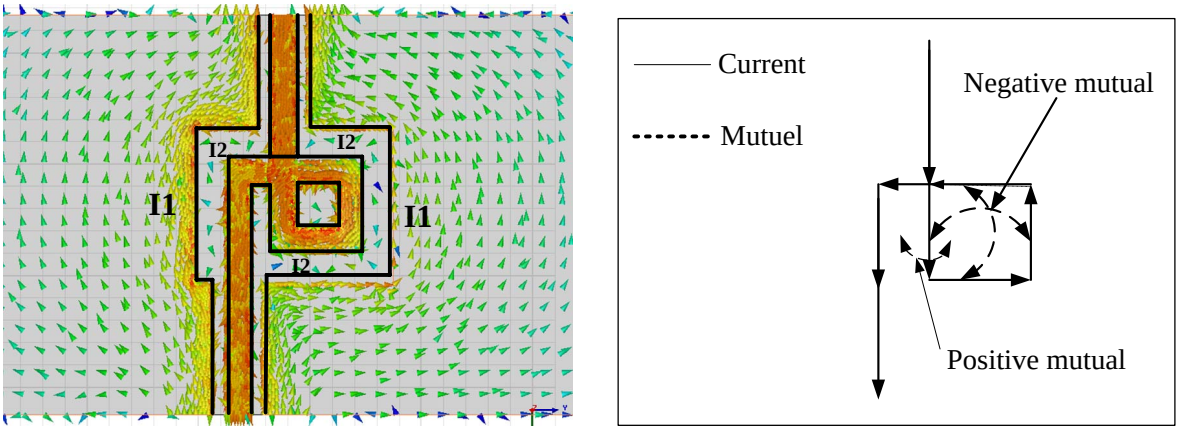


Figure 2.27: Current distribution with illustration of the mutual effect

($I2$) is concentrated in the substrate and it is generated by the capacitive coupling governed by the inductor strip and the ground plan.

The bases of inductor analysis are extracted principally from the integral form of the Ampere's law (Eq. 2.36) and Faraday's law (Eq. 2.37) [95] that monitor the interaction between the electric field and the magnetic field.

$$\oint_C B \cdot dl = \mu \cdot \oint_S (J + \xi \cdot \frac{\partial E}{\partial t}) \tag{2.36}$$

$$\oint_C E \cdot dl = -\frac{\partial \oint_S B \cdot ds}{\partial t} \tag{2.37}$$

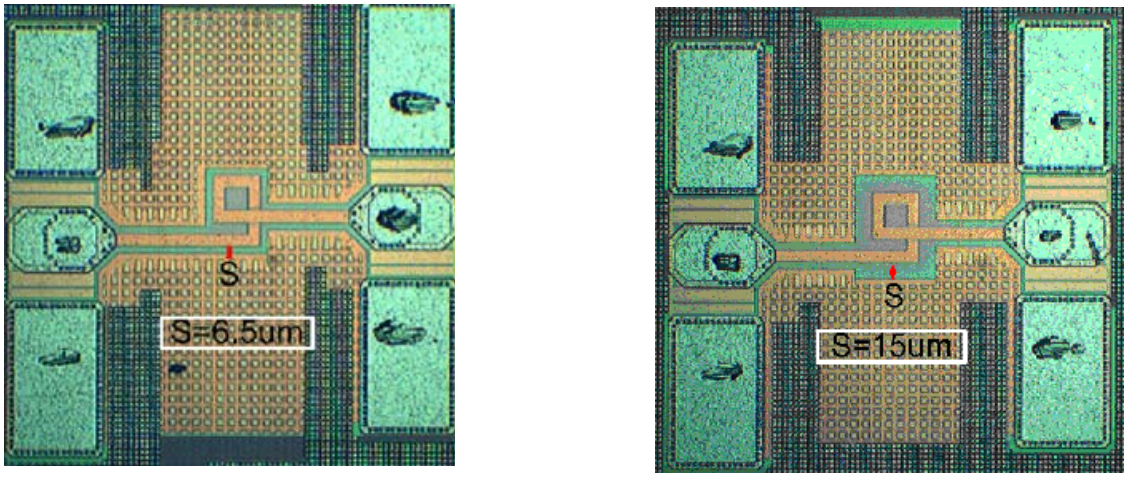
where

- E and B are the electric and magnetic fields respectively,
- C is the contour that encloses the surface S,
- μ is the magnetic permeability,
- ξ is the electric permittivity of the material,

According to Eq. 2.36, the magnetic field is created from an AC electric current and an AC displacement current. The AC electric current is the main current in a structure and it is generally approximated to the total current in the structure. However, at mmW frequencies, the capacitive coupling rises and acts as a return current that reduces the inductance. Thus, the displacement current must be taken into account to estimate the total magnetic field.

According to Eq. 2.37, the variation in time of the magnetic field ($\frac{\partial B}{\partial t}$) generates an induced current in neighbor material called Eddy current. It flows in the opposite direction of the magnetic field generated by it. This phenomena is called the negative feedback. As the electric field is proportional to $\frac{\partial B}{\partial t}$, this effect is more important when frequency rises. The reduction of the magnetic field induces a reduction of the total value of the inductance.

To check the aforementioned comments, 2 one-turn spiral inductors are designed. Figure 2.28 depicts their die photography. They have the same geometry and the same length. The inductor



Square inductor photograpy (S=6.5um)

Square inductor photograpy (S=15um)

Figure 2.28: Die photographies of the two square inductors, $S = 6.5\mu m$ and $S = 15\mu m$

width is w =10μm. The length of each arm is equal to 50μm. The difference between the two inductors consists in the distance (S) separating the RF strip from the ground plan. S is equal to 6.5μm for the left one and equal to 15μm for the right one (Figure 2.28). The ground plan is formed by all metal levels to reduce as possible its intrinsic resistance and inductance.

The two square inductors are measured and depict good agreement between simulation and measurement results (Figure 2.29). The access-line and RF-pad effects are extracted. Instead of an open-short de-embedding method, an open-thru de-embedding method is used to calculate L and Q.

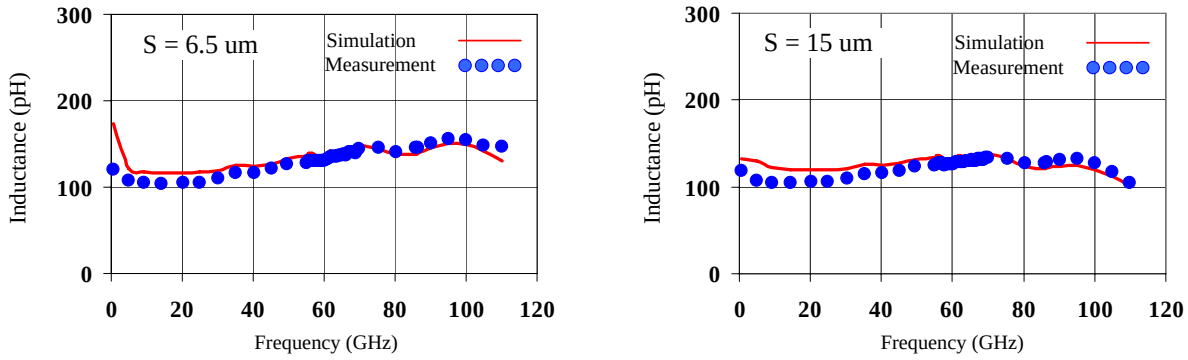


Figure 2.29: Simulated vs. Measured L of the two inductors

Figure 2.30 compares the two measured inductors. Reducing S from 15μm to 6.5μm generates

too much coupling. Thus, the proximity effect is more important. Then, the inductance is reduced by 10%, from 105pH to 95pH. S controls the effective value of the inductor. However, reducing the inductance is at the cost of a high capacitive coupling which reduces both its SRF and its Q.

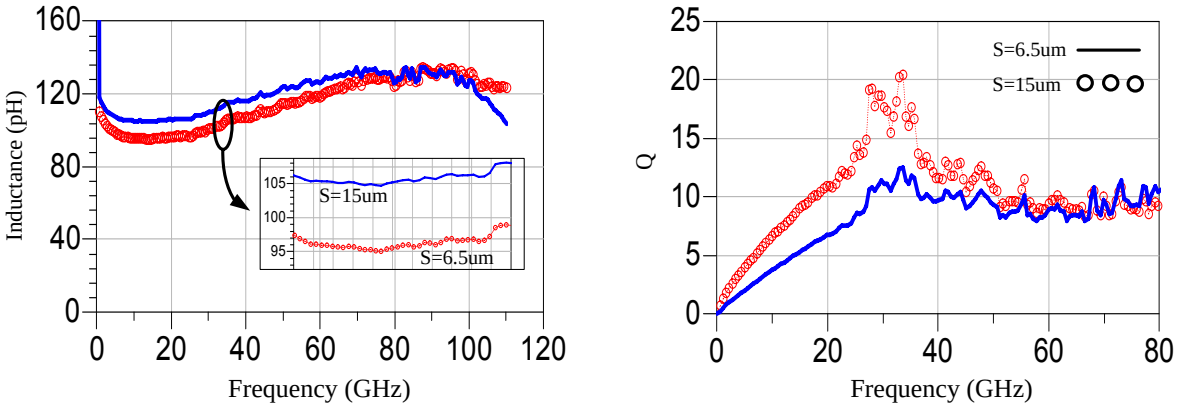


Figure 2.30: The effect of S on L and Q

Square inductors are attractive since they do not consume a large area. Due to their easy customization, they are extensively used at RF frequencies. They exhibit good performances due to the low substrate losses and the low negative mutual coupling. At mmW frequencies, the use of small inductors addresses coupling issues. The return current path can be added as a parameter to customize and to improve a mmW square inductor. The drawback in a square structure is the sudden change in the current displacement in bends. It causes more resistive, capacitive losses and radiation losses at mmW frequencies.

To conclude, octagonal and square inductors are detailed. Q is their FoM. Their customization is presented separately. It is not possible to assert a better one. For octagonal inductors, the PGS and the strip resistivity are the retained parameters for their characterization. For square inductors, only the proximity effect with the return current path is handled. At mmW frequencies, the inductor performances are principally dependent on the mean of their exposition to the substrate. Moreover, due to the small mmW inductors, the chip environment including the ground plan design influences in the inductor performances by the proximity effect and the return current. That is why no preference points on any type of inductors are deduced.

2.2.3 RF-pads

The RF pad is the direct access to the circuit. A first part describes how a typical pad is designed and validated for RF applications. However, its behavior becomes critical at high frequencies. A second part discusses about issues met during the characterization of different customized RF-pads at mmW frequencies. A behavioral modeling analysis of an optimized RF-pad is finally presented and adopted.

2.2.3.1 Pad structure

Integrated circuits are immunized against any external radiation by a nitride passivation layer. It reduces the field leakage thanks to its high permittivity. However, a good contact between the pad and RF probes must be ensured. For this reason, a Copper Bondpad (CB2) which defines an opening (mask) in final nitride passivation is included in the process. The minimum opening of CB2 imposed by STMicroelectronics is $44\mu m$ x $70\mu m$. This constraint sets the minimum pad's top plate size.

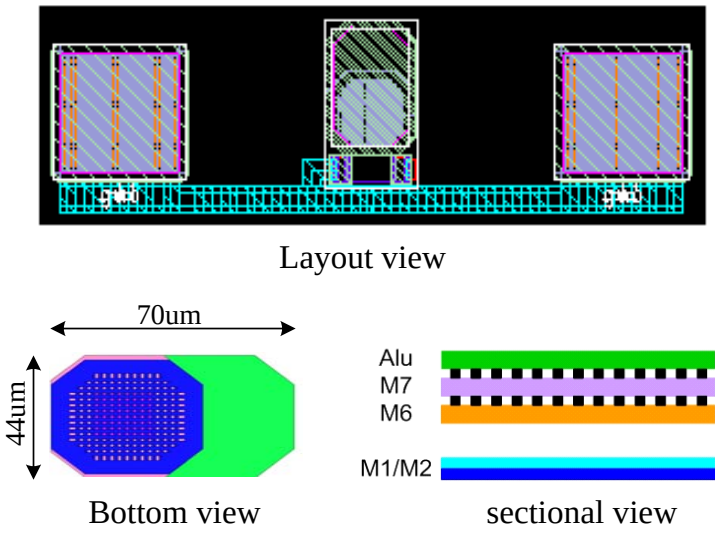


Figure 2.31: RF-Pad structure and layout

Figure 2.31 depicts an octagonal typical contact pad seen by different views. The top plate of the pad capacitor is formed by the top metal levels (Metal 6, Metal 7 and alucap). The bottom plate representing the solid metal shield is formed by Metal 1 and Metal 2. The ground pads are placed away from each other at 150μm (center-to-center) to respect the pitch of the RF probes. The bottom plate of RF pad and the ground pad are connected with long line designed in Metal 2.

Moreover, it is extremely important to pay attention to Electro-Static Discharge (ESD) protection in the circuit design. Hence, an ESD protection device is integrated to the RF pad to protect IC against ESD damages. The ESD protection circuit schematic is drawn in Figure 2.32. It is mounted as a power clamping device between the supply voltage VDD and the RF pad [96] [97]. During normal operation, the ESD circuit has a transparent behavior as it presents a high parallel impedance to the circuit (50Ω). During an ESD event, the input signal achieves much higher values than VDD. Then, the ESD circuit presents a low impedance path to discharge current and to isolate the circuit.

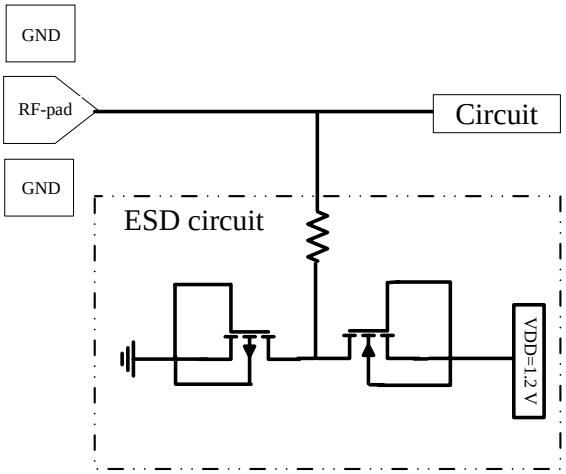


Figure 2.32: ESD circuit schematic

2.2.3.2 Pad response

Pad measurements are performed from 1GHz to 20GHz and from 20GHz to 110GHz. Figure 2.33 plots the previously described input capacitance and Q of the RF-pad. From 1GHz to 20GHz, the pad acts as a capacitor of 130fF with a Q decreasing from 70 to 5. The capacitance value is slightly decreased because of the skin depth effect. The current is concentrated in the pad edges and not in the overall RF-pad area reducing the capacitance. This RF pad can be used for applications below 20GHz.

Nevertheless, the RF-pad does not keep the same behavior at frequencies higher than 20GHz. The capacitance resonates at 70GHz and acts as an inductor. The RF-pad must be used at frequencies lower than 70GHz. At mmW frequencies, the capacitance of the pad is not the only parameter to be mentioned. Consequently, lumped model is developed to highlight the most important elements which cause the resonance (Figure 2.33).

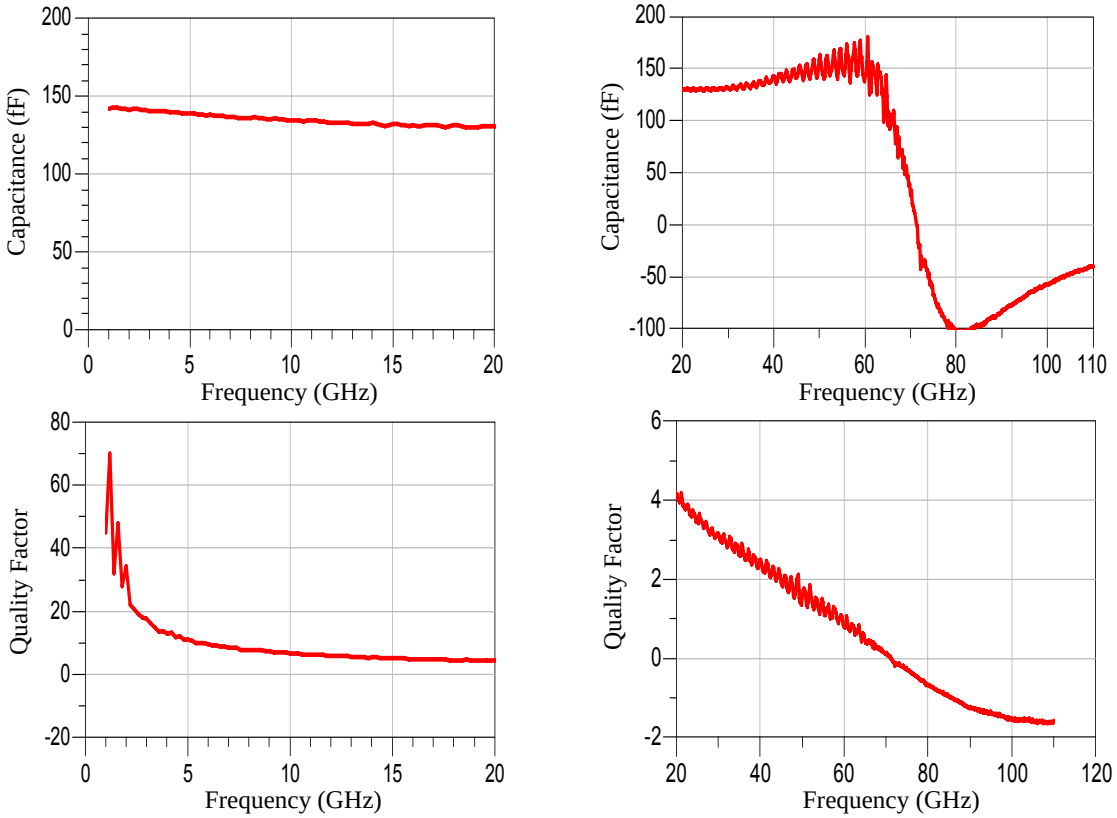


Figure 2.33: RF-pad behavior (C_p and Q) at f$\leq$ 20GHz and at f$\geq$ 20GHz

According to the pad model, the resonance is caused by a LC combination. Several RF-pads are designed and measured in order to control separately the effect of each element. This paragraph details the intrinsic parasitic elements located in the RF-pad structure namely the intrinsic capacitance and the intrinsic resistance.

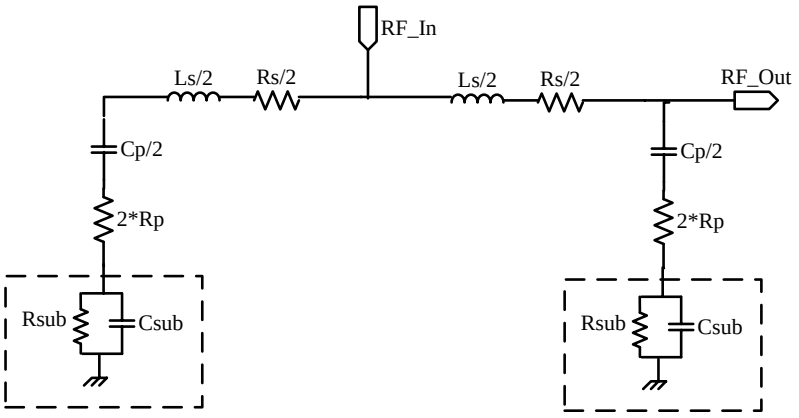


Figure 2.34: An improved RF-pad lumped model

- **Intrinsic capacitance**
  - The RF-pad capacitance: the pad is composed by the top metals (Metal 6, Metal 7 and alucap) and the bottom metals by (Metal 1 and Metal 2). Because of the low thickness of the BEOL, the DC capacitance achieves $80fF$. In addition to that, the accesses to the ground pad is routed only by Metal 2 which increases the capacitance with the substrate. The total capacitance achieves $140fF$.
  - The parasitic capacitance of the ESD circuit: at high frequency, typical ESD induces capacitive parasitics generating substrate noise coupling. The total capacitance caused by ESD is extracted by Cadence extractor. It is equal to $12fF$.
- **Intrinsic inductance**
  - The RF pad inductance: an intrinsic inductance is located in the RF path. It must be considered at mmW frequencies. Its value does not exceed 30pH.
  - The parasitic inductance of the ground path: the path from RF-pad grounds to the ground probes is ensured by a thin Metal 2 which exhibits an additional inductance.

Those inductors are added to the effective capacitance of the pad and contribute to the resonance. A first order model determines the first resonance (Eq. 2.38).

$$F_{res} = \frac{1}{2\pi \cdot \sqrt{LC}} = 75GHz_{Simu} \approx 70GHz_{Meas} \tag{2.38}$$

2.2.3.3 Optimized pad design

Firstly, the pitch is reduced from $150\mu m$ to $100\mu m$. In fact, the resonance is directly related to the length of the access path. It reduces both inductive and capacitive parasitics. The resonance frequency is shifted from 70GHz to 100GHz (Figure 2.35).

The first pad is composed by the top metals (Metal 6 or Metal 7 and alucap) and by the bottom metals (Metal 1 and Metal 2) representing the solid metal shield. The main motivation of this design is the reduction of the substrate coupling and the improvement of Q. This configuration suffers from capacitive coupling losses because of the low thickness of the BEOL. Indeed, this solution is adopted in a Bi-CMOS BEOL where a shunt T-line stub resonates with the RF-pad capacitance [98]. To minimize the intrinsic capacitance, a method consists in realizing a deep trench, etching a deep groove in a silicon substrate. This solution adds extra process during the IC fabrication. Thus, it is not adopted for our design because of its cost.

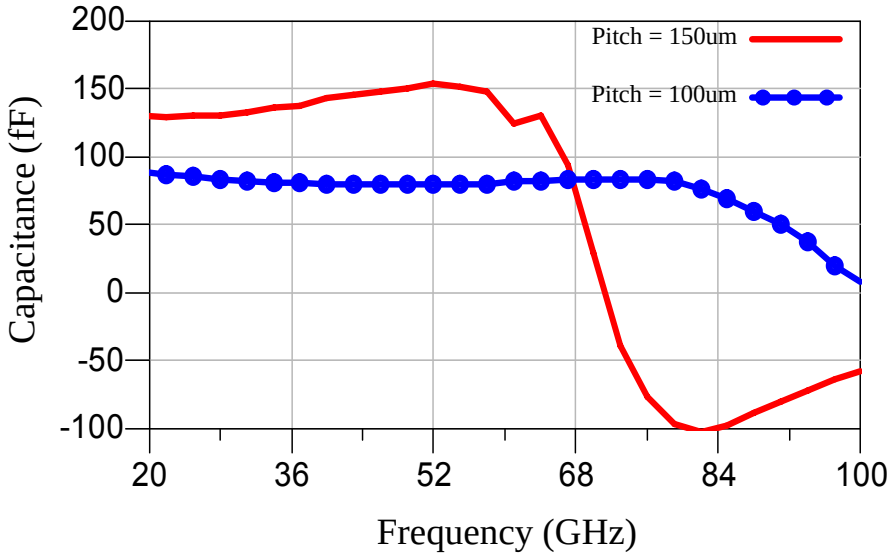


Figure 2.35: The effect of the pitch on RF-pad resonance

An investigation is brought to determine the impact of the substrate in the RF-pad design. The bottom metals are removed and the RF-pad is exposed to the silicon substrate to support that characterization. Only Metal 7 and alucap are used as a top plate to obtain the minimum capacitance. It reduces the capacitance by a ratio of 43%. Figure 2.36 depicts the two octagonal contact pads.

The two pads are sent to foundry. Figure 2.37 depicts simulation results and measurement results of their intrinsic capacitance, from DC to 110GHz. The intrinsic parasitic capacitance (C_p) of the shielded (Sh) RF-pad varies from 45fF to 40fF (11%). Whereas, the C_p of the non-shielded (NSh) RF-pad varies from $30fF$ to $15fF$ (50%). Nevertheless, for frequencies beyond 55GHz, the NSh RF-pad presents almost the same C_p value and is equal to $16fF$. This pad has a quasi-constant capacitance and can be used for the most important mmW applications which are centered at 60GHz, 77GHz and 94GHz.

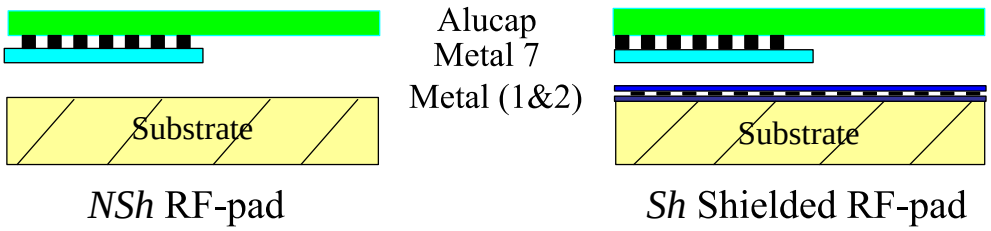


Figure 2.36: The structures of a Sh RF-pad and a NSh RF-pad

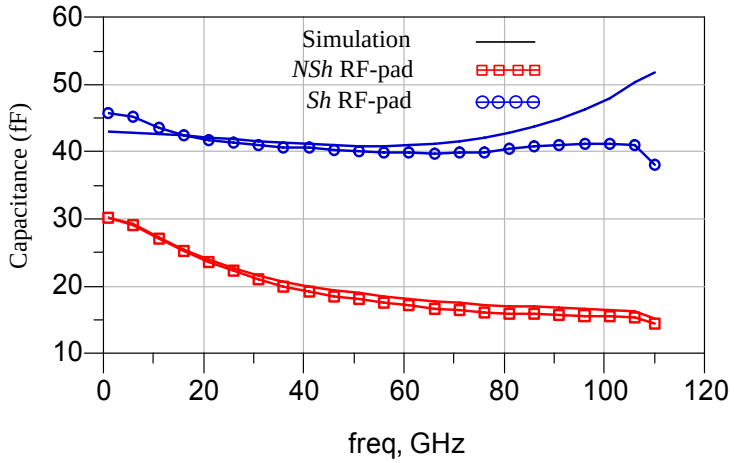


Figure 2.37: Measured and simulated capacitance of RF-pads

Investigating to lower C_p has an important effect in the design of PAs, LNAs or VCOs. For instance, at $60GHz$, the input and the output impedances are deviated from 50Ω to $Z_{1pad} = (42 - j * 9)\Omega$ for the NSh RF-pad and is drastically deviated to $Z_{2pad} = (15 - j * 13)\Omega$ for the Sh RF-pad (Figure 2.38). In fact, the impedance deviated by the Sh RF-pad is closer to the input impedance of the transistor (around 10Ω) than the impedance deviated by the NSh RF-pad. This behavior is advantageous for the matching in the design of single-function circuit. Nevertheless, the ultimate goal of mmW applications is to design fully integrated transceivers.

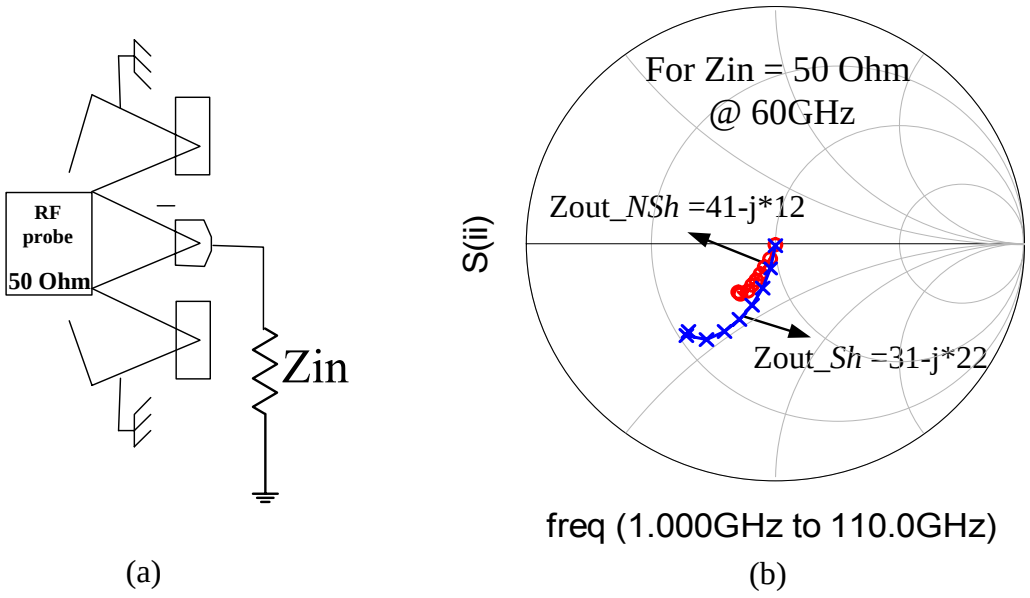


Figure 2.38: The impact of a RF-pad pattern shield on impedance matching and losses

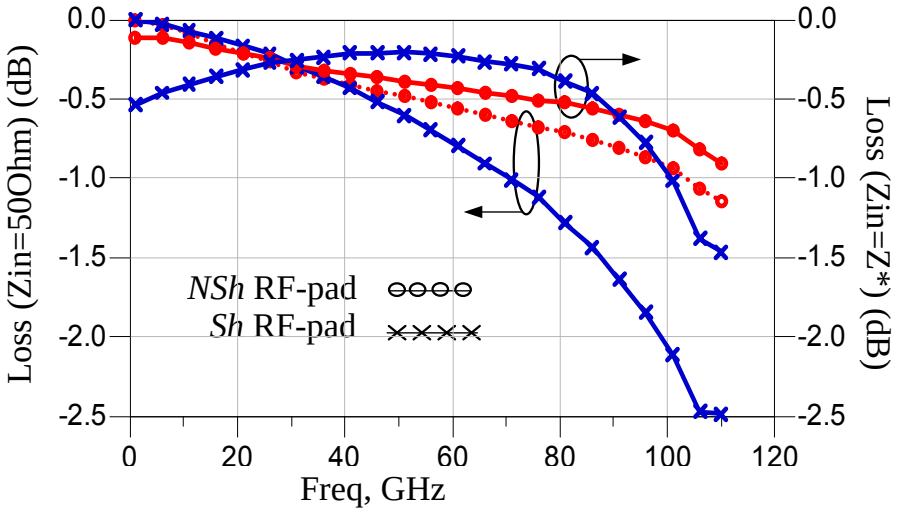


Figure 2.39: The impact of a RF-pad pattern shield on circuit mismatch and losses

Consequently, high-loss passive devices are required and must be added for each circuit to match every stage to 50Ω in the transceiver design. That drops the total gain of the transceiver.

The insertion loss is shown in Figure 2.39 to quantify the effect of the mismatching caused by the RF-pad. At 80GHz, when the input impedance $Z_{in} = 50\Omega$, the attenuation reaches $1.3dB$ for the Sh RF-pad and only $0.7dB$ for the NSh RF-pad. If $Z_{in} = Z_{in}^{*}$ (conjugate impedance), the NSh RF-pad causes more attenuation ($0.5dB$ vs. $0.3dB$). This result is expected because of the substrate losses which increase more rapidly than the conductor losses at high frequencies.

This work has been published in [99] and [100]. Table 2.2 summarizes positive and negative behaviors of Sh RF-pads and NSh RF-pads in 65nm CMOS technology.

Table 2.2: Sh RF-pad vs. NSh RF-pad

	Sh RF-pad	NSh RF-pad
Simplicity of modeling	++	-
Metallic losses	-	+
Substrate losses	+++	–
Quality factor	++	-
Matching	-	++

To conclude, the choice of the pad depends on the design outlooks. The *Sh* RF-pads is well advised for a stand-alone design of PA when the final purpose is not to design a fully transceiver. Due to its higher capacitance, the matching between both two elements is difficult and any additional matching network must be added. Moreover, the use of the *Sh* RF-pads can be restrictive to characterize transistors. Indeed, it is not possible to cover the overall Smith chart during load pull measurement to determine the desired impedance after de-embedding procedures.

However, the *Sh* RF-pads do not suffer from substrate losses and benefit from higher Q compared to the NSh RF-pads. In our work, the NSh RF-pad is chosen since our goal is to design the overall transceiver.

2.3 Conclusion

This chapter aims at certifying an optimized 65nm CMOS DK from STMicroelectronics library listing behavioral models before designing a 60GHz PA. This work is focused on passive device modeling.

A first investigation is brought into play to perform rapid EM simulations for 65nm CMOS BEOL. In fact, the challenge in CMOS technology design is to take into account a maximum of high frequency considerations to identify critical parameters during the characterization. Moreover, calibration and de-embedding methods are detailed to make an appropriate comparison between simulation and measurement results.

A second investigation reviews passive device characterization and their optimization. A particular interest focuses on basic elements namely, T-lines, inductors and RF-pads. This part is organized in three sections.

- **T-lines**: this section describes different T-lines topologies. MS lines and CPW lines are retained and compared in the context of a PA design. It reviews their electric performances and also non-common aspects as coupling issues. The CPW line is chosen for PA design. The MS line takes advantage on taking off the substrate effect during the design. Furthermore, MS lines suffer from high capacitive coupling and require a large die area to be isolated from neighbor elements. The analysis of the adopted CPW line is confirmed by depicting a good agreement between simulation and measurement results. A 50Ω $(w, G) = (10\mu m, 6.5\mu m)$ CPW line exhibits an attenuation of $1.6dB/mm$ at 60GHz.

- **Inductors**: this section reviews two types of inductor namely octagonal and square inductors.

  - Octagonal inductors: they are available in the 65nm CMOS DK from STMicroelectronics. They are analyzed by adopting Q as a major FoM. It is proved that the resistive losses impact at RF frequency whereas losses due to the capacitive coupling impact at mmW frequencies. Consequently, their performances are improved by suppressing the PGS and the low metal levels which compose the inductor strip. Indeed, the PGS is responsible for high capacitive coupling reducing Q and SRF. Moreover, the inductor strip must be designed only with high metal levels to be as far as possible from the substrate.
  - Square inductor: they are proffered for low cost production since they occupy a compact die area. This advantage becomes an issue at mmW frequencies. Indeed, the negative mutual becomes comparable to the positive mutual making hard the design of high Q inductors. This phenomenon is observed in the return current when the distance between the RF strip and the ground plan is varied. In addition to that, orthogonal bends increase the total resistance of the strip degrading Q. Q_{max} is equal to 12 which is comparable to the Q of T-lines.

  Those inductors have a similar Q and area at mmW frequencies. The purpose of this part is not to choose one type of inductor. It aims at understanding critical parameters and their losses mechanisms.

- **RF-pads**: this section details the impact of RF-pad at mmW frequencies. Both traditional and optimized RF-pads are presented and measured. The goal is to model them and to consider any parasitic elements. Two structures are proposed, simulated and measured: a Sh RF-pad and a NSh RF-pad. The Sh RF-pad exhibits a high capacitance of $40fF$ with a Q of 12 at 60GHz while the NSh RF-pad exhibits only $17fF$ at 60GHz. However it suffers from a low Q. The RF-pad design is face to a low C_p and a high Q trade-off. The choice of a RF-pad depends on the targeted application. The Sh RF-pad is advised for a stand-alone design while the NSh RF-pad is advised for designing a fully transceiver.

The low resistivity of the substrate and the small thickness of the 65nm CMOS BEOL degrades potentiality passive device performances at mmW frequencies. T-lines and inductors exhibit high losses. T-lines have a low Q of 12. Inductors keep better performances after optimization and consume a smaller area compared to T-lines. However, their analysis is more complex and generates more coupling issues than T-lines. Those issues are also valid in the RF-pad design.

Resistors and capacitors are not detailed in this chapter since we adopt the available ones in the 65nm CMOS DK from STMicroelectronics.

chapter 3 focuses on active device to complete the 65nm CMOS DK from STMicroelectronics dedicated to 60GHz PA design. 2 PAs are presented when using the T-lines and a second one using inductors.

Chapter

3

60GHz PA Design

Contents

Chapter 3 discusses firstly about key design procedures for a generic mmW PA. Secondly, additional considerations are noticed according to some issues met during the design of preliminary PAs. Next, two 65nm CMOS PAs are described, sent to foundry and fabricated. The two PAs are designed with different topologies. Their respective simulation and measurement results are exposed. A critical point of view of the fabricated PAs is given to further improve their performances. The functional PAs are compared with the ones found in literature which target the 60GHz WPAN standard. Finally, promising future works are briefly presented.

Key words: 65nm CMOS PA design, load pull measurements, impedance matching, stability, baluns.

3.1 Introduction

The previous work details passive device characterization to improve the 65nm CMOS DK library dedicated to 60GHz IC design. This chapter focuses on the design of 60GHz PA. This part highlights the design methodology before presenting PAs realizations.

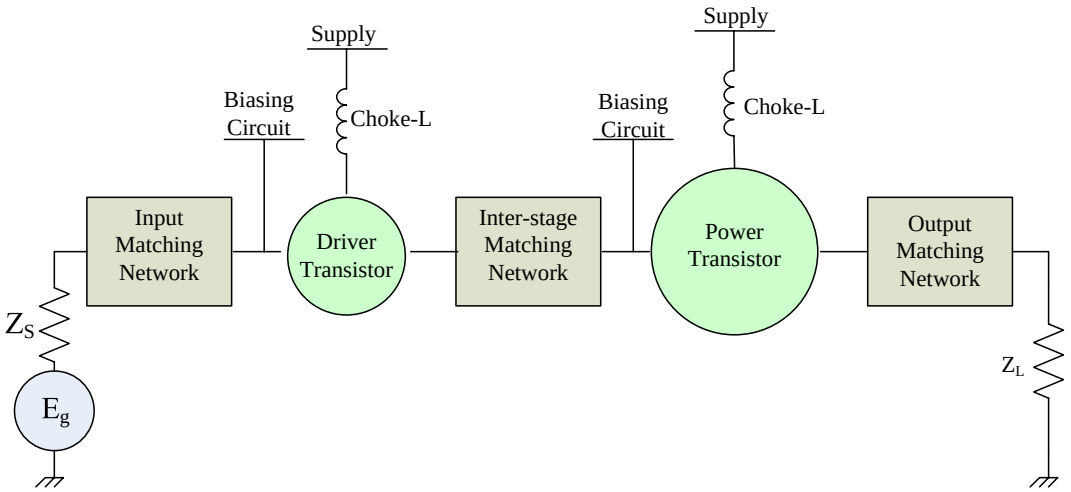


Figure 3.1: Generic PA structure

Figure 3.1 depicts a generic PA composed by a power stage, driver stages (only one driver stage is plotted), biasing circuits, supplies and matching networks:

- **The power transistor:**
  It is responsible for providing a required P_{out}. The power transistor represents the most critical element in a PA design. Indeed, a high current and a high dissipated power are concentrated in the power transistor area. For linear PAs, the power transistor must respect linearity and PAE specifications. The challenge in mmW CMOS technology design is not only to provide a high P_{out} by the power transistor, its gain must be reasonable to decrease the linearity constraints of the driver stage.

- **The driver transistor:**
  It allows improving the gain of the PA. Thanks to the power transistor gain, linearity constraints of the driver stage are less important than the ones of the power transistor.

- **Biasing circuit:**
  The choice of biasing voltage is set according to the required conditions for a desired operating class. The biasing circuit must be stable in temperature to maintain a constant DC operating point. Choke inductors ($Choke - L$) are used at RF frequencies to isolate the transistor from any supply voltage fluctuation. The higher $Choke - L$ value is, the more efficient the role is. Moreover, $Choke - L$ allows having drain voltage swing from 0V to 1*Vdd. At mmW frequencies, low values of $Choke - L$ are designed on-chip to participate at performing impedance matching.

- **Matching networks:**
  They allow the transformation impedance from Z_1 to a desired Z_2. Typically, the output matching network induces 1dB of losses. Inter-stage and input matching exhibit less losses. The design of multiple stages represents a mean to compensate matching network losses and to keep high PA gain. Unfortunately, this solution is at the cost of a high power consumption and thus a low PAE. Indeed, CMOS technology suffers from low intrinsic gain. So, a trade-off between the number of stages and PAE must be found.

The following parts present the main elements of a PA. They are accurately analyzed during PA design methodology demonstration.

3.2 PA design methodology

The design of *mmW* PAs does not change fundamentally from RF PAs design. The design flow is almost the same. It requires paying more attention to particular points such as:

- The intrinsic frequency performances of transistors,
- The model availability and parasitic considerations at *mmW* frequencies,
- The high sensitivity of PA performances with transistors and passive devices layouts.

Figure 3.2 illustrates the supported 60GHz PA design methodology. The architecture of the PA must be set at the beginning. Contrary to a typical design of a LNA or a filter for instance, PA design progresses from the output toward the input. Hence, The design of the power stage is done before the design of the driver stage. The PA design steps are detailed as follows:

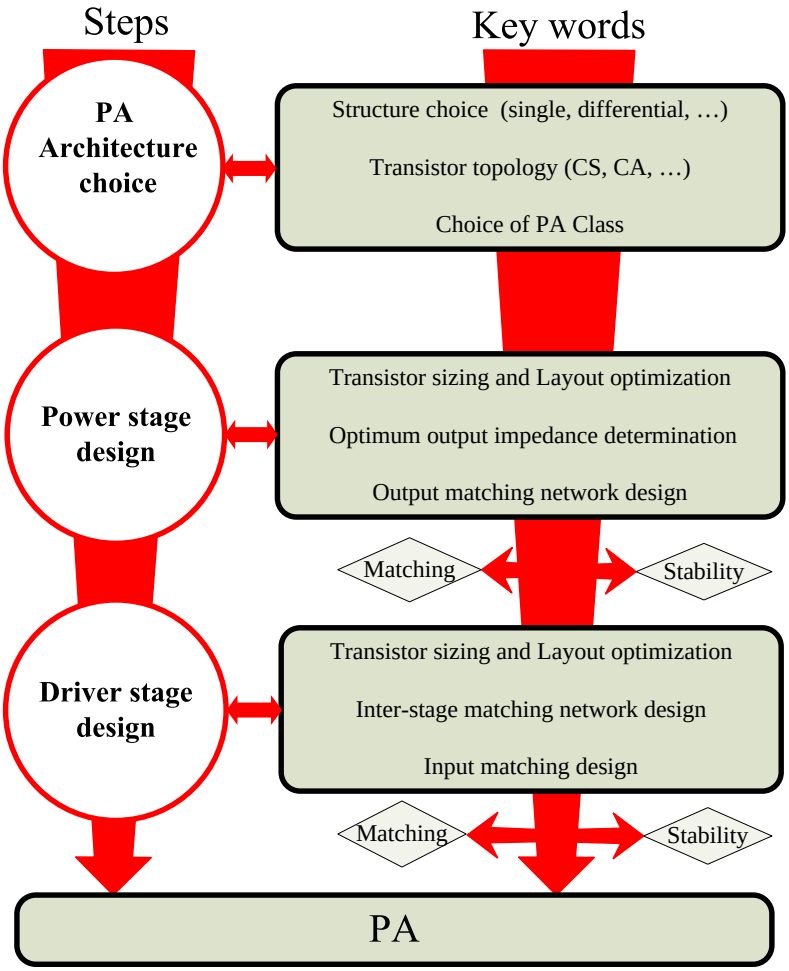


Figure 3.2: A *mmW* PA process flow diagram

3.2.1 PA architecture choice

It is the 1*st* step in the PA design. The meaning of PA architecture is not limited here to only a system analysis. It concerns the system and transistor topologies. It is divided into three parts:

- PA structure choice,
- Transistor topology,
- Classes of PA Operation.

3.2.1.1 PA structure choice

In a typical transmitter, PAs are implemented between a mixer and an antenna. The input excitation of a PA is set as a function of the mixer output whereas its output depends on the excitation nature of the antenna. Then, the architecture of the PA depends on system requirements. There is more flexibility in a stand-alone design where the purpose is to realize firstly an operating PA. The fundamental PA topologies are: single-ended, differential and balanced [101].

Figure 3.3 plots a simplified block diagram of each topology. The main difference consists in the way in which the signal phase passes through the PA. Each topology exhibits its own advantages and drawbacks. Table 3.1 summarizes positive and negative points of those three topologies.

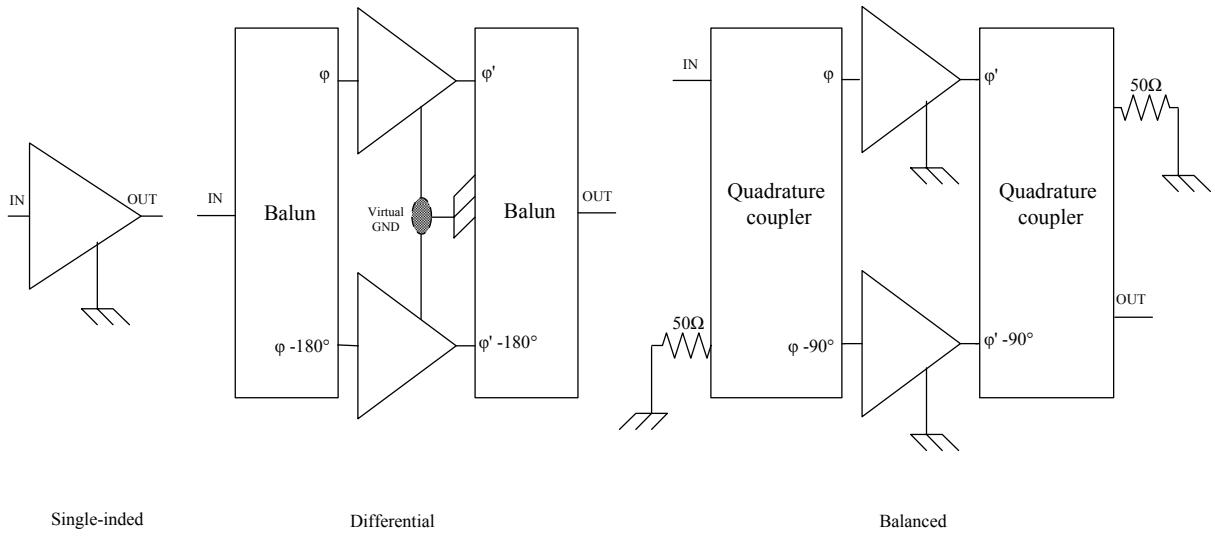


Figure 3.3: Different PA architectures

Table 3.1: Comparison between PA architectures

	Advantages	Drawbacks
Single-ended	Easy design Small area	Sensitive to ground connections Stability issues
Differential	Less sensitive to ground connections No need for coupling capacitors	Require two baluns (losses) Stability issues Large area
Balanced	Less sensitive to mismatch Good stability Good phase linearity	Sensitive to ground connections Requires two quadrature couplers (losses) Requires two 50Ω resistors Large area

Single-ended structure is firstly adopted because of its simplicity. Indeed, this structure is recommended to validate a 1st 60GHz PA realization.

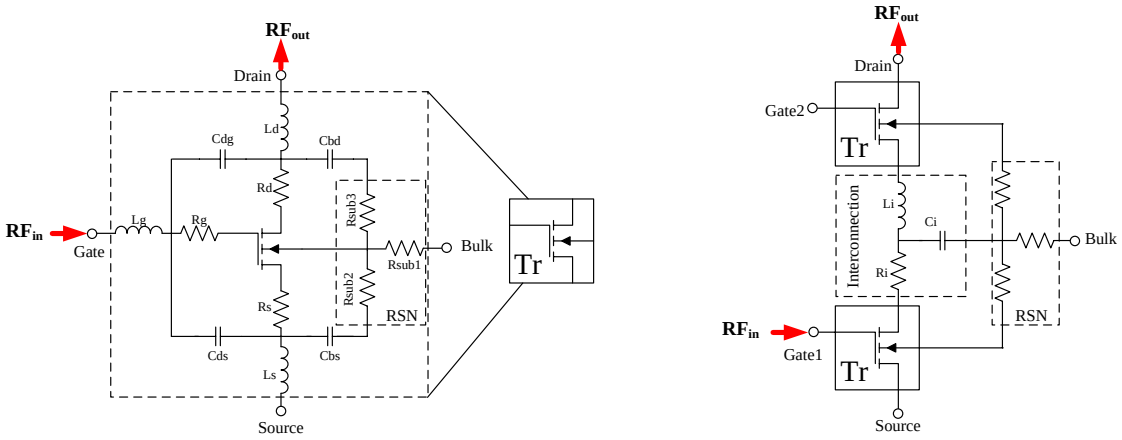
Differential structure adds few constraints because it requires the design of baluns. This topology is also adopted in our design. The baluns perform mode conversion and also impedance matching to limit the PA die area.

Nevertheless, in spite of promising linearity performances of the balanced topology, a quadrature couplers are required. They are typically designed with cumbersome T-lines causing high losses.

3.2.1.2 Transistor topology

The two basic transistor topologies used in PA design are CS structure and CA structure. Their equivalent circuits are plotted in Figure 3.4. Each transistor model is composed by the intrinsic transistor core based on BSIM4 model and extrinsic parasitics modeled by lumped elements.

The intrinsic model of the transistor is calculated with non-quasi-static assumptions instead of quasi-static assumptions to be more accurate at mmW frequencies. BSIM4.6.0 MOSFET model user manual details the model extraction [102]. At RF frequencies, the extrinsic elements effects can be neglected without significant response changes. However, neglecting extrinsic parasitics at mmW frequencies induces significant errors in the transistor response. The extrinsic parasitics are modeled with ideal lumped elements which are dependent on the transistor layout.



(a) CS structure (b) CA structure

Figure 3.4: Equivalent circuit of a CS and a CA structure

Parasitic resistances (R_g, R_d and R_s), parasitic capacitances (C_{gs}, C_{gd}, C_{db} and C_{bs}), inductances (L_g, L_d and L_s) and resistive substrate network (RSN) are added in the transistor model [103]. The method of extraction of each element will be detailed in section 3.2.2.

CS structure:

The CS structure has a low Z_{out}, a low transconductance (g_m) and serious stability issues. Indeed, the Miller capacitance C_{gd} degrades the voltage gain and causes a poor isolation between the input and the output. Moreover, low resistive RSN causes a double issue: in one hand, mmW frequency signal is absorbed in the substrate dropping the gain, in the other hand, the RSN represents a possible path from the output to the input that reduces the isolation between the input and the output. The main advantage of this structure consists in a high voltage excursion from knee voltage (V_k) to 2Vdd at the output of a class A PA achieving high linear P_{out}. In addition to that, designing a CS structure is simple and does not consume a large area.

CA structure:

The CA structure has a higher gain and a higher output impedance. Consequently, the output matching network causes less losses than the one in a CS structure. Moreover, the isolation between the input and the output is improved. Those benefits are affected by the frequency rising. In fact, the CA device is more sensitive to parasitics, especially to the interconnection node between the two transistors. Its own capacitance (C_{in}) absorbs mmW frequency signal dropping the total gain. At 60GHz, its available gain becomes equal (if not lower) than a CS device [104]. two solutions are adopted in few works:

- One solution consists in merging two transistors making a shared junction (shared substrate). This solution changes the intrinsic layout of the transistor and requires a specific study [104]. Nevertheless, the CA structure still has a parasitic capacitance affecting the gain.

- A second solution consists in adding an interstage matching between the two transistors [105]. This solution requires an accurate matching design and consumes a larger area.

The CA structure is also sensitive to the connection between Gate2 and the biasing circuit. In addition to those issues, this structure has a lower voltage excursion from $2*V_k$ to 2Vdd at the output of a class A PA suffering from low linearity.

Table 3.2 gives the most adapted structure (CS or CA) according to the design constraints at mmW frequencies:

Table 3.2: Comparison between CS and CA structures

	Simplicity	Stability	Linearity	Gain	Output power
Most adapted structure	CS	CA	CS	Similar	CS

The CS structure is chosen because of its high linearity performances and also for its design simplicity (for a $1st$ realization) compared to the CA one. A CA transistor is promising to design a driver stage to improve the total gain of the PA.

3.2.1.3 Choice of PA Class

The PA operating class is controlled by biasing conditions. Biasing is adjusted as a function of the system requirements. OFDM modulated signals are chosen for the 60GHz WPAN standard to achieve high data rate communication system. It requires a linear PA operating in class A. This class of operation is characterized by a continuous conduction of the active device and thus, it suffers from low PAE. The class AB is an alternative if the power/efficiency trade-off is not sufficient in class A operation. The choice of the class is not definitive. Size and frequency performances of transistors and losses of matching network drive the biasing too. As a result, DC conditions progress with the design.

3.2.2 Power stage design

The 2*nd* step consists in designing the power stage. It is the most challenging step because the power stage is the most current hungry. Consequently, inaccurate design causes a significant damages. This step focuses on the transistor performances in terms of frequency and gain. Its layout is also critical since it affects its performances. Finally, the transistor must operate at the optimum required regime to achieve a good trade-off between linearity, gain and PAE. This part is divided into three parts as follows:

- Determination of frequency and gain performances,
- Transistor sizing and layout optimization,
- Optimum Load Resistance Determination.

3.2.2.1 Determination of frequency and gain performances

The most important parameters that characterize frequency and gain performances of a transistor are the cut-off frequency (f_t) and the maximum frequency of oscillation (f_{max}).

f_t is defined as the unity current gain frequency. It depends strongly on the dimensions of technology node and depends less on layout parasitics (Eq. 3.1) [106]. Scaling-down CMOS process from 130nm to 45nm improves f_t from 120GHz to 300GHz (cf. Figure 3.5).

$$f_t \approx \frac{g_m}{C_{gs} + C_{gd}} \tag{3.1}$$

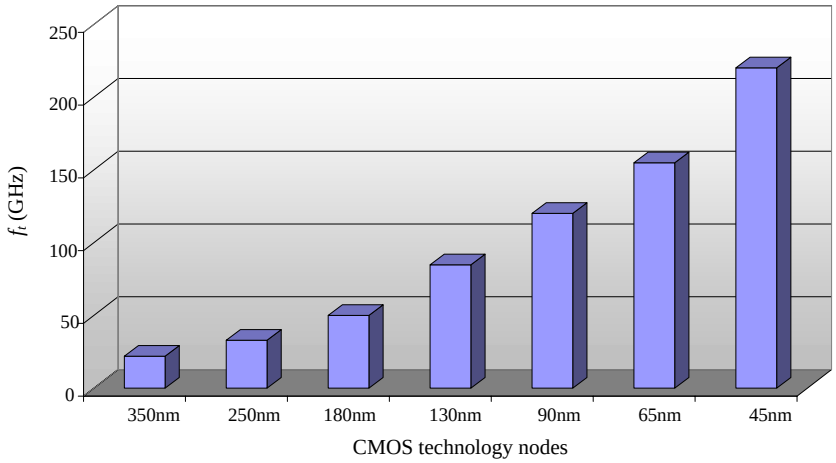


Figure 3.5: f_t enhancement with technology evolution

f_{max} is defined as the unity power gain frequency that gives the limit of use in frequency of an active device. It is proportional to f_t but it is hardly affected or improved by the transistor layout. The most critical parameter is R_g (Eq. 3.2).

$$f_{max} \approx \frac{1}{2} f_t \sqrt{\frac{R_{ds}}{R_g}} \tag{3.2}$$

The next paragraph demonstrates how the transistor sizing and layout influence those two parameters.

3.2.2.2 Transistor sizing

A big power transistor is required to provide high P_{out}. However, the relation between P_{out} and the transistor width (W_T) is not linear. Losses and complexity of modeling are also increased with W_T. In addition to that, a bigger transistor is more sensitive to impedance values seen at the input and the output [62]. A small shift of those impedances drops the transistor gain.

In a first time, W_T is estimated according to the desired P_{out} and the current density (J_c) in the transistor. P_{out} is voltage supply driven ($P_{out} \propto Vdd$), Z_L is calculated from Eq. 3.3. The amount of current swing is determined by P_{out} and Z_L (cf. Figure 3.6).

$$P_{out} = \frac{V_{peak}^2}{2Z_L} = \frac{(Vdd - V_k)^2}{2Z_L} \tag{3.3}$$

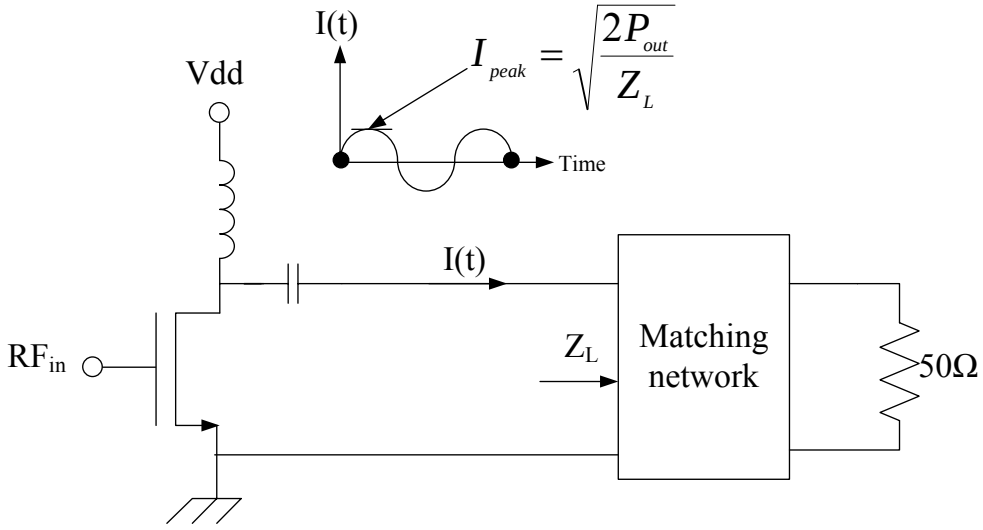


Figure 3.6: Maximum power delivered to Z_L

Consequently, Z_L and I_{peak} are respectively equal to 12.25Ω and 29mA to achieve 10dBm of P_{out} for a V_k) of 0.5V. In class A biasing, I_{peak} is approximated to I_{DC}. Consequently, W_T and J_c are the two parameters to be optimized to set DC point conditions.

As mentioned before, W_T is not definitively set. The final configuration of the power transistor is modified after the determination of its following own three parameters, namely the finger width (W_F), the number of fingers (N_F) and the number of transistors (cells) in parallel (N_C) (cf. Figure 3.7).

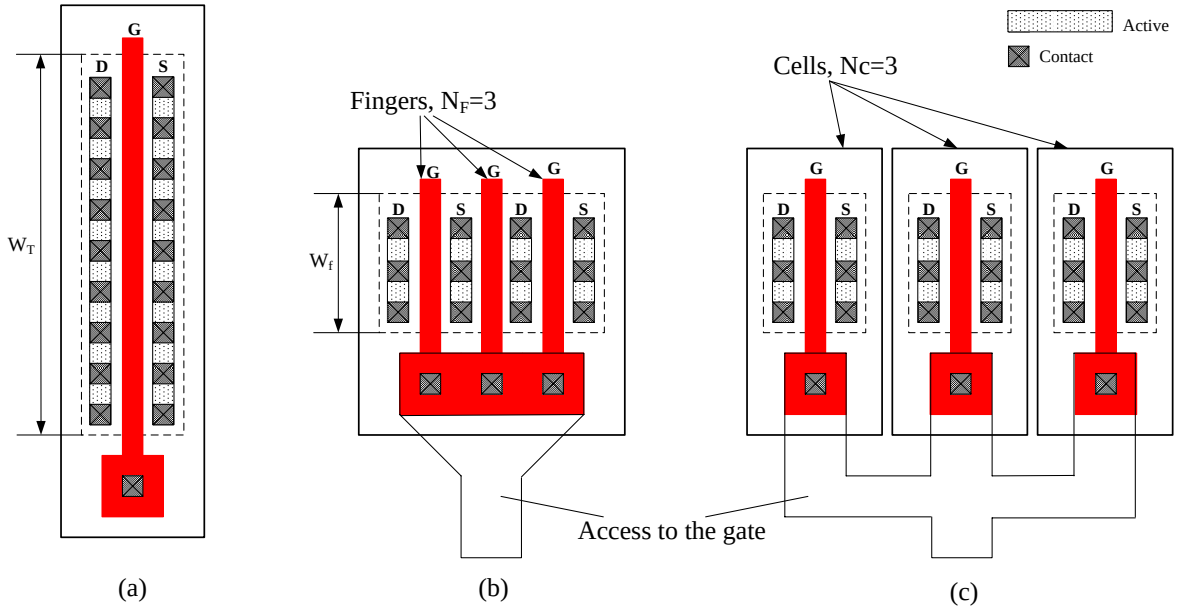


Figure 3.7: Different configurations for the same W_T

- W_F: down-scaling in technology leads to design transistors with narrow fingers. Hence, an improvement of the gain and a limitation in the power capability are noticed. Moreover, CMOS transistor must be designed with short fingers to be functional at mmW frequencies. Indeed, W_F affects directly the gate serial resistance responsible for the degradation of f_{max} (cf. Figure 3.8). Decreasing W_F from $7\mu m$ to $1\mu m$ leads to improve f_{max} from 50GHz to 180GHz. Our transistor realizations have a W_F=1 μm to keep high performances at 60GHz.

- N_F: in one hand, W_T must be high to reach a high P_{out} level. In the other hand, W_F must not exceed $2\mu m$ (cf. Figure 3.8). Hence, it is necessary to design transistors with high N_f. The transistor is divided into N_F fingers to reduce the serial resistance of the gate. The maximum N_f must be reasonable to avoid additional layout parasitics. In addition to

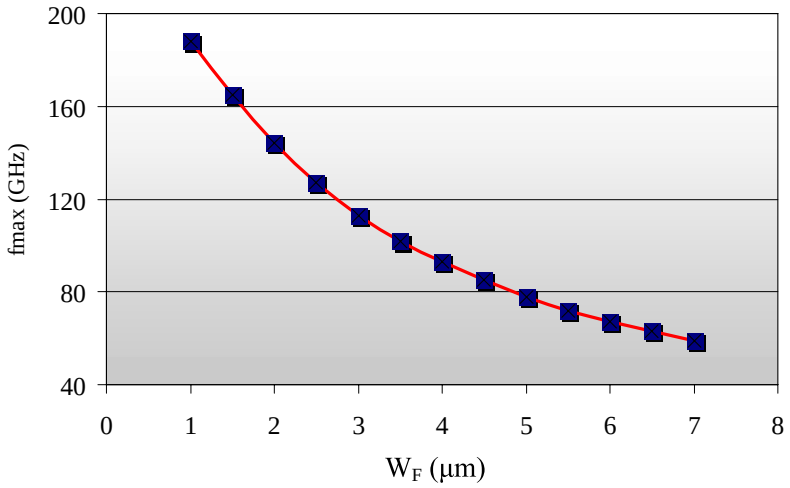


Figure 3.8: f_{max} as a function of W_F for 1 finger of an NMOS transistor

that, a high N_F reduces Z_{in} and Z_{out} causing high losses by matching networks. Moreover, a high reduction of Z_{in} and Z_{out} induces the risks of instability. Finally, due to the skin depth effect, the design of the transistor accesses requires more attention in order to have a uniform signal distribution in all transistor fingers.

- N_C: the model of a transistor is likely to be inaccurate for very long transistor ($N_F > 100$). Hence, dividing a big transistor into multiple small transistors in parallel represents a solution for this issue. In addition to that, the overall power is divided into multiple transistors reducing stress and improving transistor reliability.

To summarize, the purpose is to find the maximum W_T meeting the trade-off between power, losses and accuracy. It is important to determine the optimum W_T. After, an optimum N_C transistor is routed in parallel to provide the desired P_{out}.

After determining W_F, N_F and N_C, the next step consists in routing the transistor. Parasitics must be considered in the simulation setup. At mmW frequencies, neglecting parasitics induce a reduction of the gain due to important changes of Z_{in} and Z_{out} of the transistor. The determination of resistive and inductive effects is performed by simulating the different accesses to the transistor with HFSS. The determination of capacitive parasitics is performed by using the extractor tool of Cadence.

The other important issue is the electro-migration phenomenon. It must be in mind during the routing phase of the transistor. A transistor biased in class A carries an important DC

current. According to the current density rules, Figure 3.9 shows the evolution of the limit of the maximum DC current designed with a thin Metal 1 and with a thick Metal 7. The difficulty concerns more the low metalization level, from Metal 1 to Metal 5. The layout has to respect this restriction for reliability and aging issues.

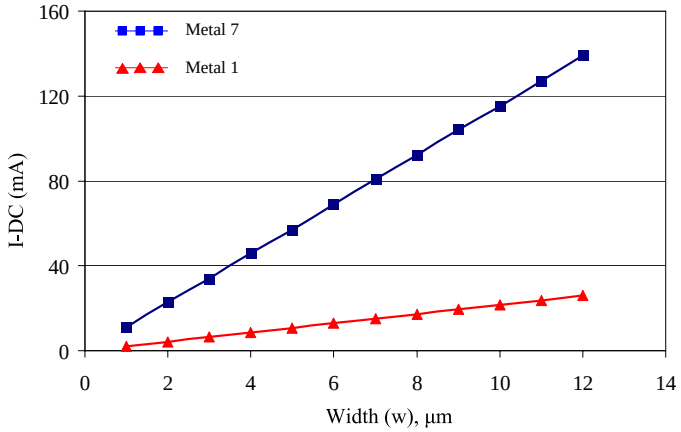


Figure 3.9: Limits of DC current as a function of w

3.2.2.3 Optimum Load Resistance Determination

This is the first step that aims at estimating the power performances of the power transistor in non-linear regime at the desired frequency (f_0). After designing the power transistor layout, it is necessary to present it an adequate Z_L to achieve a maximum P_{out}, gain or PAE. The choice of the FoM depends on the system requirements. Our purpose is to have a maximum P_{out} under class A operation.

In class A operation, the presented Z_L sets maximum voltage and current swings. Ideally, they are approximated to VDD and I_{DC}. In practice, a tuner is placed at the output of the power transistor sweeping Smith chart impedance plan. The power performances are calculated for each impedance to determine Z_{opt}. Indeed, Z_{opt} should be determined according to load pull or load line characterizations rather than presenting Z^*_{out} that optimizes only the transistor gain. Those two methods are presented as follows:

- **Contour plots:**
  This method consists in projecting constant P_{out}, gain, PAE contours after tuning Z_L. This method is more convenient to find rapidly Z_{opt}. Figure 3.10 shows the simulation setup and the determination of Z_{opt} to achieve the maximum P_{out} and the maximum PAE.

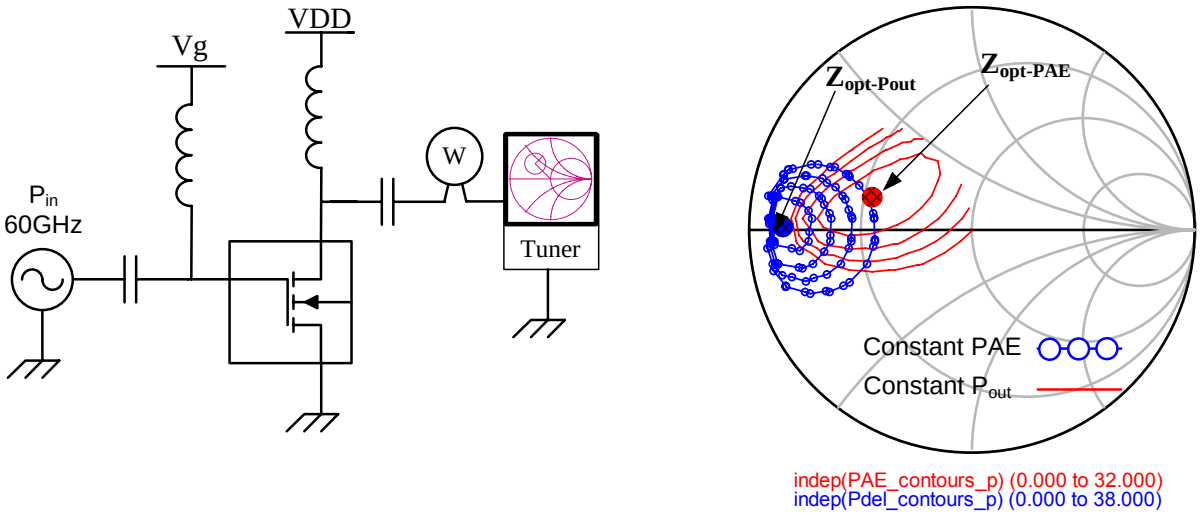


Figure 3.10: Determination of Z_{opt} with load pull simulation setup

Each FoM has its respective Z_{opt} demonstrating that the linearity-efficiency trade-off is also met during this analysis. Due to the availability of accurate models and measurement equipments at RF frequencies, the characterization of transistors is not limited to be performed at f_0. At mmW frequencies, this is not available anymore. It is only possible to perform load pull simulations to characterize transistors linearity by studying their behaviors at $2f_0$ and $3f_0$ or at $2f_2 - f_1$ and $2f_1 - f_2$ for double-tone f_1, f_2 excitation. However, this method hides phase information of the voltage and the current at the output.

- **Load line characterization:**
  It aims at plotting load line in the I-V plan. Figure 3.11 illustrates the behavior of the transistor for two different impedances. The first one is purely resistive and equal to 10Ω. The second one has the same real part and has a imaginary part equal to $j18$ to compensate the output capacitance of the power transistor. This impedance is found thanks to load pull simulations to achieve a maximum P_{out}.

When $Z_L = 10\Omega$, the load line is quasi-ideal. The slope of the line represents the real part of R_L. When Z_L=(10+j18)Ω is presented, the load line represents a two-dimensional curve that forms an ellipse. This is due to an important phase difference between drain current and voltage. The voltage and current swings are increased compared to the case when Z_L=10 Ω which allows getting higher P_{out}. That can be demonstrated by analyzing the difference between the line and the ellipse extremities. The area of the ellipse represents the reactive energy. A high area lowers the PAE and increases the transistor stress

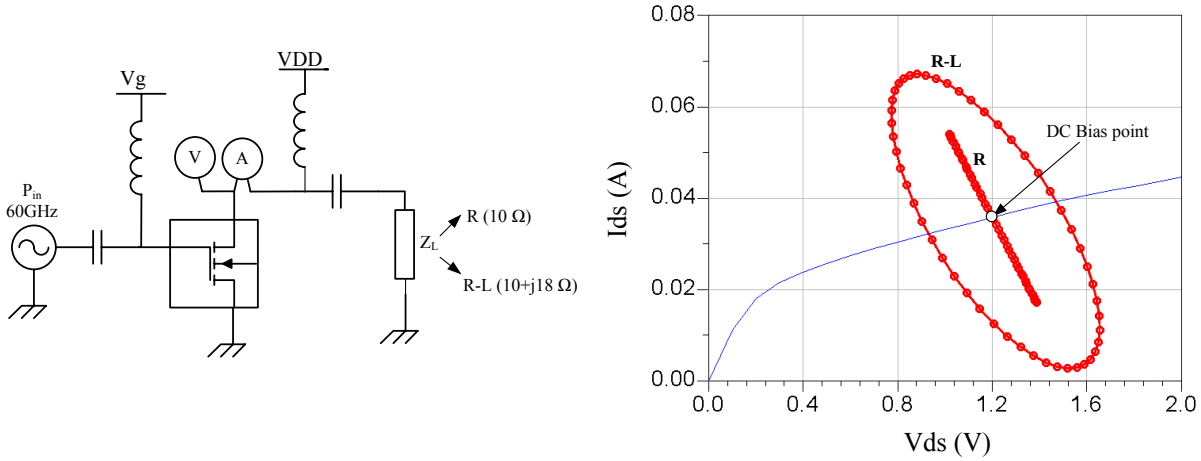


Figure 3.11: Load line shapes for different Z_L

[107]. Indeed, the transistor sustains frequently and simultaneously a high voltage and a high current during one signal period. The purpose is to obtain the minimum of loop area and a maximum voltage and current swings.

3.2.3 Driver stage design

The steps of the driver stage are similar to the ones of the power stage. However, the driver stage does not necessarily operate under the same conditions as the power stage. It depends on the technology performances and the system requirements. The two different ways are presented:

- **Similar design as the power stage:** some works demonstrate a driver stage similar (if not exactly) to the power stage [26] [57]. Other designs keep the same transistor dimensions with a reduction of the conduction angle by decreasing the gate biasing to operate in class AB. This methodology aims at conserving the PAE. The main motivation of this design is that CMOS transistors demonstrate low intrinsic gain at mmW frequencies. Hence, the driver stage remains almost under the same linearity constraints as the power stage.

- **Different design as the power stage:** In most cases, the driver stage is under-sized compared to the power stage. If the power stage provides a considerable gain compared to losses generated by its matching networks, the design of the driver becomes less critical and aims to provide higher gain. In this case, the fundamental difference between the power and the driver stage is that the driver transistor drives less current. Thus, the following list of constraints is lighted:

- W_T of the driver is lower than W_T of the power stage (till a ratio of 1/2).
- The driver transistor is matched to provide high gain instead of high power (its Z_{out} is matched to $Z*_{out}$ instead of Z_{opt}).
- The impact of parasitics is less important than the ones of the power stage.

Figure 3.12 depicts the power transfer for a typical PA composed by a driver stage and a power stage. The driver stage has a higher Compression Gain (G_c) than the one of the power stage. The input and the output 1dB compression point of the driver and of the power stage ($ICP1_{Driver}$, $OCP1_{Driver}$, $ICP1_{Power}$ and $OCP1_{Power}$) are defined in Eq. 3.4, where:

$$\begin{aligned} OCP1_{Driver} &= ICP1_{Driver} + Gc_{Driver} \\ OCP1_{Power} &= ICP1_{Power} + Gc_{Power} \end{aligned} \tag{3.4}$$

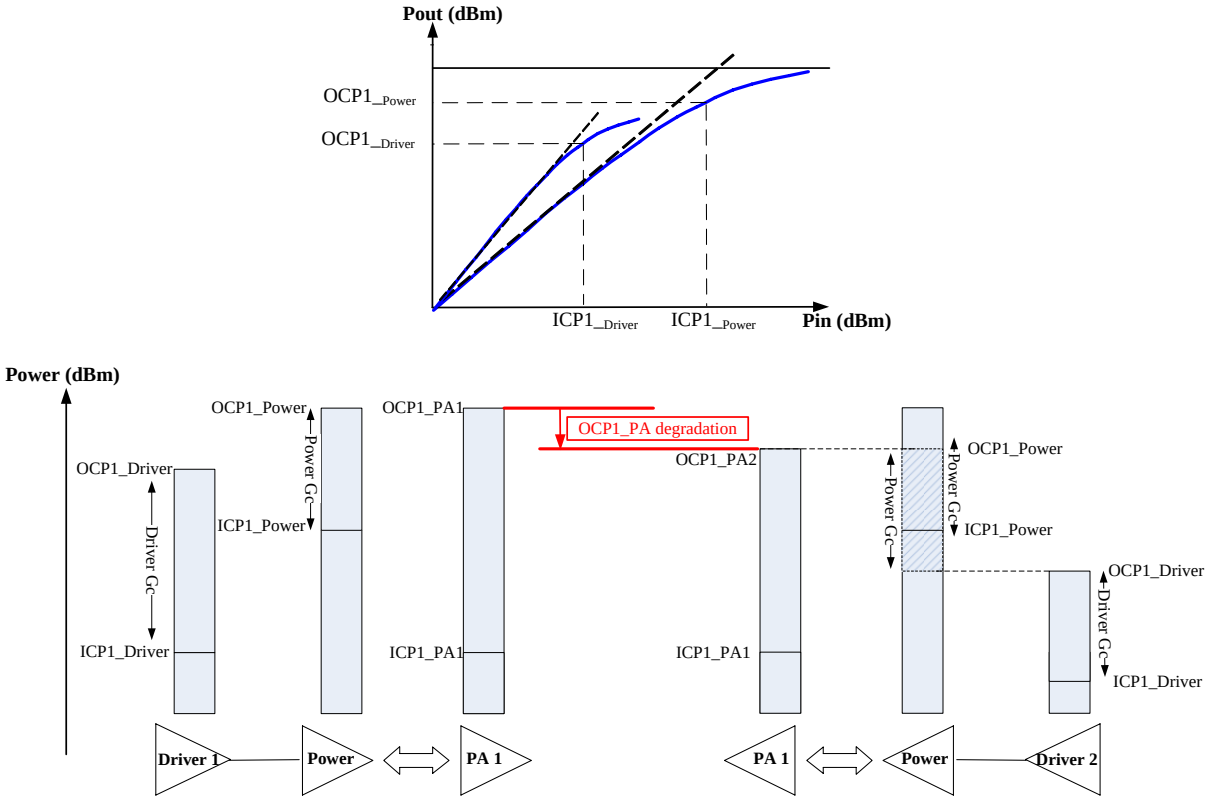


Figure 3.12: Illustration of linearity worsening because of the driver stage

Figure 3.12 illustrates an example where the power stage is already designed and the goal is to scale the driver stage without degrading the PA linearity. In plain terms, the purpose is to keep the $OCP1_{PA}$ same as $OCP1_{Power}$. The first driver (Driver 1) is designed in such a way that $OCP1_{Power} = OCP1_{PA1}$ while the second driver (Driver 2) degrades the PA linearity. As a result, $OCP1_{PA1} < OCP1_{PA2}$.

The difference between the two driver designs is described in Eq. 3.5, where the level of $OCP1_{Driver}$ is compared to $ICP1_{Power}$.

$$\begin{aligned} OCP1_{Driver1} &> ICP1_{Power1} \\ OCP1_{Driver2} &< ICP1_{Power2} \end{aligned} \tag{3.5}$$

Driver 1 is overestimated and thus the linearity is conserved while Driver 2 is underestimated degrading the PA linearity. The first design is preventive for linearity. This is at the cost of a high consumption and a low PAE. This is why a reasonable margin between $OCP1_{Driver}$ and $ICP1_{Power}$ is recommended to achieve a good linearity/efficiency trade-off.

The degradation of the PA linearity is risked when multiple drivers are designed to reach high gains. Only one under-dimensioned driver stage degrades the overall PA linearity. The design is managed upon trust to non-linear model of transistor and to the accuracy of passive device modeling that perform matching. According, to our experience in designing PA at 60GHz, our PA designs are based on PA composed by two stages, one power and one driver stage. This choice is also motivated to not degrade the PAE.

During PA design, other operations are not defined as a principal steps because they are done continuously during the PA design, from the beginning to the end of the design. They can not be defined sequentially. This part focuses on those operations, namely matching networks and stability issues.

3.2.4 Matching network

The determination of the optimum conditions of the power and the driver stages is the most important information to perform impedance matching. For a two-stages PA, three matching networks are integrated in the design as follows (cf. Figure 3.13):

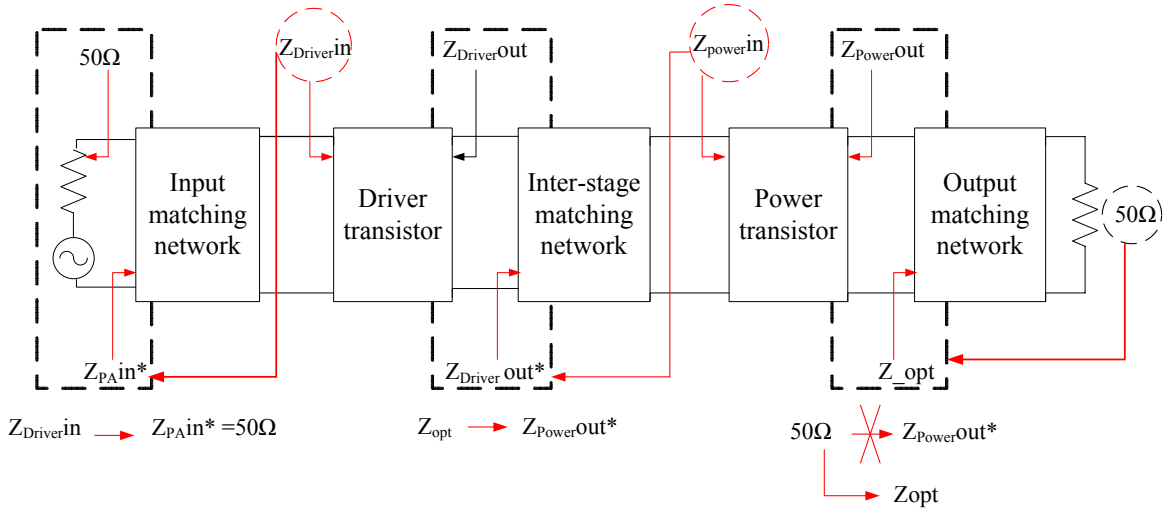


Figure 3.13: Matching networks in a PA

- An output matching network: to transform the normalized 50Ω output impedance to a desired Z_{opt}.
- An inter-stage matching network: to transform Z_{in} of the power transistor to a desired Z_{opt} or to $Z*_{out}$ of the driver. The choice of the transformed impedance depends on the appropriateness of power and gain performances of the active device with the system requirements.
- An input matching network: to transform Z_{in} of the driver transistor to the normalized 50Ω.

The most critical matching network in PA design is the output matching network. In one hand, this is due to its high impedance transformation ratio (r). Indeed, $r = 50/Z_{opt}$ is proportional to power losses of the matching network. Z_{opt} of big transistors is low especially in low voltage technology such as the 65nm CMOS (1.2 V). Hence, r is increased. In the other hand, each matching network acts as a filter. The purpose is to trap undesired harmonics to drive the fundamental harmonic. It suppresses non-linearities generated by the transistor to drive a sinusoidal current and voltage to the load. The selectivity of the matching network depends on its Q and r.

In one case, the matching networks affect the gain, already low in CMOS technology. In the other case, it must ensure a high fractional bandwidth to not restrict the PA bandwidth and the data rate of the system. Consequently, after characterizing the performances of passive device in chapter 2, the adopted order of the matching networks which is inversely proportional to Q has a maximum order of 2. The impedance matching of the inter-stage and the input is designed

with the same considerations. Only the impedances noticed before change.

At RF frequencies, the use of high inductors at the supply and the biasing circuits do not influence the impedance matching. At mmW frequencies, bypass capacitor shorts the the RF signal allowing matching networks participating in both biasing and impedance matching.

The choice between using lumped elements (inductors, baluns) or distributed elements (T-lines) is made during the BEOL and the passive devices analyzes. Both of them are used to design two different PAs presented later.

3.2.5 Stability analysis

A PA is the most subjugated device to be instable and to operate as an oscillator. The stability presents the most ambiguous issues to be analyzed. Numerous reasons make the PA potentially instable. In one hand, several methods exist to detect oscillations but it is difficult to assert a better one. In the other hand, choosing stabilization method must be efficient in the overall frequency domain and not only at operating frequency. The most known reasons that cause instability are plotted in Figure 3.14 and detailed as following:

- Fundamental reason of instability deals with control of feedback systems. If the input signal is fed by a portion of the output signal and the two signals are in phase *(Barkhausen stability criterion)* [108], the gain is improved in such a way that the output converges. The use of miniaturized transistors at mmW frequencies rises the risks of instability and makes analysis more complex. Indeed, transistors have a short channel making poor isolation between the input and the output (S_{12} $\nearrow$). A high C_{gd} and a low resistive substrate network present a path joining the output with the input.
- The outbreak of low frequency harmonics favors instability because of the high flat gain of miniature transistors. Moreover, those harmonics are mixed with the fundamental harmonic generating inter modulation product at the output.
- The simulation of passive devices is performed separately to avoid long computation time and high memory resources. Hence, mutual effect is not taken into account. Due to high coupling at mmW frequencies, a bad location (layout) of passive device decreases the isolation between the input and the output. Two examples are quoted:
  - Inductors are the most important element in the layout. They generate electromagnetic field to neighbor elements. Routing two inductors in the same direction

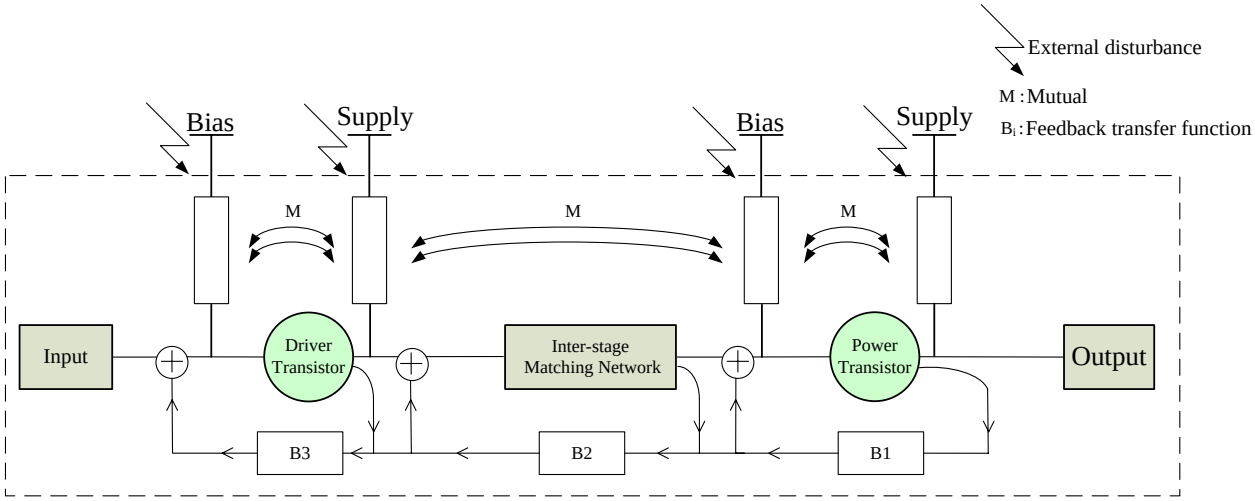


Figure 3.14: Causes of instability in a mmW PA

maximizes their mutual. If the $1st$ inductor performs output matching and the $2nd$ performs the input matching, a loop between the input and the output is formed. Additionally, output non-linearities are injected at the input.

– As discussed in section 2.2.1.1, two close MS lines exhibit high coupling. A T-line connecting supply voltage with transistor drain can be coupled with T-line connecting biasing circuit with transistor gate causing instability.

The stability analysis is categorized in linear and non linear studies. Both are necessary to predict PA stability. In most cases, only linear analysis is investigated to certify stability criterion. Those methods are described briefly highlighting their efficiency and their limitations:

- **Linear analysis:** it studies PAs such as 2-port systems. It uses S-parameters theory and sets conditions in input and output reflection coefficients ($|\Gamma_{in}|, |\Gamma_{out}| < 1$) in all the frequency range for a given load and source impedances. $K - factor$ and $B - factor$ parameters must respect both conditions (Eq. 3.6 and Eq. 3.7) to make PA unconditionally stable:

$$K = \frac{1 - |S11|^2 - |S22|^2 + |S11.S22 - S12.S21|^2}{2|S12||S21|} > 1 \tag{3.6}$$

$$B = 1 - |S11|^2 - |S22|^2 - |S11.S22 - S12.S21|^2 > 0 \tag{3.7}$$

This method is easy but only available for one couple of load and source impedances (Z_L, Z_s). It does not help for determining the wanted (Z_L, Z_s) to assure PA stability. To overcome this limitation, stability circles analysis is more powerful. Indeed, all (Z_L, Z_s) are swept in Smith chart plan. More details about the determination of stability regions are available in [109]. However, with this method, there is no prediction of the amplitude and the phase of the oscillation [110].

An other method consists in studying circuits by resolving differential equations in frequency domain using Laplace transform. The stability is given as a function of pole locations in Nyquist plan. However, this method is used for simple circuits (RL, RLC) and demands a transfer function of the studied system. It is difficult (if not possible) to determine an accurate transfer function of the PA without rough approximations.

Linear analysis are reformed and are efficient in small signal regime. The issue is that PAs are expected to operate in non-linear regime. Consequently, linear analysis has an uncertain significance in large signal regime [111]. Indeed, non-linearities of intrinsic transistor capacitances such as C_{gd} and C_{gs} lead to modify the transistor behavior in magnitude and phase. In addition to that, S-parameters are not available anymore if DC bias point is fluctuating in large signal regime. Nevertheless, linear stability analysis still remain significant if the PA is biased to operate in linear classes such as class A or class AB. Consequently, a non-linear analysis is required to assure PA stability.

- **Non-linear analysis:** non-linear stability analysis can be performed using Harmonic Balance (HB) simulations. This method is dedicated to non-linear circuits such as PAs. The HB computing process is operated in the frequency domain using Fourier transform. However, simulation results give power and stability performances at specific frequencies. Indeed, the input signal is an ideal sine wave signal limiting PA stability characterization only at integer multiple of the fundamental and not in all frequency range [111]. This is the main limitation of HB simulations. However, testing PA stability at the operating frequency is recommended because the PA is expected to provide a high gain increasing instability risks but a complementary analysis is still required.

Linear and non-linear stability analyzes can be performed using the Normalized Determinant Function (NDF) method. This method is efficient since it detects all types of

instabilities. The circuit is stable if NDF plots encircles the origin more times clockwise than counter-clockwise at the Nyquist plan. Despite the robustness of this method, it is not adopted in our design since it does not give any information concerning the stability margins.

Our adopted method to study PA stability is supported by linear and non-linear analysis:

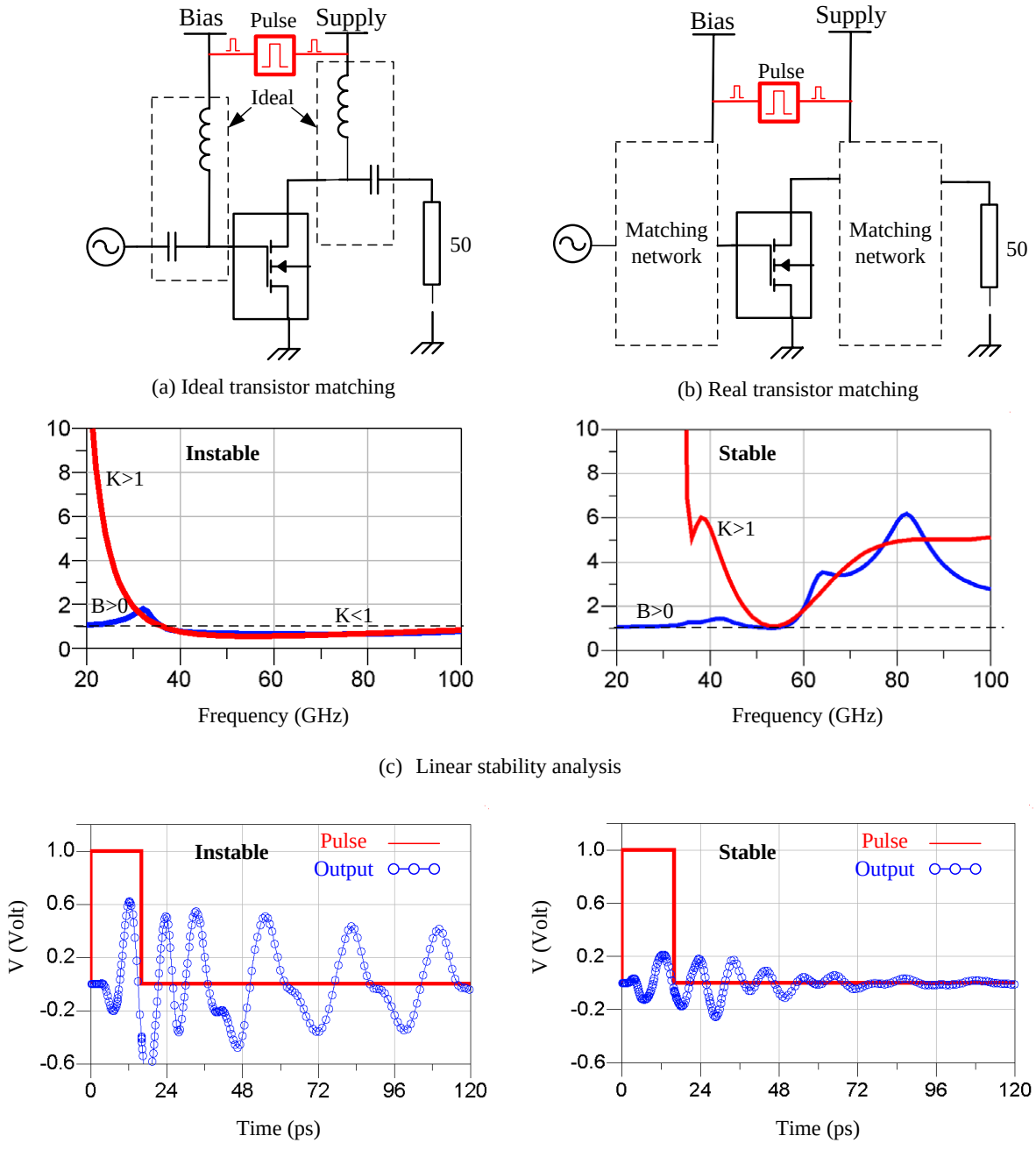
- In linear analysis, $K-$ and $B-$ factors are calculated separately for the power stage and the driver stage. A last computation of $K-$ and $B-$ factors is done at the end of the PA design.

- In non-linear analysis, after checking stability with HB simulations, a time domain approach based on transient simulation is adopted. The time domain is chosen because of its illustration of oscillation and divergence phenomena. This approach is commonly used in oscillator analysis. The PA is excited with temporal square wave pulse instead of sine wave signal due to its substantial number of harmonics (Eq. 3.8). In addition to that, the excitation is located in different regions of the PA (output drain, biasing circuit, inter-stage matching, ...). This procedure aims at stimulating the measurement setup where a PA is biased and must sustain to any external disturbances.

$$V(t) = \frac{E_0}{2} + \frac{2E_0}{\pi} \cdot \sum_{n=0}^{\infty} \frac{1}{2n+1} sin((2n+1)w_0 t) \tag{3.8}$$

If the PA exhibits instability, multiple stabilization techniques exist. The most common ones are based on feedback techniques or by adding a high-pass filter at the transistor gate. In the context of 65nm CMOS at 60GHz, those methods are not adopted because they degrade considerably the gain even at high frequency. They are useful in SiGe or GaAs PAs which have comfortable gains.

For our PAs realizations, all designed transistors are always instable if an ideal matching is performed. However, after integrating real components including losses, the gain of the transistor is reduced by resistive losses that stabilize the PA as depicted in Figure 3.15.



(a) Ideal transistor matching

(b) Real transistor matching

(c) Linear stability analysis

(d) Non-linear stability analysis

Figure 3.15: Linear and non-linear stability analyzes

The previous part presents the elementary principles and methods to design any PA. Contrary to a sequential design, numerous trade-offs must be considered at the same time. Gain-linearity, gain-stability and linearity-efficiency are controlled in every design step. One mistake in the design can degrades definitively each FoM. An investigation in passive and active devices as well in small signal as in large signal domains is required.

The next part presents two PAs realizations with different topologies:

- Single-ended PA designed with distributed elements.
- Differential PA designed with both lumped and distributed elements.

For each PA, simulation and experimental results are shown. Since the PA design procedure is detailed before, a brief description of the used active and passive devices of each PA is highlighted. A major interest is done for analyzing performances in order to propose novel solutions to improve PA performances.

3.3 Single-ended PA design

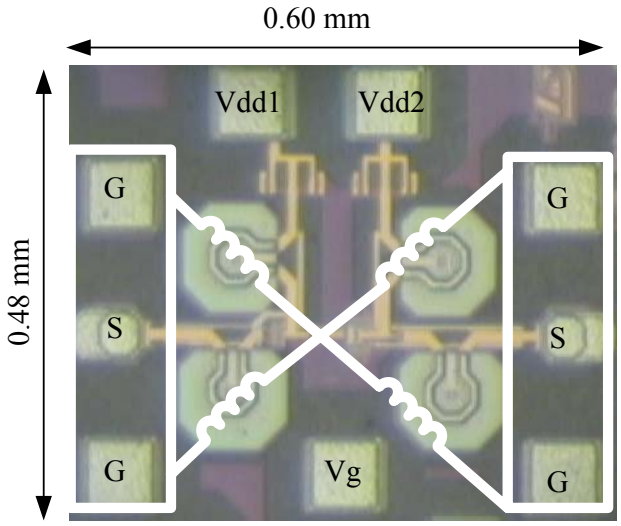
This work focuses on the characterization of active and passive devices before detailing the PA design. The novelty of this work is to realize a PA that demonstrates high performances in terms of linearity and efficiency. The ITRS FoM is our reference to compare this PA with the existing ones. This section is organized in three parts:

- The first part highlights few additional considerations according to issues met during the design of preliminary PAs. Providing an acceptable gain (gain > 10) in a desired frequency band is our first goal. Hence, the choice of passive devices is detailed. Passive devices are based on distributed elements instead of lumped elements. Moreover, novel RF-pad and ground plan are also designed.
- The second part summarizes the performances of the bulk 65nm CMOS Low Power Transistor (LPT). DC, S-parameters and load pull measurements are performed to predict the ability of LPT to provide power without consideration of passive network losses.
- The last part describes the PA design with experimental results. Finally, the PA performances are compared with PAs ones found in literature and designed with other technologies.

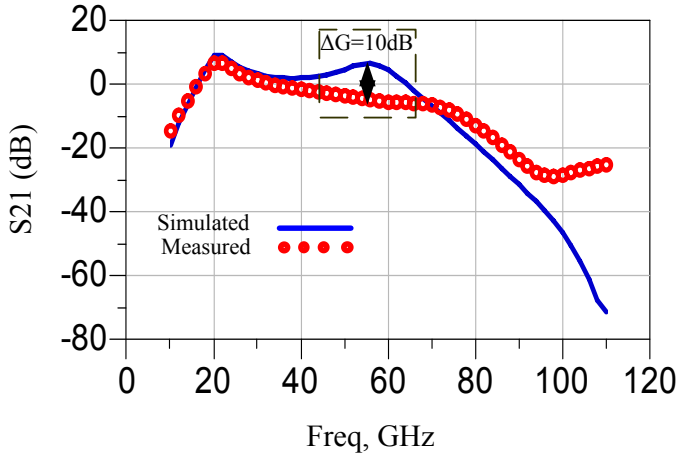
3.3.1 Passive device characterization

Two preliminary realizations of 60GHz PAs are presented in detail in appendix A and appendix B respectively. The respective adopted design techniques are also published in [112] and [113]. These PAs do not exhibit power performances as expected. According to measurement results, some design errors made during their design are pointed out. The next paragraph gives a brief description of circuit 1 and circuit 2 highlighting the different issues and the proposed solutions to them.

- The first PA (circuit 1) is matched with lumped and distributed elements. Figure 3.16(a) and Figure 3.16(b) show respectively the circuit 1 structure indicating the inaccurate analyzed areas in the design and the consequences on the PA gain. The simulation setup is set to correctly predict the PA behavior till 40GHz. According to redo simulation results, some assumptions must be reviewed over 40GHz. Indeed, assumptions that a RF-pad and the ground connections do not hardly affect the PA performances are not correct anymore at high frequency.



(a) Die photography of the circuit 1 highlighting neglected areas



(b) The gain of the circuit 1

Figure 3.16: Background of the circuit 1

Consequently, additional improvements are performed in the PA design to avoid gain issues. Those improvements are detailed as follows:

– **Bad current evacuation**: the absence of GND-pad in the circuit means that the overall current is evacuated by the GND-pads linked to the RF-pads. As the return current path is very long and resistive, the ground is not well distributed and not well defined in the circuit.

The most important issue concerns the ground connection with the transistor source. Indeed, connecting the transistor source to high inductance value creates a source degeneration reducing dramatically the gain. Consequently, a customized ground plan is designed in order to reduce as much as possible the inductive and resistive losses of the ground connections. Figure 3.17 shows the stacked ground plan which is designed under density rules.

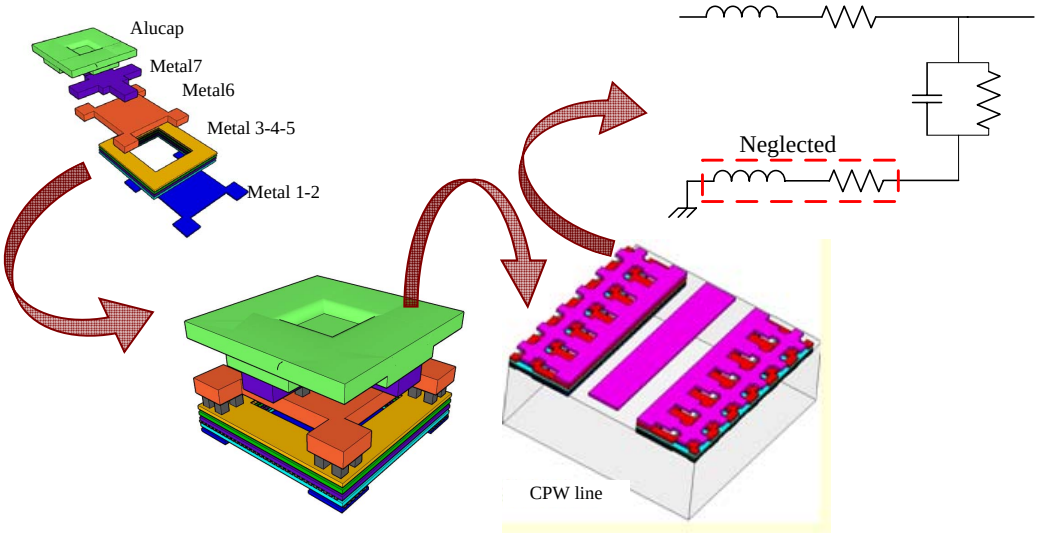


Figure 3.17: Novel ground plan layout

– **Pad resonance**: the RF-pad has an important intrinsic capacitance and inductance. Its intrinsic resonance frequency leads acting as a low-pass filter at the input and at the output of the circuit reducing considerably the gain. More details concerning the pad model and its resonance are given in section 2.2.3. Consequently, a design

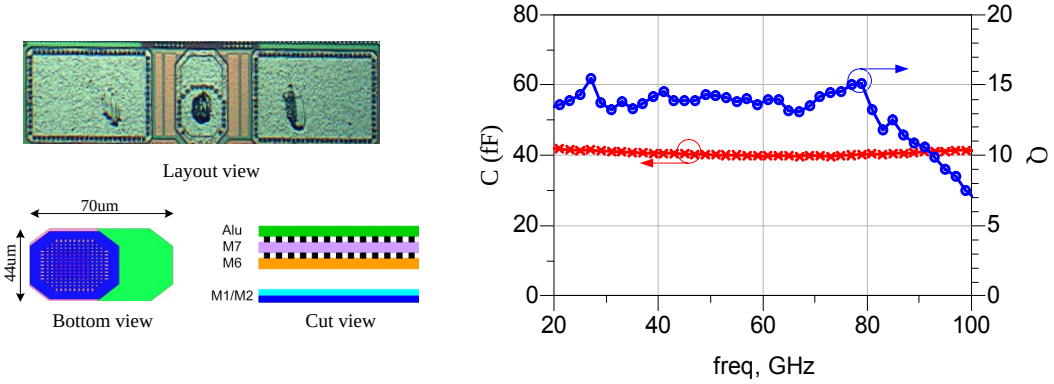
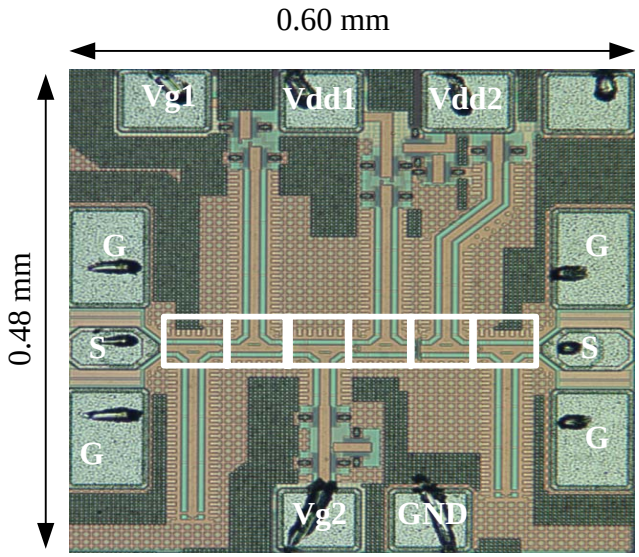


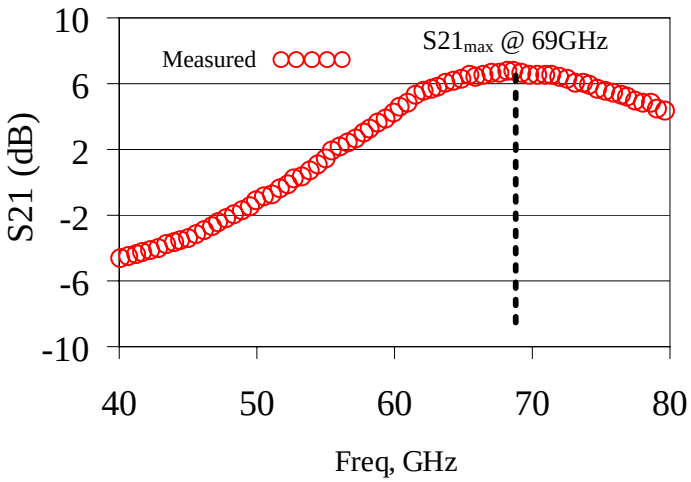
Figure 3.18: Novel ground plan layout

of a new RF-pad with a good trade-off between low parasitic capacitance and high Q is performed. The optimized Sh RF-pad design is presented in section 2.2.3.3. Figure 3.18 depicts an octagonal typical contact pad seen by different views. It has an intrinsic capacitances value of 40fF and a Q of 14.

– The second PA (circuit 2) is designed with CPW T-lines. Figure 3.19(a) and Figure 3.19(b) show respectively the circuit 2 die photography indicating the inaccurate analyzed areas in the design and the measured S_{21}.



(a) Die photography of the circuit 2 highlighting neglected areas



(b) The gain of the circuit 2

Figure 3.19: Background of the circuit 2

In this work, an over-estimation of the inductive effect in the T-junction interconnects is done. T-junction interconnects are used six times in the circuit leading to a frequency response shift of 5%. Hence, the PA reaches its maximum gain at 69GHz.

Consequently, additional improvements are performed in the PA design to avoid frequency shift and gain issues. Those improvements are detailed as follows:

– **Interconnect elements consideration**: a shift in frequency toward lower frequencies is due to a common mistake. In most of cases, it is resulting from a non-accurate modeling of the interconnect elements (T-lines, access to the transistor, ...). The use of T-Lines for biasing (not dimensioned to $\lambda/4$) leads to RF signal crossing over them. Thus, if numerous T-junctions present in the circuit are neglected, a frequency shift is expected.

Figure 3.20 confirms that the current flows mainly on the corners. This phenomenon is amplified by the skin depth effect which is responsible for the high current density concentrated on the edges of the line. A part of the metal in the center of the T-junction is cut to decrease the parallel capacitance. T-junctions have also an inductive effect with serial resistance. This model is taken into account in the simulation schematic. However the inductive effect has been overestimated to 20pH instead of 10pH.

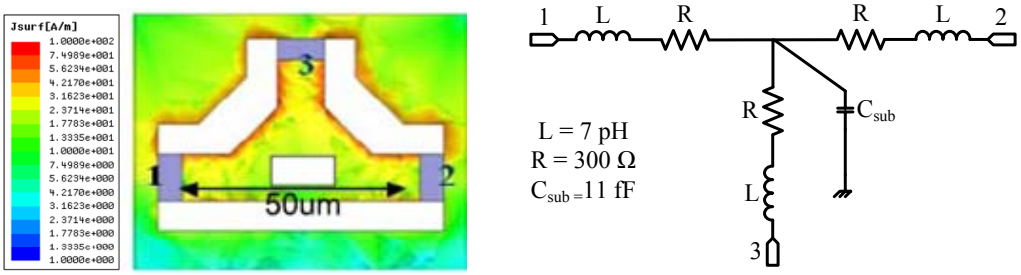


Figure 3.20: T-junction current distribution and its lumped model

In addition to the listed considerations, the CPW T-lines are used instead of inductors. Indeed, the first design uses the smallest inductor value of 80pH. This inductor sets the rest of the matching network. Besides, T-lines are scaled in length offering additional flexibility during

matching network design. Their advantage consists in the easiness of their characterization and their broadband behavior. CPW lines topology is adopted for our design. Their characterization is detailed in section 2.2.1.2. To reduce the PA die area, ideas are exposed as follows:

- The minimum of serial T-lines are used. All the matching is performed with parallel elements and serial capacitors.
- The T-lines simultaneously feature in the matching and the biasing (there is no additional bias circuit).

3.3.2 Active device characterization

Two different transistors are available in the 65nm CMOS DK namely, Low Power Transistor (LPT) and General Purpose Transistor (GPT). A detailed comparison is given in [114] and summarized in Table 3.3. LPT is the standard active device while GPT includes process options. Because of low cost motivations, LPT is chosen. It has a low leakage current and sustains a higher voltage supply of 1.2V compared to GPT which sustains only 1V. Although, the LPT has a thick gate oxide which limits the power gain at mmW frequencies.

Table 3.3: Comparison between LPT and GPT

	f_t (GHz)	$I_{on}(nA)$	$I_{off}(nA)$	Voltage supply (V)	Gate oxyde (Å)
Standard GPT	202	765	26	$1 \pm 10\%$	1.3
Standard LPT	162	610	0.35	1.2 ± 10	1.8

The power transistor is set to $(W_f, N_f, N_c) = (1\mu m, 90, 1)$. It has a smaller size compared to the first realization. The transistor model is more accurate and some improvements on its routing are done to reduce extrinsic capacitive parasitics. Figure 3.21 plots the 3D view of the scale-shaped layout. Indeed C_{gs}, C_{gd} and C_{ds} are reduced by 25%, 5% and 50% respectively.

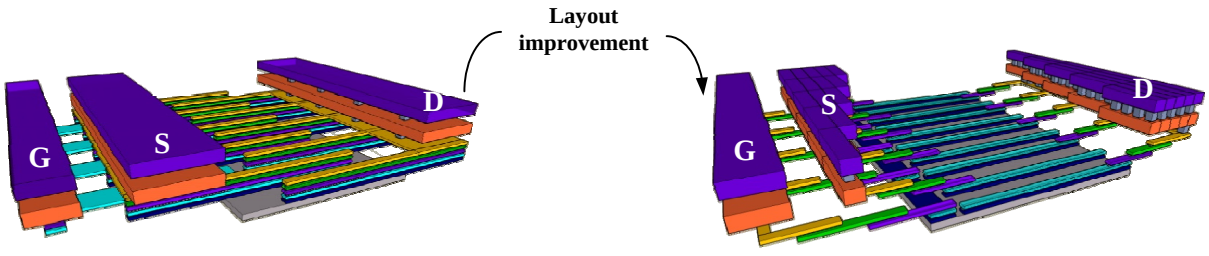


Figure 3.21: Layout optimization of a 65nm NMOS transistor

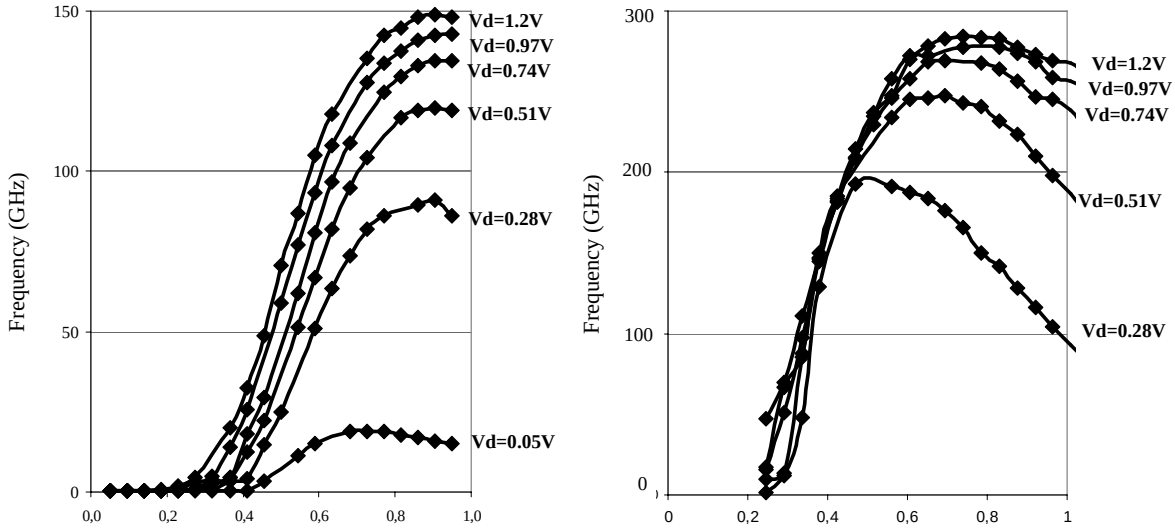
Table 3.4 gives the extrinsic parasitic capacitances which are extracted thanks to HFSS and Cadence extractor tools.

Table 3.4: Extrinsic parasitic capacitances

	$C_{gs}(fF)$	$C_{gd}(fF)$	$C_{ds}(fF)$
Typical transistor	19	6	28
Scale-shaped transistor	14	5	15

3.3.2.1 Small signal characterization

Figure 3.22 shows the measured f_t and f_{max} of a $(W_f, N_f, N_c) = (1\mu m, 90, 1)$ 65nm NMOS LPT. They are proportional to VDD and to $(V_{gs} - V_T)$. The current density monitors the transistor g_m featuring a maximum f_t of 150GHz at the optimum bias point (V_{gs}, V_{dd}) = (0.95V, 1.2V). Due to the optimized routing of the transistor, f_{max} has a higher value achieving 280GHz.



(a) f_t versus Vgs for a (1um, 90, 1) NMOS LPT

(a) f_{max} versus Vgs for a (1um, 90, 1) NMOS LPT

Figure 3.22: f_t and f_{max} for a $(1\mu m, 90, 1)$ 65nm NMOS LPT

The previous transistor is characterized from 1GHz to 110GHz. Open and short de-embedding structures are used to remove the capacitive effects of the RF-pad and the delay caused by the RF-lines as well as their serial resistive losses. Without high frequency considerations, the intrinsic behavioral simulation of the transistor (with its own accesses) results fit with the

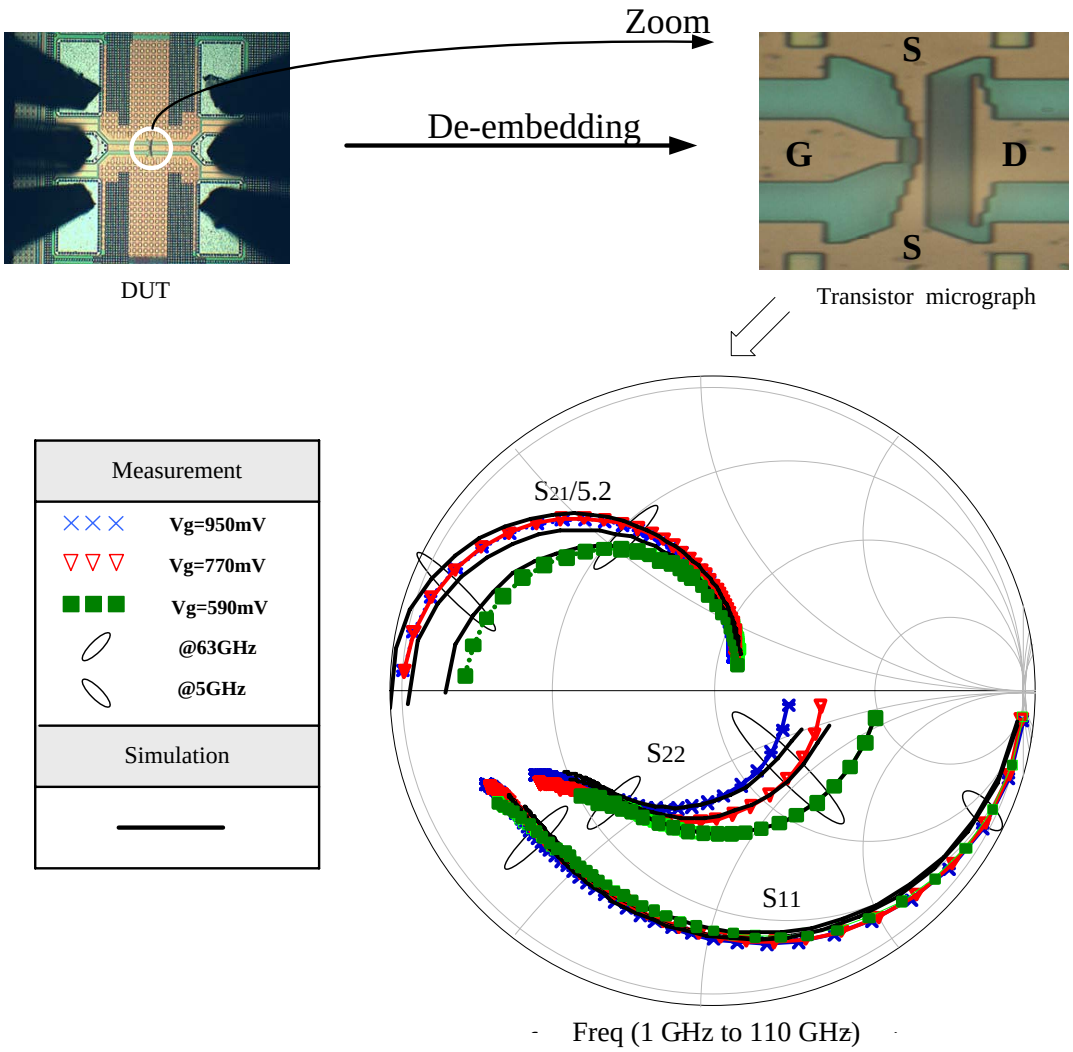


Figure 3.23: Measured and modeled S-parameters for $V_{dd} = 1.2V$

measurement results until 40GHz. At higher frequencies, accesses to the transistor have to be considered to be in compliance with measurement results as shown in Figure 3.23. Losses due to the conductive substrate and the serial resistances of the gate, source and drain are increased. Hence, parasitic elements are added in simulation setup. It can be noticed that parasitic values are only available around 60GHz. That justifies why S_{21} does not fit with the measurement results only for frequencies lower than 10GHz.

3.3.2.2 Load pull characterization

The load pull measurements enable the validation the transistor model in its non-linear regime. A Focus load pull system from 58GHz to 90GHz is used. It is described in Figure 3.24. At

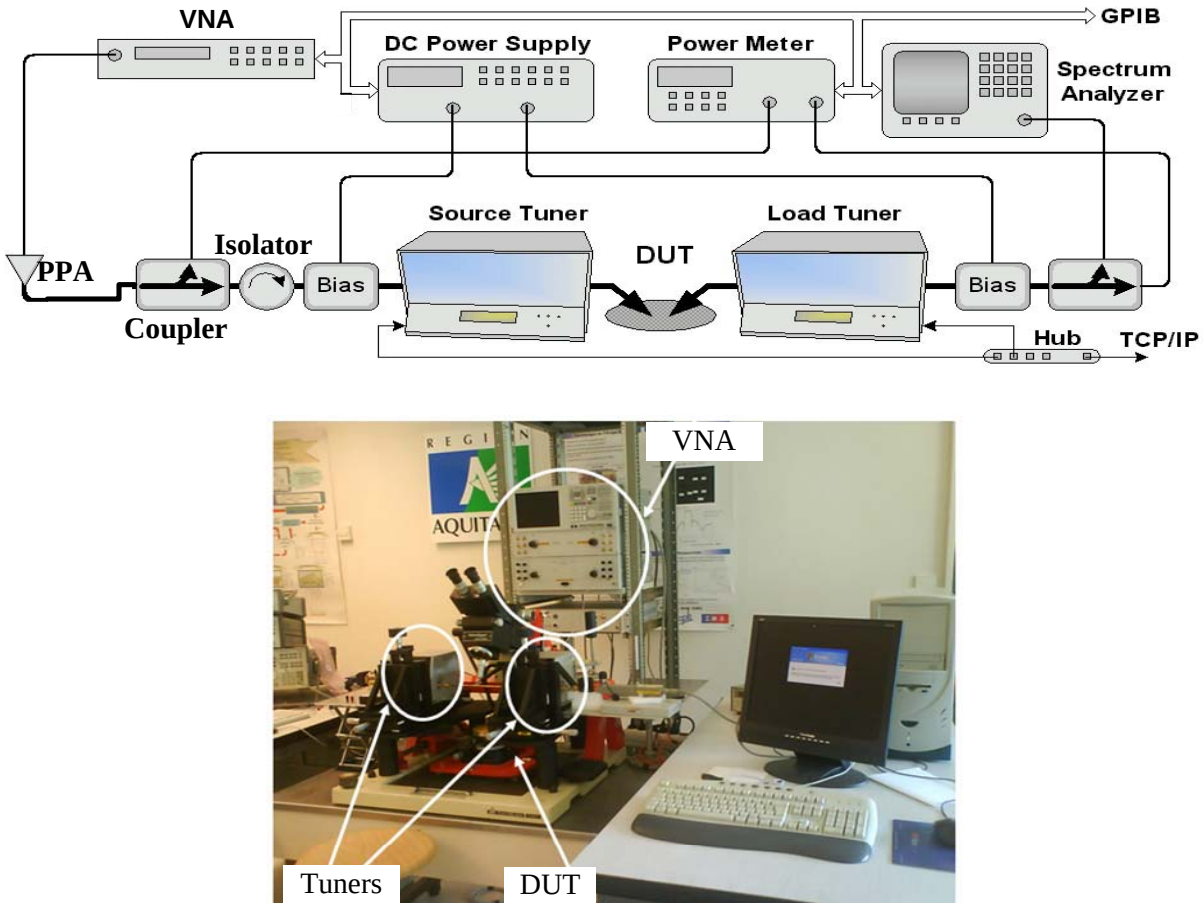


Figure 3.24: Load pull measurement setup

60GHz, the source delivers a maximum power of -2dBm which it is not sufficient to reach ICP_1 of the targeted 60GHz PA. This is why a preamplifier providing a gain of 18dB with an OCP_1 of 8dBm is added. To vary load and source of the DUT, two mechanical tuners are used. The tuners can not sweep the overall Smith chart because of high frequency losses. To perform the power measurements, a 10dB 60-90GHz directional coupler is used. After the load tuner, an isolator is used to prevent from the reflected signal in the coupler. Finally, a variable attenuator ensures the good operating of power sensors. Measurement results are processed by computer with a dedicated software. This work focuses on characterization of the power transistor used in the PA design.

The $(1\mu m, 90, 1)$ 65nm NMOS LPT is characterized. The simulated constant P_{out} contours are plotted in Figure 3.25. The difference between two contours exhibits a power difference of 1dB. After de-embedding, the optimum simulated and measured impedances are $Z_{opt}(sim) =$

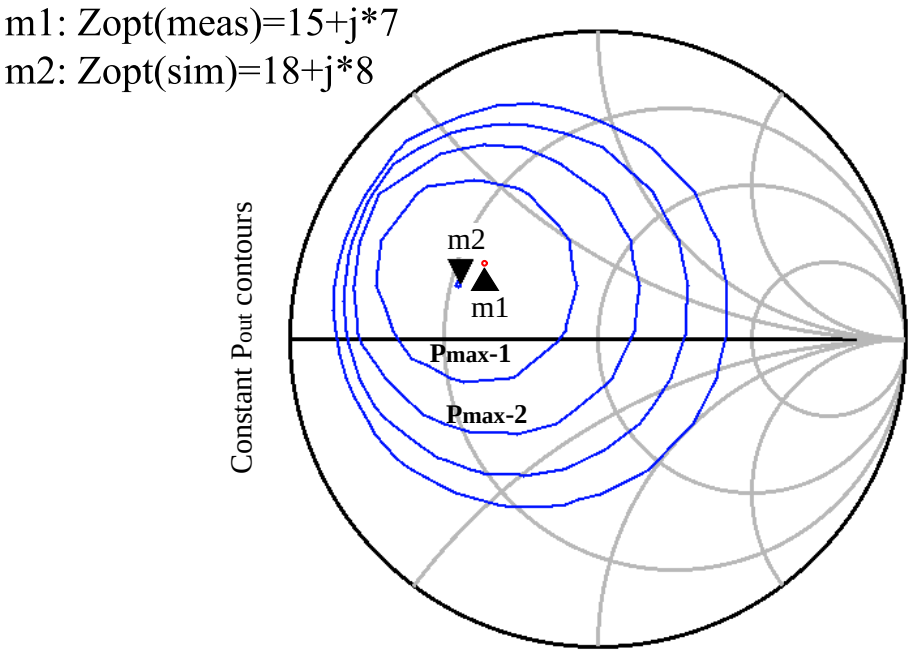


Figure 3.25: Measured and simulated optimum impedance to deliver a maximum P_{out}

(18+j∗8) and $Z_{opt}(meas)$ = (15+j∗7) respectively. An inaccurate matching does not affect dramatically P_{out} since the distance between two contours is large. This does not remain valid for very large transistors ($W_T = 400\mu m$) [104]. Metallic and dielectric losses considerably increase with the size of the transistor making the total gain sensitive. This is an additional reason motivating the use of small transistor size.

The transistor is driven over a wide range of input power when the optimum impedance is set. It varies from -12dBm to 8dBm. Figure 3.26 shows the P_{out}, the gain and the drain efficiency performances. The transistor is biased at $(V_{gs}, V_{dd}) = (0.95V, 1.2V)$. This bias conditions lead to a DC current of 32mA. The transistor achieves a P_{sat} of 11dBm and an OCP_1 of 9.4dBm. This result gives the maximum P_{out} delivered by the PA. The 1dB compression gain is 5dB and the maximum PAE is 18% at 63GHz. The slight difference between the simulation and the measurement results on P_{out} and gain is lower than 1dB. A slight difference of 3% is observed for the maximum PAE. It is explained by the deviation between the simulation and the measurement results seen in the I-V characteristics in Figure 3.27. Open-short de-embedding reveals a good match between the simulation and the measurement results.

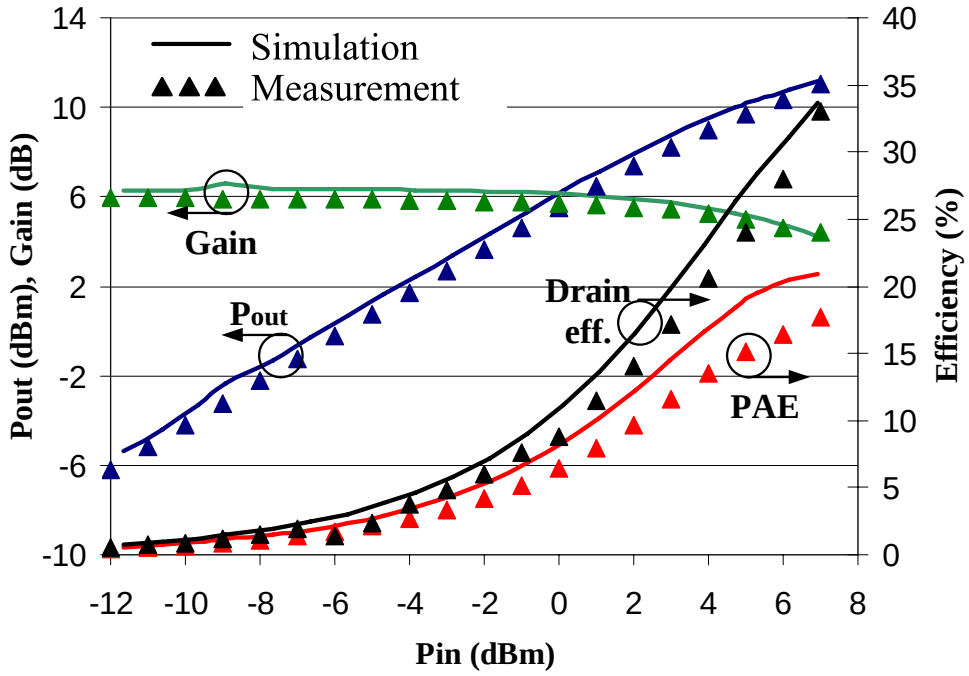


Figure 3.26: Power performances of the power transistor at Z_{opt} for a maximum P_{out}

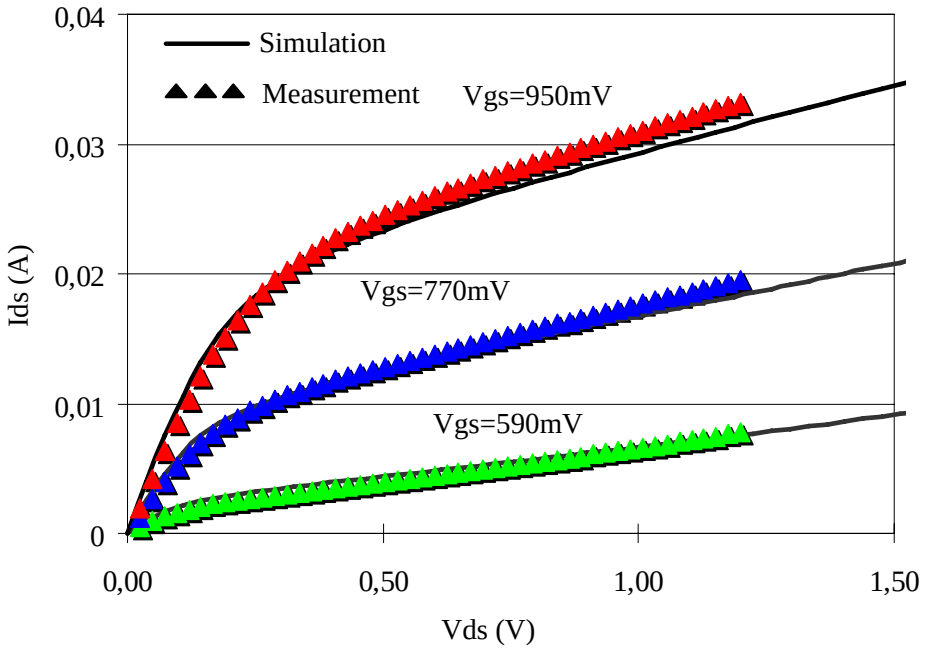


Figure 3.27: I-V characteristics for a $(W_f, N_f, N_c) = (1\mu m, 90, 1)$ NMOS LPT

3.3.3 PA description and results

The PA is a single-ended two-stage CS structure. The power transistor is described before and the transistor of the driver stage is sized to $(1\mu m, 48, 1)$. Both of them are biased in the same conditions $(V_{gs}, V_{dd}) = (0.95V, 1.2V)$ to have a maximum g_m. The two stages are biased by T-lines that also feature the matching since a RF-short is presented to the targeted length of the T-line. The short is made thanks to the MiM capacitors of 3pF. The MiM capacitors are exclusively used to perform DC blocking and supply decoupling. They offer a better Q compared to the MoM capacitors. Their values are set to roughly 150fF and 3pF respectively. The output matching transforms the impedance from 50Ω to the optimum impedance determined to obtain P_{max}. The driver stage is matched to its conjugate impedance to offer the maximum gain. The input impedance is matched to 50Ω. Thanks to the absence of serial lines, the PA takes place within a compact silicon area of $0.29mm^2$ with pads. Figure 3.28 and Figure 3.29 show the schematic and the die photography of the PA. The ground of the circuit is distributed in all metal layers to reduce significantly the resistive and inductive effects of the ground connections. Additionally, all ground surfaces are connected to the substrate by the contact vias.

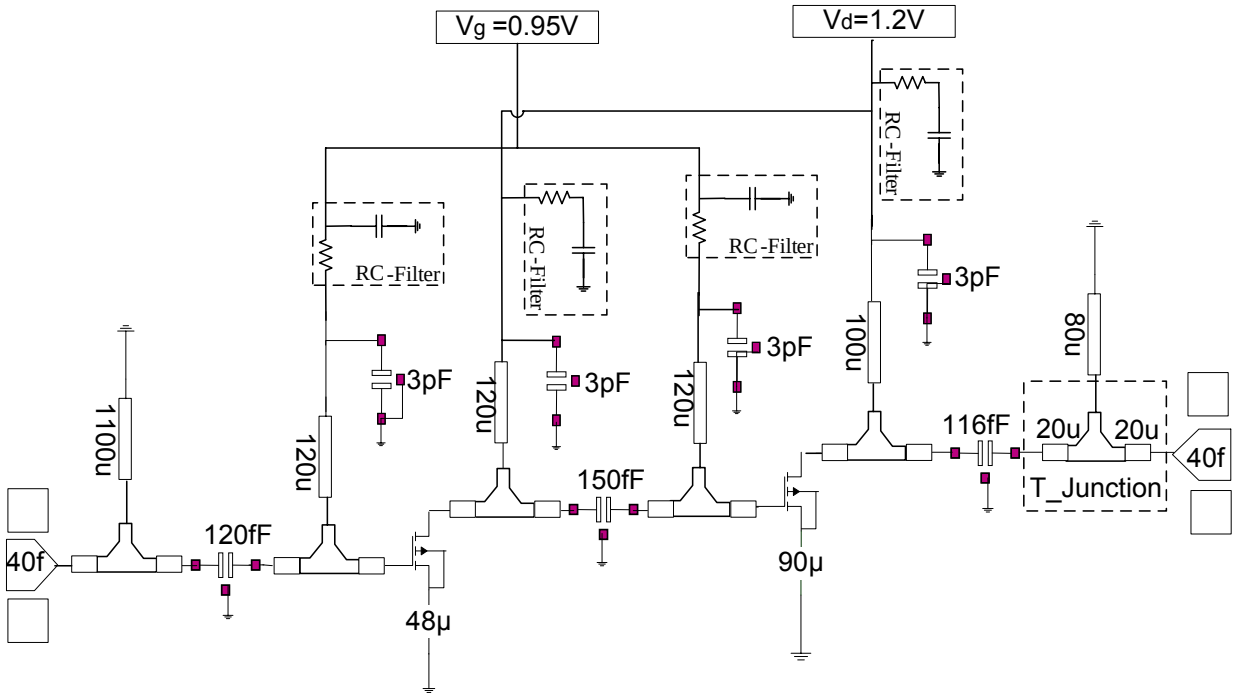


Figure 3.28: Schematic of the 60GHz single-ended PA in 65nm CMOS technology

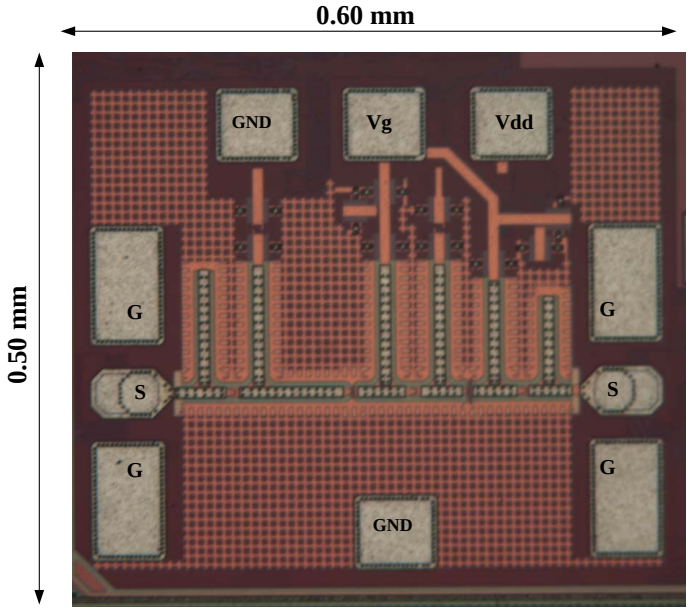


Figure 3.29: Die photography of the 60GHz single-ended PA in 65nm CMOS technology

3.3.3.1 Small signal performances

Measured S-parameters are reported in Figure 3.30. The PA reaches a maximum of 13dB at 63GHz. This PA operates in the desired band and offers a minimum gain of 9.7dB from 59GHz to

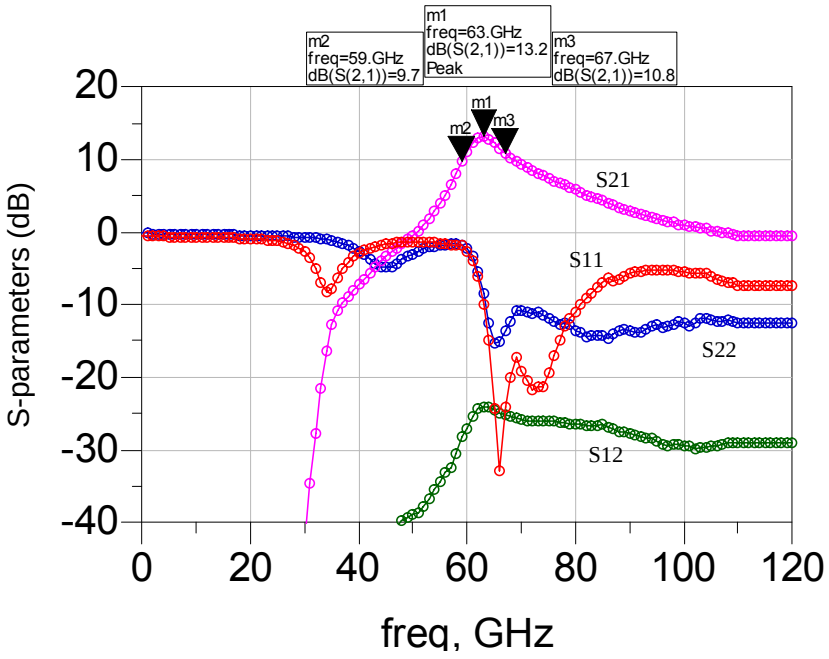


Figure 3.30: Measured S-parameters at the bias point $(V_{gs}, V_{ds}) = (0.95V, 1.2V)$

67GHz. The input matching exhibits a -32dB return loss whereas S_{22} is measured to -15dB. The isolation parameter is more than 25dB from DC to 110GHz. The PA offers good performances in terms of matching and gain in the useful band.

3.3.3.2 Large signal performances

Large signal measurement results summarizing the PA power characteristics at 63GHz are exhibited in Figure 3.31. The PA is matched to 50Ω at input and output. Thanks to the total bias current of 40mA, the PA has an OCP_1 of 9.2dBm and a saturation power of 10.6dBm at 63GHz. The PA has a maximum PAE of 8.6% at 63GHz. In the compression region, the PAE still has a value close to its maximum. This characteristic is targeted in the context of WPAN applications.

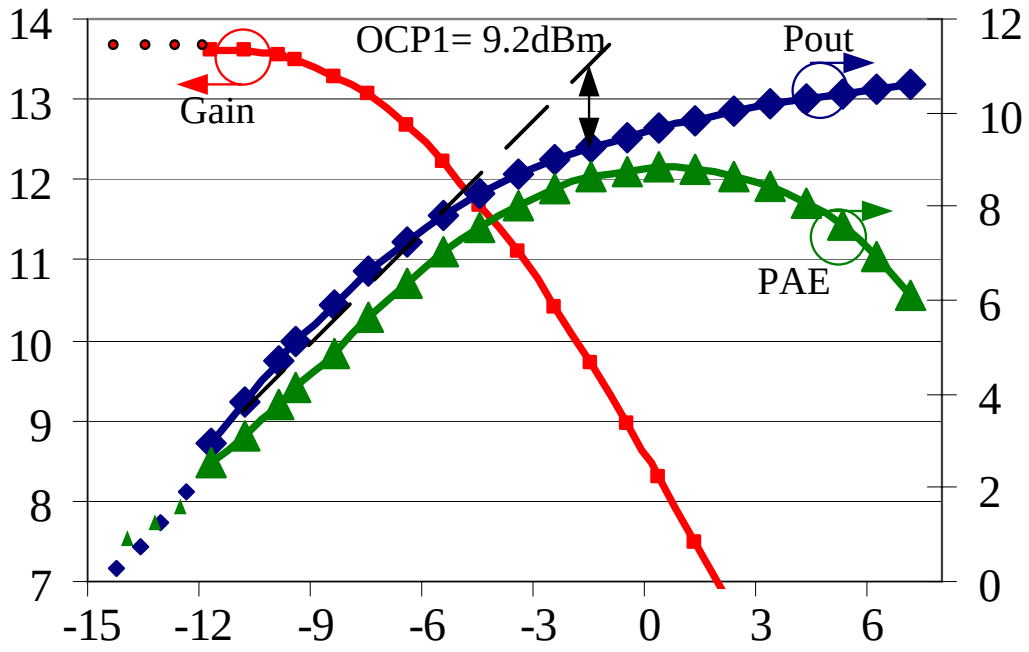


Figure 3.31: Measured P_{out}, gain and η_d at 63GHz $(V_{gs}, V_{ds}) = (0.95V, 1.2V)$

3.3.3.3 Performance improvements with load pull setup

Thanks to load pull measurements, the optimum output impedances of the PA are presented at 63GHz (cf. Figure 3.32). The real part of the impedance is close to 50Ω while the imaginary part is not null. Due to the tuner losses at 63GHz, the Smith chart is not completely covered and limited by a $|\Gamma_{max}|$ equal to 0.6.

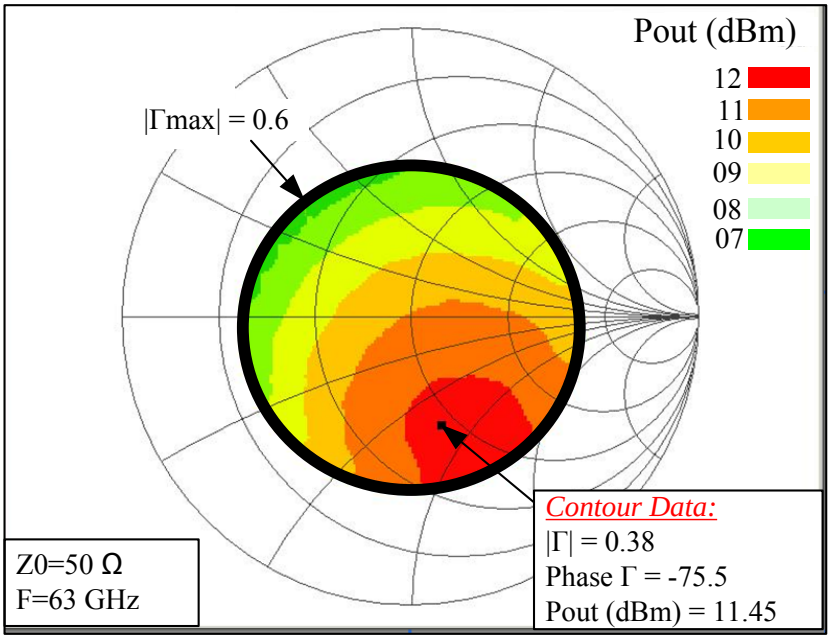


Figure 3.32: Z_{opt} determination to deliver a maximum of P_{out} at 63GHz

The power performances are plotted in Figure 3.33 and reported in Table 3.5. P_{sat}, gain and OCP_1 are increased resulting in a considerable improvement of the PAE. The PAE rises from 8.9% to 15%. This experience highlights the influence of Z_L in DC characteristic of the transistor. Indeed, with 50Ω, the P_{DC} varies with P_{out} and/or P_{in} and achieves a maximum value of 80mW while it is always close to 65mW when Z_{opt} is presented at the output of the PA.

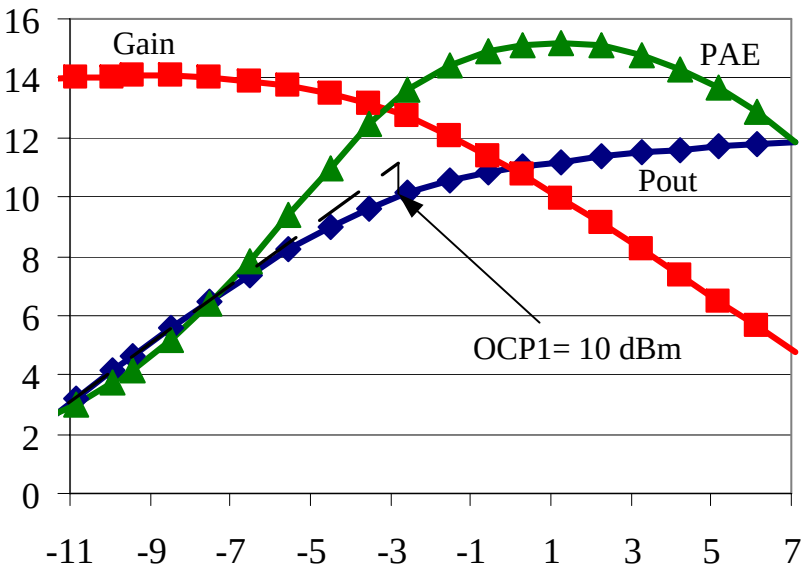


Figure 3.33: Measured P_{out}, gain and PAE at 63GHz

Table 3.5: Large signal PA performances

$(Z_{in}, Z_{out})(\Omega)$	Gain (dB)	P_{sat} (dBm)	PAE (%)	$OCP1$ (dBm)	P_{DC} (mA)
(50,50)	13.2	10.6	8.6	9.2	80
(Z_{Sopt}, Z_{Lopt})	14	12	15	10	65

3.3.4 Conclusion

The design flow and measurement results of a fully integrated PA are presented. DC, small signal and load pull analysis of the power transistor are demonstrated. More considerations are taking into account in this realization compared to first PA realizations. Indeed, the layout process is optimized. The RF-pads and the distributed ground plan are optimized to solve ground connection issues, met in the first PA design. CPW lines are well characterized and offer more flexibility in the design. Moreover, Tee-junctions are accurately estimated to solve frequency shift issue. This PA exhibits high performances affirming gain, linearity and linearity trade-off. Thanks to load pull measurements, the PAE of the PAE is improved reaching 15%. A comparison of power performances of the single-ended PA with PAs found in literatture is presented in section 3.5.

3.4 Differential PA design

The motivation of designing a differential PA is to increase P_{out}. Due to the absence of differential probes, the insertion of two baluns is required to perform single-to-differential mode conversion at the input and the output. According to passive device characterization discussed in chapter 2, baluns are expected to generate considerable losses. Our investigation aims at designing baluns with minimum of insertion loss about at least ($G_{PA} - 2 * Loss_{Balun} > 0$). This section is divided into three parts:

- Section 1 discusses about the balun design. Basic coupling structures are presented and compared by performing EM before presenting the implemented baluns.
- Section 2 presents the PA design with the experimental results. Lumped and distributed elements are used in this design.
- Section 3 discusses the optimization of the baluns. This analysis concerns particularly advanced technologies on bulk. Generally, three-port mixed-mode S-parameters characterize the balun performances. Our procedure is done differently. EM simulations are performed to visualize the electric and magnetic fields which are responsible for the voltage and current crossing over the balun. Finally, a high performance balun using an innovative methodology design is presented here and published in [115].

3.4.1 Balun design

The main issues of a balun design come from the thin BEOL and the low substrate resistivity. Those elements set the minimum insertion loss (IL_M) and the coupling factor K. The purpose is to minimize the insertion loss keeping K close to one to ensure energy transfer from the primary to the secondary. The implementation of baluns in the PA is optimized since they also perform input and output impedances matching.

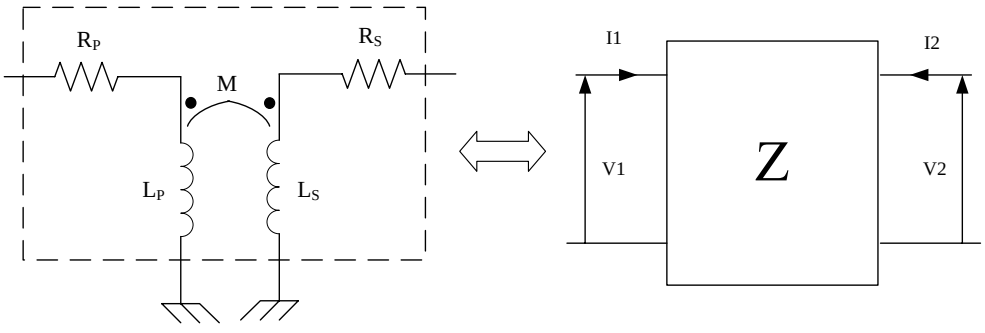


Figure 3.34: Simplified model of a generic transformer

Before choosing one topology, a simplified model of a generic transformer is plotted in Figure 3.34. According to current and voltage expressions, the impedance matrix is given by:

$$[Z] = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} R_P + jwL_P & jwM \\ jwM & R_S + jwL_S \end{bmatrix} \tag{3.9}$$

Where:

- L_P and L_S are the serial inductances of the primary and the secondary,
- R_P, R_S are the serial resistances of the primary and the secondary,
- M is the inductive mutual between the primary and the secondary.

Those elements are frequency-dependent and do not highlight all physical phenomena acting in a transformer. More explicit models are presented in [116] [117], [118] and [119]. The presented model still allows the comprehension of the transformer FoMs namely K and IL_M, defined according to Z-parameters in Eq. 3.10 and Eq. 3.11 [120]:

$$K = \sqrt{\frac{\Im(Z_{12})\Im(Z_{21})}{\Im(Z_{11})\Im(Z_{22})}} \tag{3.10}$$

$$IL_M = -10 \cdot Log_{10}(G_{max}) \tag{3.11}$$

Where,

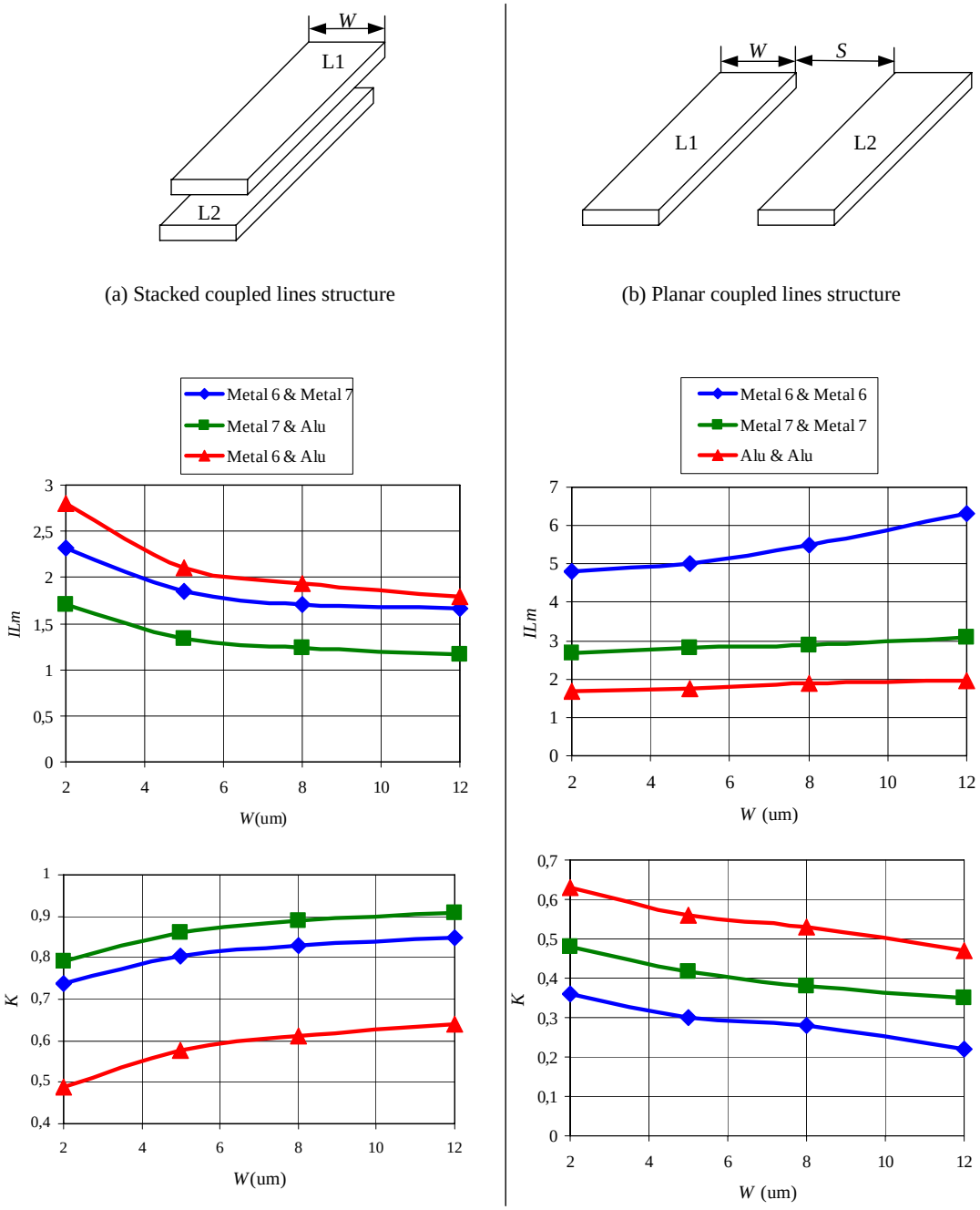
$$G_{max} = 1 + 2(x - \sqrt{x^2 + x}) \tag{3.12}$$

and

$$x = \frac{\Re(Z_{11}).\Re(Z_{22}) - [\Re(Z_{11})]^2}{[\Im(Z_{12})]^2[\Re(Z_{12})]^2} \tag{3.13}$$

At the beginning, the purpose of our study is to find the best way to perform coupling between the primary and the secondary. Thus, stacked and planar coupled lines presenting the two basic

transformer topologies are compared. The design of the adopted balun is presented at the end. Figure 3.35 shows their structures and the simulated results depicting K and IL_M versus W.



(a) Stacked coupled lines structure

(b) Planar coupled lines structure

(c) K and IL_M versus W, (S=2um) for stacked and planar coupled lines

Figure 3.35: Coupled lines characterization with EM simulation

Planar coupled lines are designed with the same high metal levels (Metal 6, Metal 7 and Alucap) where W varies from $2\mu m$ to $12\mu m$. The distance S separating the two lines is set to $2\mu m$ to maximize K. For the stacked coupled lines, the same W and metal levels are used. The coupling is performed between two different metal levels (Metal 6 & Metal 7, Metal 7 & Alucap and Metal 6 & Alucap).

For the planar coupled lines, the structure that demonstrates simultaneously high K and low IL_M is the one designed with Alucap metal level. However, Alucap metal level does not sustain high current. So, the structure using Metal 7 is preferred. K and IL_M are equal to 0.5 and 1.7dB respectively when W is at its minimum value of $2\mu m$. Increasing W makes capacitive-lossy coupling between the two lines and the substrate more important. It excesses the required active coupling that remains low and invariant.

For the stacked coupled lines, the coupling between Metal 7 and Alucap leads to better performances. As said before, to avoid design with Alucap metal level, the structure using Metal 6 and Metal 7 is preferred. K and IL_M achieve 0.9 and 1.3dB respectively when W is at its maximum value of $12\mu m$.

In terms of coupling and losses performances, stacked coupling demonstrates better results compared to planar coupling and thus is chosen for the PA design. Table 3.6 summarizes their performances with additional characteristic parameters.

Table 3.6: Comparison between planar and stacked coupled lines

	K	IL_M	Q	SRF	Compact	Symmetry
Most adapted one	Stacked	Stacked	Planar	Planar	Stacked	Planar

The choice of the inductor (primary or secondary) shape does not change considerably the balun performance especially in mmW frequencies context. Indeed, the number of inductor turns is low if not only limited to one turn. Consequently, our work is based on the known orthogonal inductors without PGS since they are already analyzed and presented in section 2.2.2. The diameter of the balun and W are the two degrees of freedom to perform input and output impedances. The input balun must transform the impedance of 50Ω to $2Z_{INtransistor}$ as depicted in Figure 3.36.

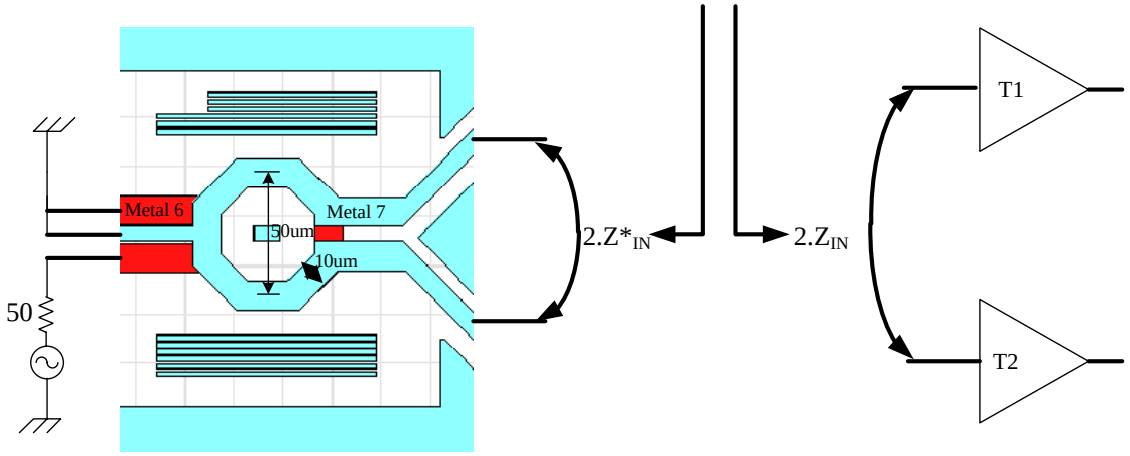


Figure 3.36: Balun integration in a 60GHz PA (only input is plotted)

3.4.2 PA design description

The schematic and the die photography of the PA are depicted in Figure 3.37 and Figure 3.38. Two different stacked baluns are placed at the input and the output of the circuit to ensures simultaneously matching and single-to-differential conversion. The amplification is performed thanks to a two-stage CS structure. The power transistor and the driver stage have the same size as the previous PA namely, $48\mu m$ and $90\mu m$ respectively. The transistors are driven to operate in class A to satisfy linearity requirements. Bias connections of the first stage and supply connections of the second stage are performed at the virtual ground points of baluns. The bias connections of the second stage and supply connection of the second gate are individually performed for flexibility. The driven current is equal to 32mA for the driver stages and equal to 66mA for the power stages. Matching structures are symmetrically designed to maintain a balanced design.

50Ω CPW lines are used as the ones used in the previous design. MiM capacitors are used in this design to ensure several roles: C_m capacitors ensure DC blocking and matching impedance, C_s capacitors improve stability and C_g capacitors assure a RF-short to the virtual ground points of the balun. The PA is matched to 50Ω at the input and the output. Thanks to the absence of serial lines, the active area takes place within a compact silicon area of $0.065mm^2$. The NSh RF-pad is used. All ground surfaces are connected to the substrate by the contact vias.

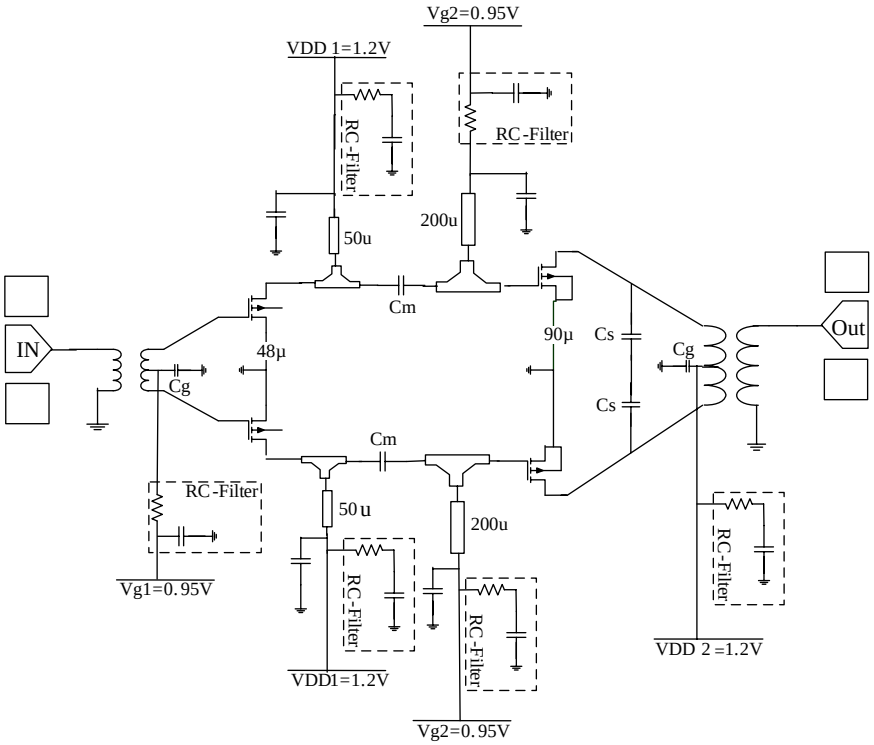


Figure 3.37: Schematic of the 65nm 60GHz differential PA

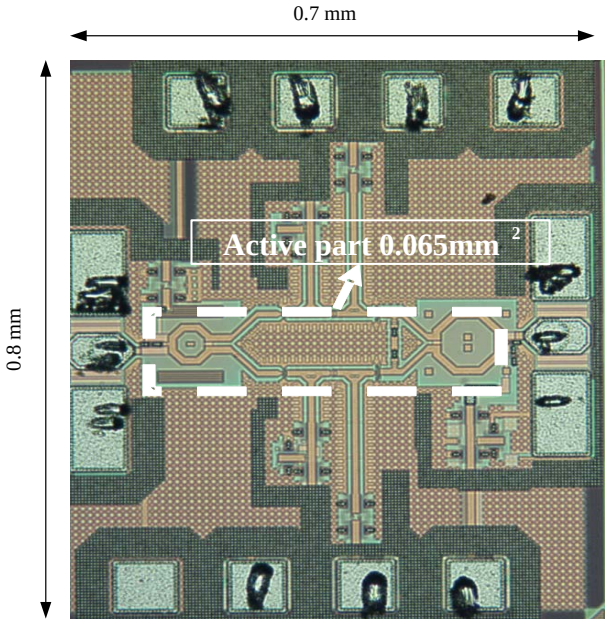


Figure 3.38: Die photography of the 60GHz differential PA

3.4.3 PA measurement results

The small signal measurement results are plotted in Figure 3.39. The PA operates at the desired frequency band because of the accurate modeling of passive and active devices. At a voltage supply of 1.2V, the PA reaches a maximum gain of 8.5dB at 61GHz in spite of losses caused by power dividing and power combining performed by the baluns. The input reflection coefficient is lower than -10dB at 60GHz while the output reflection coefficient is lower than 10dB from 62GHz to 76GHz. The isolation is more than 20dB from DC to 110GHz. Stability is improved by adding RC filters to absorb possible oscillations. P_{out} as a function of P_{in} is measured and is expected to be higher than the single PA one. However, the differential PA reaches a P_{sat} of 7.2dBm and an OCP_1 of 4.2dBm (cf. Figure 3.40). In these, conditions, the PA has a weak PAE of 2.3%

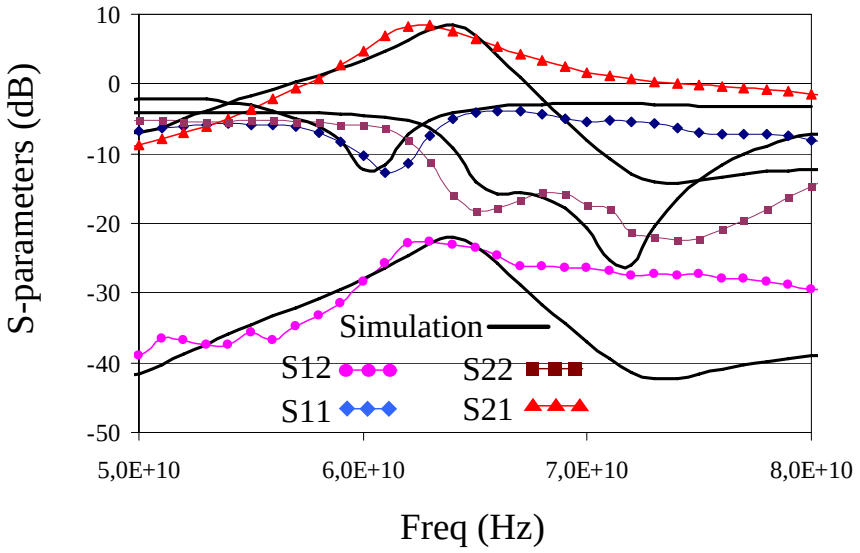


Figure 3.39: Measured S-parameters at $(V_{gs}, V_{ds}) = (0.95V, 1.2V)$

3.4.3.1 Interpretation of measurement results

The PA is expected to exhibit better linearity performances. However, it does not demonstrate linearity or gain improvement even after performing load and source pull measurements. In addition to that, the two differential stages have the same power consumption than the one predicted by simulation. The issue is not coming from matching losses or transistor modeling but from the balun. Thus, it is analyzed in a different way. Indeed, during balun characterization, our attention is focused on the impedances brought by the balun. The conversion of the unbalanced to the balanced mode is assumed to be well performed due to its axial symmetry.

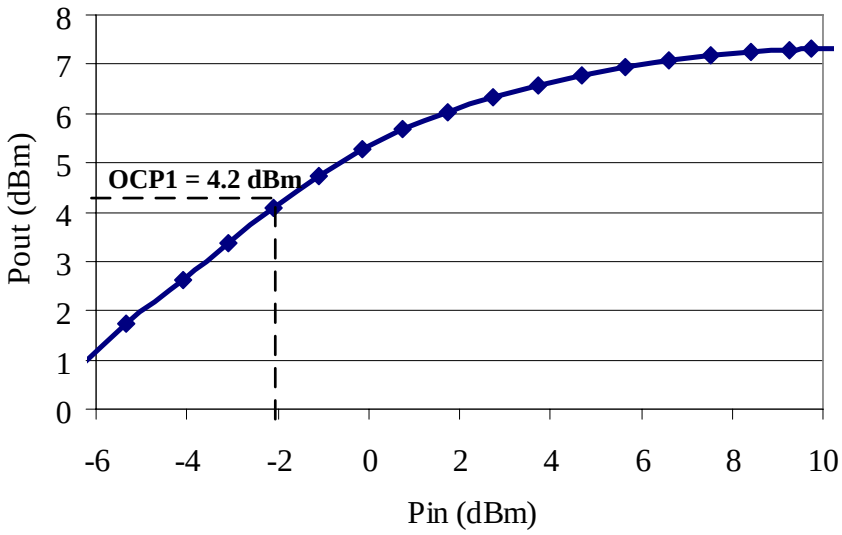
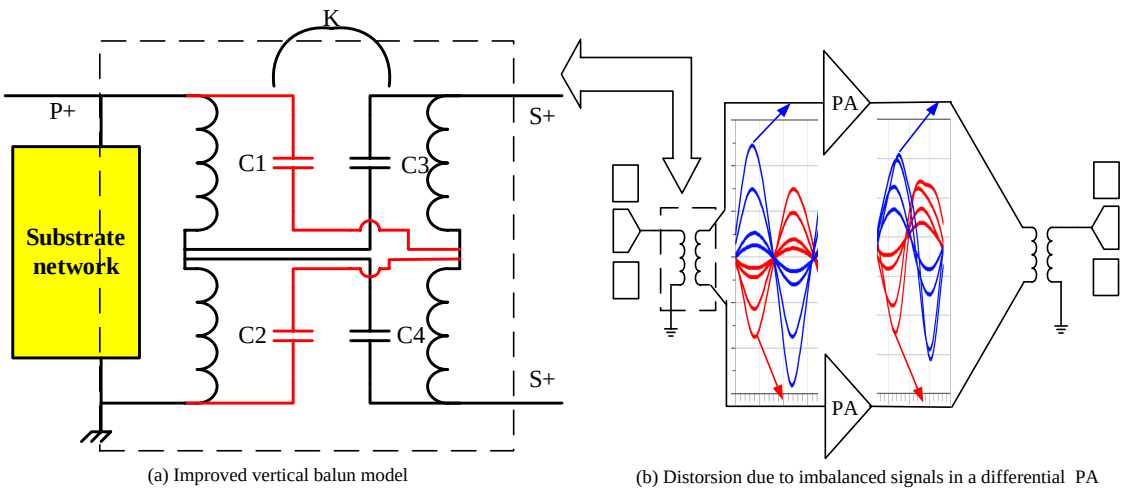


Figure 3.40: Measured power transfer at $(V_{gs}, V_{ds}) = (0.95V, 1.2V)$

To understand the reason for this unbalance, an advanced model of the vertical balun is plotted in Figure 3.41(a). It considers substrate effect and parasitic capacitances. The assumption that the axial symmetry induces a good conversion mode is not valid at mmW frequencies. According to the plotted model, $C3$ and $C4$ have a symmetric influence but some asymmetries are observed:

- $C1$ and $C2$ are exposed to the RF signal and to the ground.
- Only the primary is exposed to the substrate.



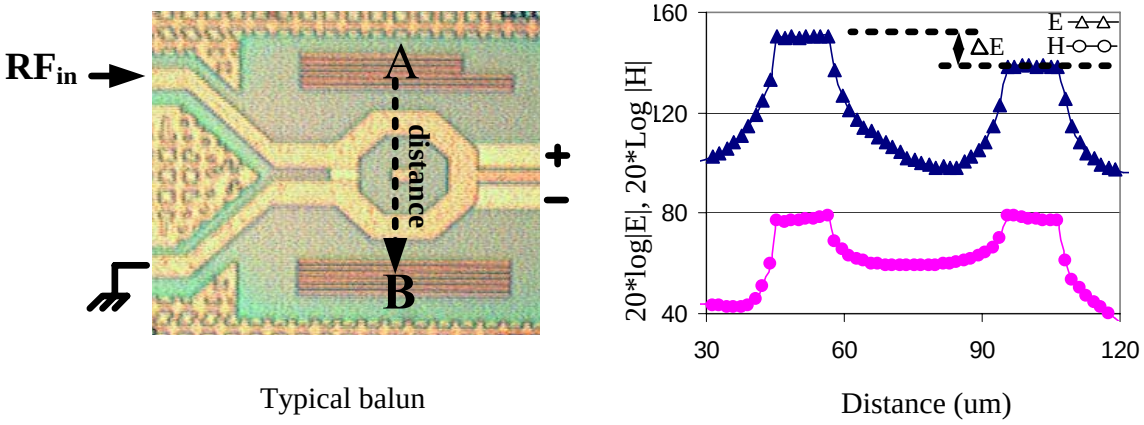
(a) Improved vertical balun model

(b) Distorsion due to imbalanced signals in a differential PA

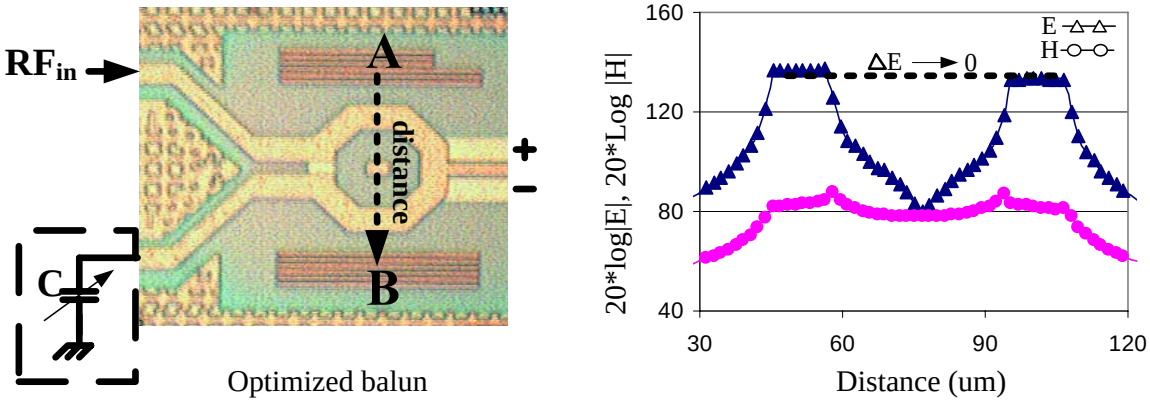
Figure 3.41: Balun assymetries and their consequence on the PA operation

However, time domain redo simulations enable to identify that the two differential stages are not acting in a balanced mode at 63GHz. Simulations exhibit a magnitude difference of 2.3dB between the two differential stages. In view of the aforementioned comments, the first half stage operates in the compression region while the second half stage remains in the linear region. Figure 3.41(b) illustrates the unbalanced two signals that pass through the differential PA.
To improve the balun performances, instead of using a typical three-port mixed-mode S-parameters characterization, EM simulations are performed to visualize the electric and magnetic fields which are responsible for the voltage and current crossing over the balun. Finally, a high performance balun using an original methodology design is presented.

3D-EM simulations are performed to confirm those reasons for this unbalance. Therefore, the magnitude of electric field and magnetic field are probed along the cross section AB (cf. Figure 3.42(a)). A single RF-mode is applied at the input of the balun. According to Figure 3.42(a),



(a) E and H distributions in a typical balun



(b) E and H distributions in an optimized balun

Figure 3.42: Comparison between a typical and an optimized baluns

the electric field is the responsible for this imbalance confirming the influence of the high capacitive coupling between the primary and the secondary and between the primary and the substrate. The retrieved energy by each half secondary is unequal. This phenomenon is always located in one turn balun and can be lowered:

- by decreasing the capacitive coupling to the detriment of the coupling coefficient.
- by interleaving the primary and the secondary to improve the symmetry coupling [117]. This method lowers the resonance frequency and increases the coupling area with the high-loss substrate.

Unlike the electric field, the magnetic field is distributed symmetrically to the secondary because of the constant current crossing over the primary.

An original idea to improve the balance performances of this balun is proposed. It consists in adding a serial capacitor at the end of the primary (cf. Figure 3.42(b)). This capacitor compensates the coupling (previously discussed). It also forces a non-zero voltage at the end of the primary to be coupled with the secondary at the resonance. Hence, a symmetric distribution of the electric and the magnetic fields in the secondary is set.

Typically, the Common Mode Rejection Ratio ($CMRR$), defined as the ratio between the differential mode and common mode, is calculated to evaluate the single-to-differential mode conver-

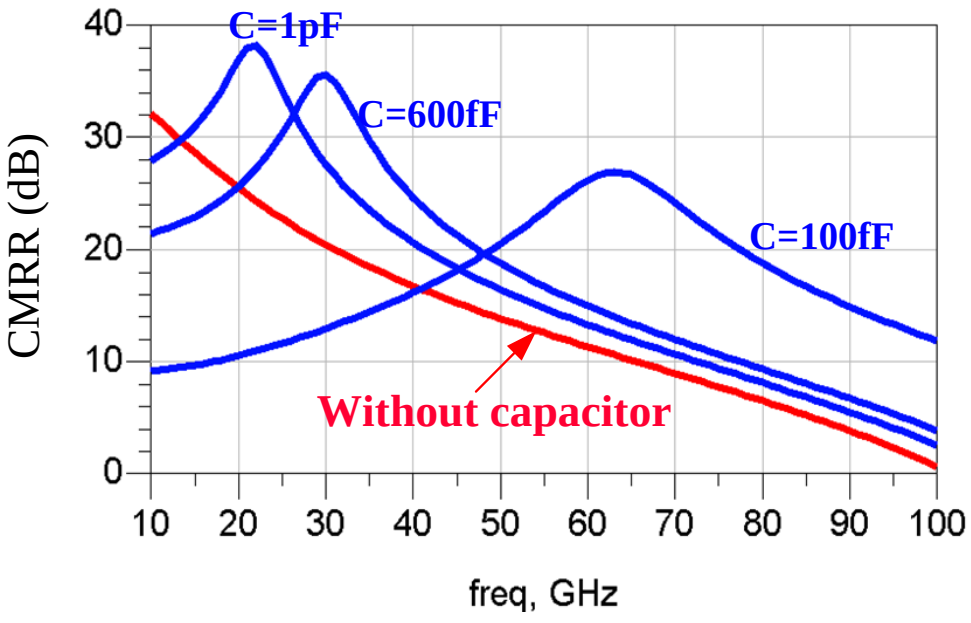


Figure 3.43: Influence of the capacitor on CCMR

sion balun performance. Figure 3.43 depicts the simulated $CMRR$ of the balun which is used in the PA and the optimized baluns. Up to 15GHz, the first balun (without additional capacitor) has a good $CMRR$ of 30dB. Furthermore, getting higher in frequency induces more losses due to the capacitive coupling and a considerably drop of the $CMRR$. Adding a capacitor to the end of the primary reduces the assymetry affects in a specific frequency band. Indeed, a capacitor of 1pF leads to an optimum operation of the balun at 23GHz. A capacitor of 100fF allows the balun reaching a $CMRR$ of 26dB at 60GHz instead of 12dB. As demonstrated in Figure 3.43, for the optimized balun, a frequency reconfigurable balun can be designed by tuning the added capacitor.

The optimized balun is integrated instead of the first balun. The PA is able to deliver up to 9.5dBm of P_{out}, and has an OCP_1 of 6.8dBm instead of 4.2dBm (cf. Figure 3.44).

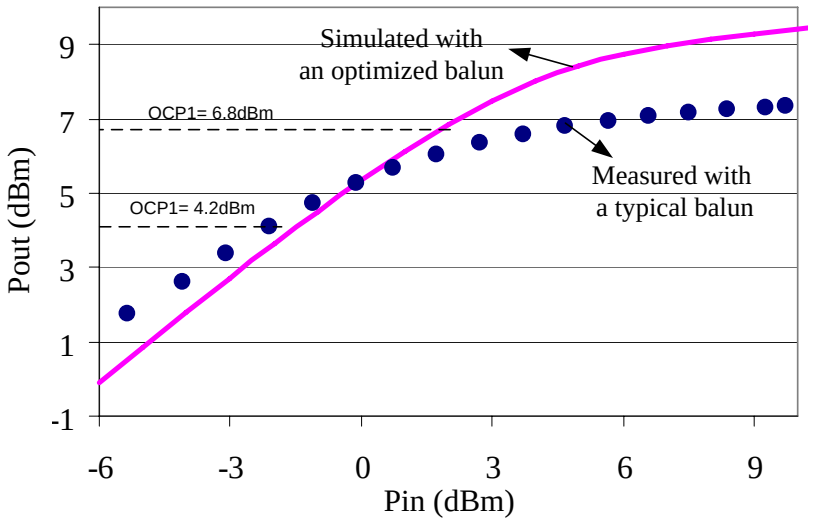


Figure 3.44: Simulated power transfer with the improved balun

3.4.4 Conclusion

For this PA realization, lumped elements based on compact baluns and distributed elements based on CPW lines are implemented. Small signal and large signal analyses of the PA are depicted. This PA offers a gain of 8.5dB in spite of using baluns at the input and the output of the PA. A critical point of view of the fabricated stacked balun is given concerning balanced-to-unbalanced conversion performances. Finally, an optimized high-performance balun is proposed contributing to the design of mmW frequencies circuits.

3.5 Comparison with the state of the art

The ITRS FoM is used to compare the PAs performances [121]. It considers the gain, the PAE, the P_{sat} and the operating frequency as given in Eq. 3.14:

$$FoM = P_{sat} \cdot Gain \cdot PAE \cdot f^2 \tag{3.14}$$

Three tables of comparison are presented separately to compare our PA performances with PAs found in literature as follows :

- Comparison of 60GHz CMOS PAs designed in single ended structure.
- Comparison of 60GHz CMOS parallel PA structure.
- Comparison of 60GHz PAs designed with different technologies.

- **Comparison of 60GHz CMOS PAs designed in single ended structure**:
  Table 3.7 exhibits performances of CMOS 60GHz PAs. The amplification is performed in a single way such as adopted for our PA design. Because of the presence of a restricted matching networks as a passive devices (without combining techniques), the power performances reflect directly the capability of transistors to deliver power at a given power consumption.

  These PAs use CA or CS transistor configurations. CA structure is adopted with the 130nm CMOS technology [56] [53]. This choice is relevant because of the low frequency performances of technology node (low f_t and f_{max}). The purpose is to prove the feasibility to provide a considerable gain at 60GHz in CMOS technology. However, these PAs suffer from bad linearity-efficiency trade-off resulting to a low FoM.

  Frequency and gain transistor performances are improved with the 90nm and 65nm CMOS technologies. The challenge is then set to provide high linear P_{out}. The use of CA structure is replaced in most of cases by the CS structure. The gain is not anymore the priority such as seen in [57], [62], [55] and [122]. In [122], the 4-stage PA achieves the best OCP_1 and P_{out}. This PA is designed with very big transistors which consume high DC power and thus the PA has a low PAE.

Table 3.7: Comparison of single-ended CMOS 60GHz PAs

[Ref]	[56]	[53]	[57]	[62]	[55]	[122]	[122]	Our work
Year	2004	2008	2007	2007	2008	2010	2010	2010
Processs (nm)	130	130	90	90	65	65	65	65
Freq (GHz)	60	60	60	56	60	60	58	63
Stages	3	5	3	2	1	1	4	2
Transistor	CA	CA Doherty	CS	CS	CS	CS	CS	CS
Passive	CPW	MS	Inductor	CPW	MS	MS	MS	CPW
P_{sat}(dBm)	-	7.8	9.3	7.5	8.5	9.2	14.2	10.6
Gain (dB)	12	13.5	5.2	8	4.5	4.5	13.7	13.2
PAE_{max} (%)	-	3	7.4	20	8.5	8	4.2	8.9
$OCP1$ (dBm)	-	7	6.4	6.7	6	6.4	12.2	9.2
$PAE_{@OCP1}$	-	< 1	4.6	16.5	-	8	3.6	7.1
DC (mW)	57	200	54	28	23	31	425	80
BW_{3dB} (GHz)	25	7	–	8	9	-	-	9
size (mm^2)	2.3	1.8	0.16	0.55	0.27	0.24	1.28	0.3
FoM (ITRS)	-	14.4	7.5	25	6.1	7	74	84

According to the ITRS FoM, our work is ranked as the best one. The PA is composed by only two stages. The driver and the power stages are accurately matched with the required impedances. It provides a high gain of 13.2dB, a high OCP_1 of 8.9dB with a low consumption. Hence, a good PAE of 9% is demonstrated. Moreover, since the 60GHz WPAN standard uses the OFDM modulation scheme, the PA operates in most of time at low power ranges. So, the PAE at the compression (PAE_{OCP_1}) is a crucial parameter to be considered. Our PA has a PAE_{OCP_1} close to the PAE_{max} making it convenient for this application.

- **Comparison of 60GHz CMOS parallel PA structure**:
  This technique is motivated by the limitation of CMOS to provide high P_{out}. Indeed, designing very big transistors at 60GHz in CMOS induces considerable losses and leads to a high sensitivity to impedances matching degrading its power performances. Hence, current and voltage combining techniques are used to improve P_{out} at the cost of additional passive device losses such as splitter and DAT.

Table 3.8: Comparison of parallel CMOS 60GHz PAs

[Ref]	[123]	[124]		[58]	[59]	[61]	Our-work	Our work (Load pull)
Year	2009	2009		2009	2010	2010	2010	2010
Processs (nm)	90	90		65	65	$65(10M)$	65	65
Freq (GHz)	60	60		62	60	60	63	63
Stages	2	2		3	2	2	2	2
Transistor	CS	CS		CS	CA	CS	CS	CS
Passive	Baluns	Spliter +CPW		Baluns	Spliter +Baluns	DAT Diff-Line	CPW	CPW
N-ways	2	4		2	8	4	1	1
P_{sat}(dBm)	12.3	14.2		11.5	16.6	17.7	10.6	12
Gain (dB)	5.6	4.2		15.8	14.3	19.2	13.2	14
PAE_{max} (%)	8.8	5.8		15.2	4.9	11.1	8.9	15
$OCP1$ (dBm)	9	12.1		2.5	11	15.1	9.2	10
$PAE_{@OCP1}$	5.8	5.8		5	< 2	7	7.1	13.2
DC (mW)	88	145		50	732	460	80	65
BW_{3dB} (GHz)	–	11		-	15	–	9	–
size (mm^2)	0.25	1.19		0.05	0.825	0.46	0.3	0.3
FoM (ITRS)	19	14		313	217	1957	84	237

Table 3.8 exhibits performances of CMOS 60GHz parallel PAs. Due to the poor knowledge of the 65nm CMOS technology, most of PA realizations are performed with the 90nm CMOS technology. The references [123] and [124] have two and four amplification ways using baluns and current combiners, respectively. These devices generate high losses due to the high impedance transformation ratio. Those PAs are still suffering from low PAE, low gain and thus, a low FoM.

In ISSCC 2010, the most relevant 60GHz PAs designed with the 65nm CMOS technology are presented. In [59], a 8-ways splitter is implemented. Each way excites a balun which is connected to a differential PA. Consequently, 16 transistors mounted in CA configuration

operate simultaneously. The PA achieves a P_{sat} of 16.6dBm but still suffers from low PAE due to the high overall DC consumption.

In [61], the best FoM is demonstrated exhibiting higher performances in terms of linearity, gain and efficiency. It is important to underline that this PA is not designed with the standard process of 7 Metal levels. This PA is routed using digital process option with 10 metal levels. Hence, passive devices exhibit high Q overcoming from many design issues. Our PA is still competitive with parallel PAs after performing load pull measurements.

- **Comparison of 60GHz PAs designed with different technologies**:
  According to the state of the art of 60GHz CMOS PAs. It is important to compare CMOS PA performances with the ones realized with other technologies. Table 3.9 exhibits performances of 60GHz PAs using GaAs, BiCMOS, SOI and CMOS technologies.

Table 3.9: Comparison of 60GHz PAs designed with different technologies

[Ref]	[125]	[126]	[65]	[64]	[61]	Our work(LP)
Year		2009	2009	2010	2010	2010
Technology	GaAs-PHEMT	SiGe	SiGe	SOI	CMOS	CMOS
Node (nm)	150	130	250	65	65	65
Freq (GHz)	60	60	61	60	60	63
Stages	3	4	2	2	2	2
Transistor	-	CS	CA	CA	CS	CS
Passive	-	SCPW	-	CPW	DAT	CPW
N-ways	2	2	2	1	4	1
P_{sat}(dBm)	25	18.8	15.5	10.5	17.7	12
Gain (dB)	17	18.3	18.8	14	19.2	14
PAE_{max}(%)	26	9.8	19.7	22.3	11.1	15
$OCP1$ (dBm)	23	13.5	14.5	7.1	15.1	10
$PAE_{@OCP1}$	25	3	–	12.5	7	13.2
DC (mW)	1625	560	132	33.6	460	86
BW_{3dB}(GHz)	12	7	–	–	–	–
size (mm^2)	10.6	1.12	–	0.57	0.46	–
FoM (ITRS)	15333	1809	1972	228	1957	237

CMOS and SOI technologies have similar performances to provide power. The main advantage in SOI technology is the high resistivity of the its substrate which leads to get higher Q of passive devices. Consequently, the PAE of the SOI PA is not so degraded such as in CMOS PAs. The use of process option in CMOS like in [61] keeps the CMOS technology competitive with BICMOS technology as demonstrated in [126] and [65]. In [125], the mature 150nm GaAs-PHEMT technology is used for the PA design. It exhibits much better performances in terms of gain, linearity and efficiency at the cost of a big die area and power consumption. These constraints represent a significant disadvantage for WPAN applications since it is dedicated to be integrated in handset products.

3.6 Future works

3.6.1 Co-integration PA/emmiter in SoC configuration

The *NANOCOMM* ANR project is intended to investigate in the *Internet of terminals* topic and more specifically in the integration of heterogeneous 3D miniaturized sensors modules into wireless communication and multi-network, multi levels architectures. It targets realizing high speed, low cost and low consumption communication systems. Thus, advanced CMOS technology, advanced MEMS are used. LAAS and IMS laboratories are partners to explore the 60GHz band for HD video application. IMS laboratory is in charge of designing 60GHz 65nm CMOS PA while the LAAS laboratory is in charge of designing a VCO and a mixer to realize a complete CMOS emitter (Figure 3.45).

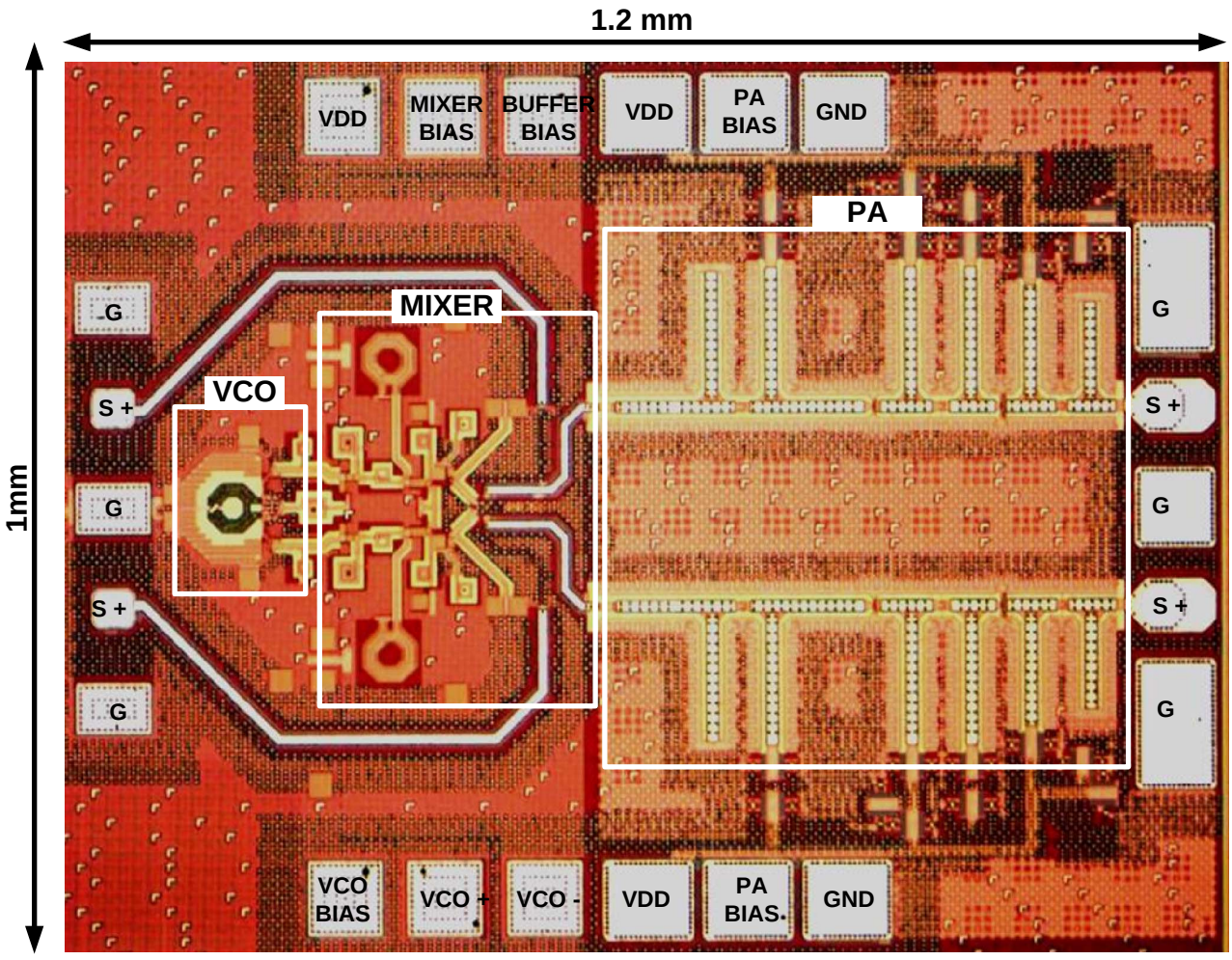


Figure 3.45: PA integration in the NANOCOM emitter

According to the presented single-ended PA, a pseudo-differential PA is designed in order to achieve higher P_{out}. The design is still similar to the first one. Only the input matching is changed by replacing the input RF-pad by a MiM capacitor. Theoretically, the PA is intended to provide additional 3dB of OCP_1 and P_{sat} keeping the same gain and PAE as the first PA (Figure 3.46). Table 3.10 summarizes the simulated performances of the pseudo-differential PA. The complete emitter is fabricated and it is scheduled to be measured.

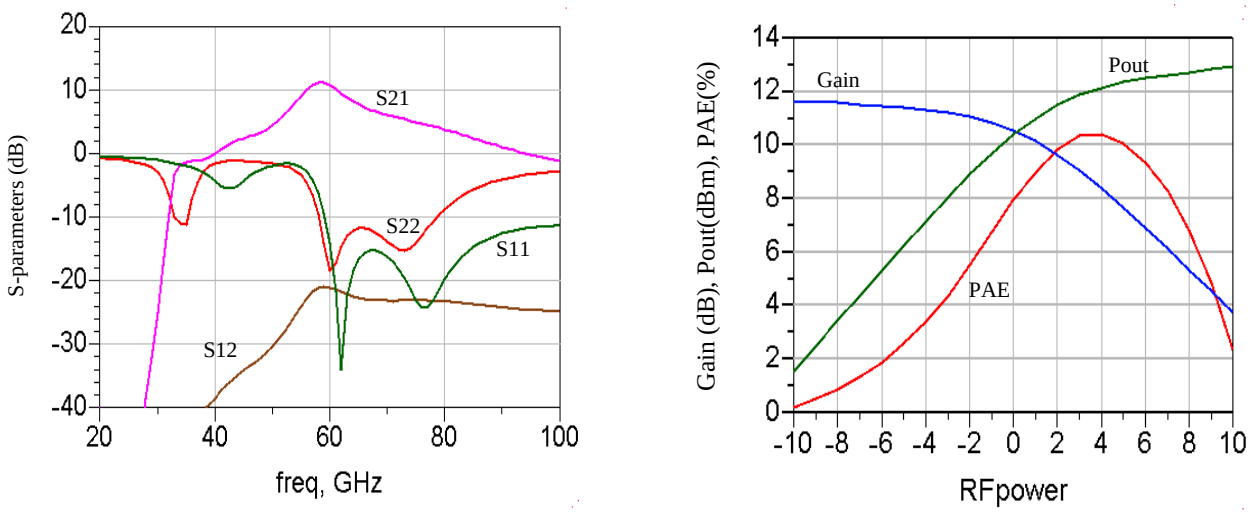


Figure 3.46: Simulated S-parameters and power performances of the pseudo-differential 60GHz PA

Table 3.10: Large signal pseudo-differential PA performances

	Gain(dB)	P_{sat}(dBm)	$PAE(\%)$	$OCP1$(dBm)
Pseudo-differential PA	12.2	13.2	11.3	11.2

3.6.2 Co-integration PA/transceiver in SiP configuration

A CMOS transceiver demonstrator is targeted in the frame of the *MEDEA+ QSTREAM* project. The main activities are the design, the fabrication and the measurements of complete CMOS RF transceivers and building blocks for the RX/TX functionality from 60 GHz to digital base band. In addition to that, SiP implementations enabling *mmW* front-end containing antenna arrays is scheduled. One of the main purpose of this project is to avoid external expensive III-V PA. IMS laboratory is involved in that partnership to design a 60GHz CMOS PA for the transceiver to be integrated in flip-chip configuration (Figure 3.47).

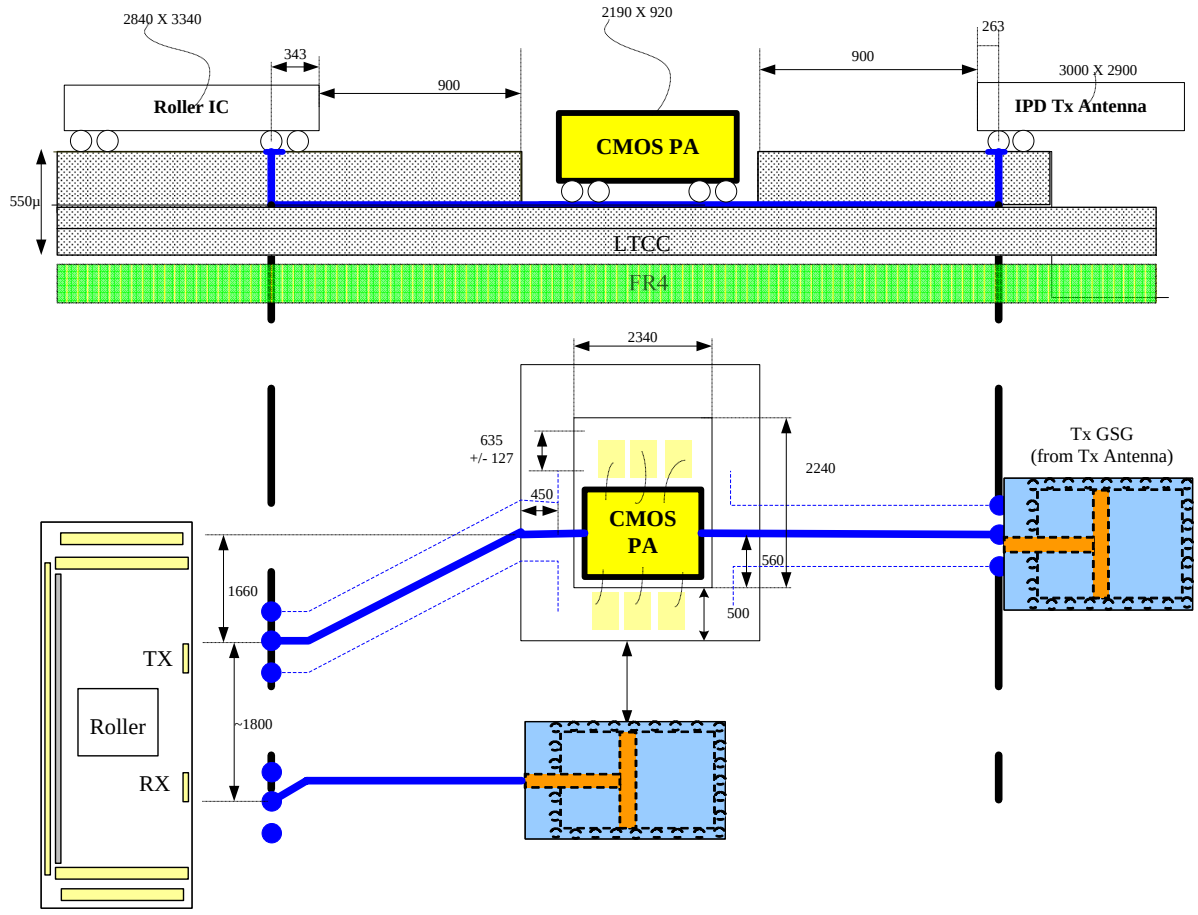


Figure 3.47: PA integration in the QSTREAM transceiver

According to the state of the art, it can be underlined that a single-ended or differential structure are still insufficient to achieve high power levels as it is the case for commercialized GaAs PAs. Hence, the design of a parallel PA is part of the solution. The PAs presented in [59] and [61] contain a DAT or a current combining structures. Despite they exhibit good results, they still suffer from low PAE as seen in [59]. Our PA design flow was to optimize as much as possible a PA based on single-ended structure, in a first time. It has already a comparable performances with existing parallel PAs. Hence, It is promising to use this PA in a parallel configuration. The main requirement of *MEDEA+ QSTREAM* is to fabricate a functional 60GHz PA with an optimum trade-off between size-cost with the respect to system performances. According to our experience, we target a linear behavior of the PA until 15dBm with a minimum PAE of 10%.

3.7 Conclusion

Chapter 3 presents our contribution in designinig *mmW* PAs. In the first part, the key design procedures for a generic *mmW* PA are exposed. The PA topologies, transistor modeling and matching issues are mentioned. Moreover, a particular interest is focused in the analysis of the PA stability.

In the second part, detailed characterization and optimization of active device is presented to complete the passive optimization work which is presented is chapter 2. A single ended 60GHz 65nm CMOS PA is described depicting simulation and measurement results. This PA is functional in the useful band and offers a high gain. Moreover, a good trade-off between gain, linearity and efficiency is met. The PA performances are also improved using load-pull measurements. This successful realization is also performed thanks to preliminary designs which are presented briefly. In this context, ground connections, RF-pads and interconnect elements effects are highlighted to avoid a frequency shift response and a gain drop.

In the third part, the design of differential PA is presented. Before describing the PA design, the analysis and the comparison between basic coupling structures are compared. The implemented baluns perform simultaneously matching impedances and single-to-differential mode conversion. The small signal measurement results fulfill the gain and the impedance matching requirements. However, measured linearity performances do not fit with the expected ones. Hence, an original method based on EM simulations is presented. It demonstrates that the balun imbalance is responsible for the linearity degradation. Thanks to this analysis, an novel optimized balun is proposed to overcome the imbalance issues.

The fourth part demonstrates a state of the art of 60GHz PAs. Our PA is compared with other ones designed with the same topology. It exhibits the best FoM. After, our PA is compared with other PAs adopting parallel amplification. Finally, CMOS PAs are compared with the ones designed with competitive technologies such as SOI, BICMOS and GaAs technologies.

The chapter is concluded by presenting the future works. The presented work is in the frame of the European *MEDEA + QSTREAM* and the *NANOCOMM* ANR projects. The PA is integrated in a differential configuration in the 60GHz *NANOCOMM* emitter in SoC configuration while a parallel PA is scheduled to be integrated in the *QSTREAM* transceiver in SiP configuration.

Conclusion

Our thesis contribution aims at designing 65nm CMOS 60GHz PAs. Downsizing CMOS technology enables at integrating circuits operating at mmW frequencies. In one hand, transistors must be optimized to satisfy the gain-linearity and power consumption trade-off. In the other hand, passive devices suffer from low quality factor due to the thin 65nm CMOS BEOL. The combination of poor gain of the transistor and low quality factor of passive devices at 60GHz makes the PA design challenging to fulfill WPAN specifications. During the PA design, the linearity and power consumption are the major parameters taken into interest. The PA fundamentals and design requirements are reminded in chapter 1.

The optimization of passive devices is performed before the PA design in chapter 2. Accurate passive device models are developed to master their effect. Firstly, an investigation is brought into play to perform rapid EM simulations for 65nm CMOS BEOL. This work is based on EM simulations to take into account the skin effect, the substrate loss, the ground connections and the proximity effects. Secondly, a description of data post-processing using calibration and de-embedding methods are presented to make an appropriate comparison between simulation and measurement results. Finally, passive device characterization and optimization are presented. A particular interest is brought to propagation structures such as T-lines, inductors and RF-pads.

Concerning T-lines, microstrip lines are compared with coplanar wave-guide lines. Their electric performances and also non-common aspects as coupling issues are analyzed. According to EM simulation, coplanar wave-guide line are retained to be integrated in the PA design. The major advantage is their higher isolation to neighbor components compared to microstrip lines. Their characterization is validated by experimental results.

Concerning inductors, two types of inductors are studied namely, the octagonal and the square ones. During their analyses, it is demonstrated that a pattern ground shield affects their performances due to the thin BEOL of the 65nm CMOS technology. Other non-common aspects such as the return current path is analyzed highlighting its effect in two square inductors. In our PA design, the inductors are not used since they generate coupling issues in the chip environment.

Additionally, 60GHz design does not require high inductance. In this context, it is demonstrated that such low inductance suffers from low quality factors as T-lines.

Concerning RF-pads, two optimized RF-pad structures are proposed for mmW design. In fact, a typical RF-pad which is commonly used for RF applications is not anymore functional at mmW frequencies. So, a particular interest is brought to point out their parasitics to develop an accurate model. A shielded RF-pad and a non-shielded RF-pad are proposed. The shielded RF-pad exhibits a high capacitance and a high quality factor while the non-shielded RF-pad exhibits a very low capacitance and a low quality factor. The design of RF-pads is faced to parasitics and quality factor trade-off. The choice of the RF-pad is justified.

The design of PAs is presented in chapter 3. The design flow of a generic mmW PA is presented. The choice of the PA topology, the power stage design and the driver stage design are given under power, gain, consumption and stability constraints. The characterization and the optimization of active devices are presented. Indeed, a poor knowledge of the transistor behaviour causes issues concerning the linearity and efficiency performances. During the characterization of the designed transistors, small signal and large signal analysis are performed thanks to an Agilent mmW VNA (10Mhz to 110GHz) and a Focus load pull system operating from 58GHz to 90GHz. After an improvement in terms of model accuracy of the 65nm CMOS DK, two functional PA are presented.

A single ended PA is designed and measured. It offers a high gain of 13dB assuring a bandwidth of 9GHz. Moreover, the PA guarantees simultaneously good performances in terms of linearity and efficiency exhibiting 9dBm of OCP_1 and 9% of PAE. The PA is enlisted in a state of the art and exhibits the highest value of the ITRS FoM compared with other PAs designed with the same topology. The PA is also competitive with other PAs designed in parallel topology using current and voltage combining techniques. In addition to that, the power performance of the designed PA are also improved by performing load pull measurements. It achieves 14dB, 12dBm and 9.2dBm of gain, P_{sat} and OCP_1 respectively and offers a maximum PAE of 15%.

A second PA is designed using differential topology. Two stacked baluns are integrated at the input and the output of the PA. They perform both impedance matching and single-to-differential mode conversion. The PA is measured and operates in the desired band with a gain of 8dB. However, it demonstrates worse power transfer performances than the predicted ones due to the low CMRR of the designed baluns. Those issues are analyzed with an original method using electric and magnetic fields amounts. Finally, a novel balun design is proposed. It exhibits an improvement of the CCMR achieving till 26dB at 60GHz.

During this work, several *mmW* CMOS technology designs are presented. Namely, T-lines, RF-pads, inductors, baluns, transistors are optimized before realizing different PAs. Design issues are also presented, analyzed and solved. Measurements have paved the way to an industrial implementation in the *NANOCOMM* and the *QSTREAM* projects. This work is promising for the interest and the investigation in CMOS technologies to be integrated in the design of *mmW* PAs in the future.

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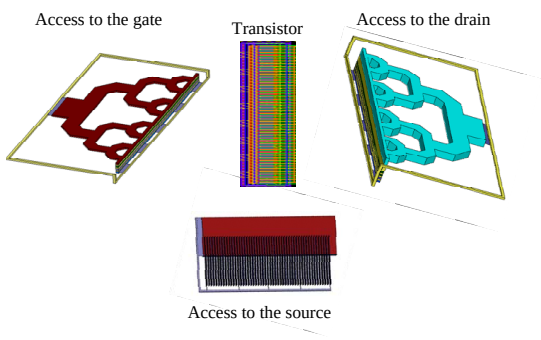
Appendix

A Preliminary PA design - Circuit 1

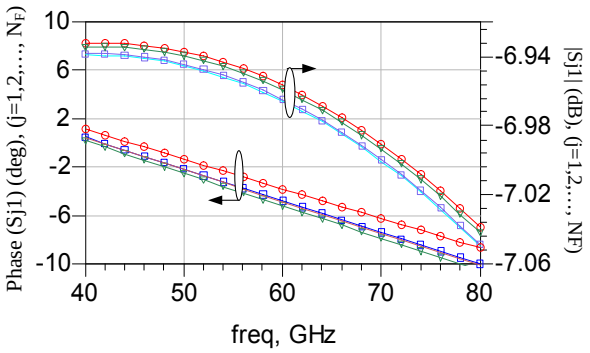
Contents

A.1 Active device

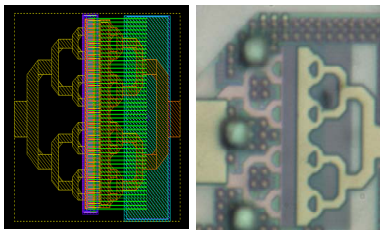
The driver transistor is set to $(W_f, N_f, N_c) = (1\mu m, 100, 1)$ and the power transistor is set to $(W_f, N_f, N_c) = (1\mu m, 100, 2)$. The transistor routing aims at reducing C_{gd} and C_{gd} in order to maximize the isolation ($S_{12} \searrow$) and f_t. An equal distance access to the transistors pins was respected to guarantee signals coming from all transistor fingers in phase and magnitude. The accesses to the gate, the drain and the source are simulated with Ansoft HFSS electromagnetic simulator and represented by S-parameters blocks. The parasitic capacitances between each 2 accesses (C_{gd}, C_{gs} and C_{ds}) are calculated using Cadence extractor tool. The simulated transistor accesses demonstrate a uniform distribution of the signal for different fingers ($\Delta\varphi \to 0$ and $\Delta|S_{j1}| \to 0$) in Figure A.1(a), (b). Figure A.1(c) depicts layout and die micrography of the



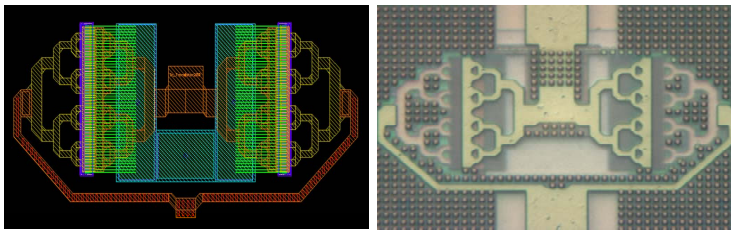
(a) Simulation of transistor accesses with HFSS



(b) Simulated magnitude and phase of different transistor fingers



(c) Driver transistor layout and die photography
(W_F, N_F, N_C)=(100um, 100, 1)



(D) Power transistor layout and die photography
(W_F, N_F, N_C)=(100um, 100, 2)

Figure A.1: Design of the power and driver transistors

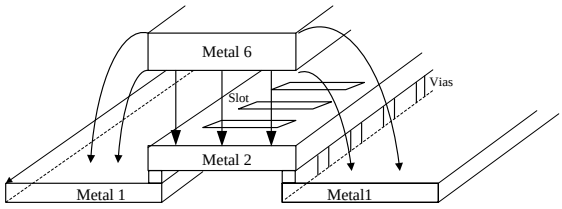
realized driver and power transistors.

A.2 Passive device

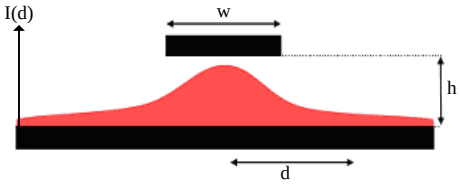
This PA is designed with lumped elements. 80pH inductor is the lowest inductance provided by the 65nm DK from STMicroelectronics. Details about its structure and its performances are presented in section 2.2.2. For coupling issues, it is forbidden to place closely any component near the inductor. So, non neglected T-lines assure interconnections between an inductor with neighbor components. Hence, the whole inductor and T-lines are considered in simulations. MS lines suffer from high capacitive coupling and CPW lines consume a large area. Therefore, slow-wave structure is preferred. This configuration is illustrated in Figure A.2(a). It aims at minimizing both substrate losses and capacitive coupling. The RF signal spreads over the Metal 6 and the return current over the Metal 2. Eq. A.1 presents the distribution of the current in the ground plan of MS lines plotted in Figure A.2(b).

Metal 1 is connected with metal 2 by their extremities in order to retrieve the remainder of electromagnetic fields. Slots in the ground plan change the return current direction as depicted in Figure A.2(c). The intrinsic inductor increases, thereby reduces the wavelength which is beneficial to reduce the interconnect access length.

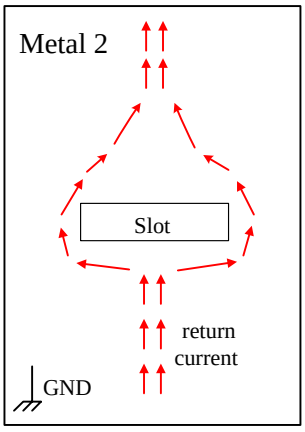
$$I(d) = \frac{I0}{\pi h} \cdot \frac{1}{1 + (\frac{d}{H})^2} \tag{A.1}$$



(a) Slow-wave line structure



(b) Return current distribution in MS lines



(c) Return current path

Figure A.2: Customized T-line structure

A.3 PA description

The fully integrated 60GHz PA is a single-ended two-stage common-source structure (cf. Figure A.3). The first stage is biased by an external tee polarization (LT, CT) and the second stage is biased with a current mirror. The PA is optimized to deliver a maximum of linear power. Both two stages are supplied with 0.9V and biased with 1V. The PA input and output impedances matching are set to 50Ω. Whole inductors (I1, Id1, I2, Id2), T-lines (L1, ..., L5) and MoM capacitors are used for impedances matching and decoupling. The chip size is $0.48*0.6mm^2$ including pads as shown in the layout view (cf. Figure A.4).

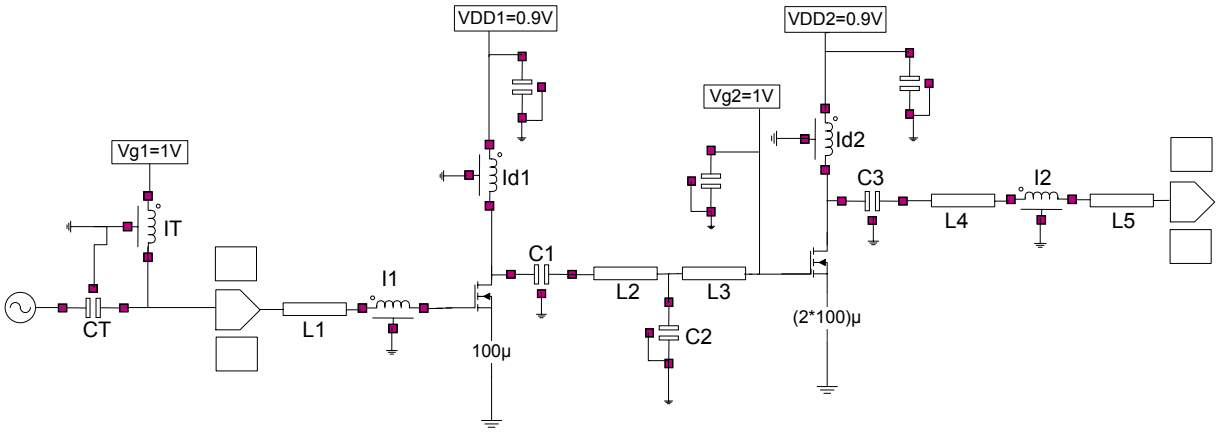


Figure A.3: Schematic of the 60GHz PA in 65nm CMOS technology

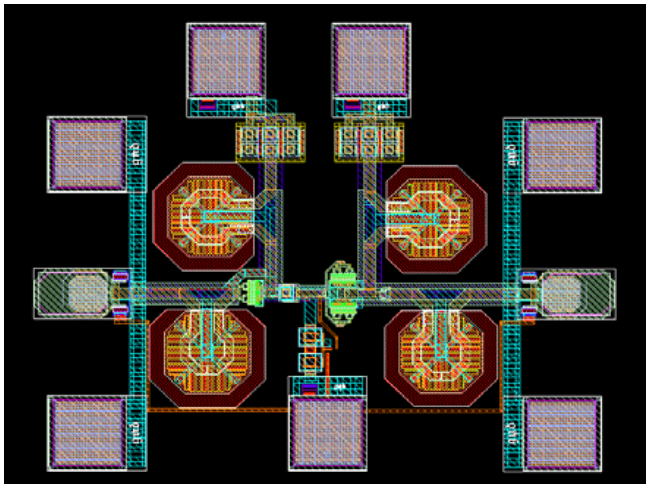


Figure A.4: Die photography of the fabricated 60GHz PA in 65nm CMOS technology

A.4 Simulation and measurement results

A.4.1 Simulation results

Figure A.5 presents the simulated S-parameters and power transfer characteristic of the PA. The PA was designed to operate from 57GHz to 64GHz frequency range. The return loss (S_{11}) of the PA is less than -10dB in all the useful band (from 57GHz to 64GHz) with an isolation (S_{12}) of -22dB at 60GHz. The simulation exhibits a maximum gain S_{21} of 8dB. At large signal operation, thanks to high bias current of 62mA, the PA achieves an OCP_1 of 8.9dBm, a PAE$_{max}$ of 11% and a P_{sat} of 13dBm.

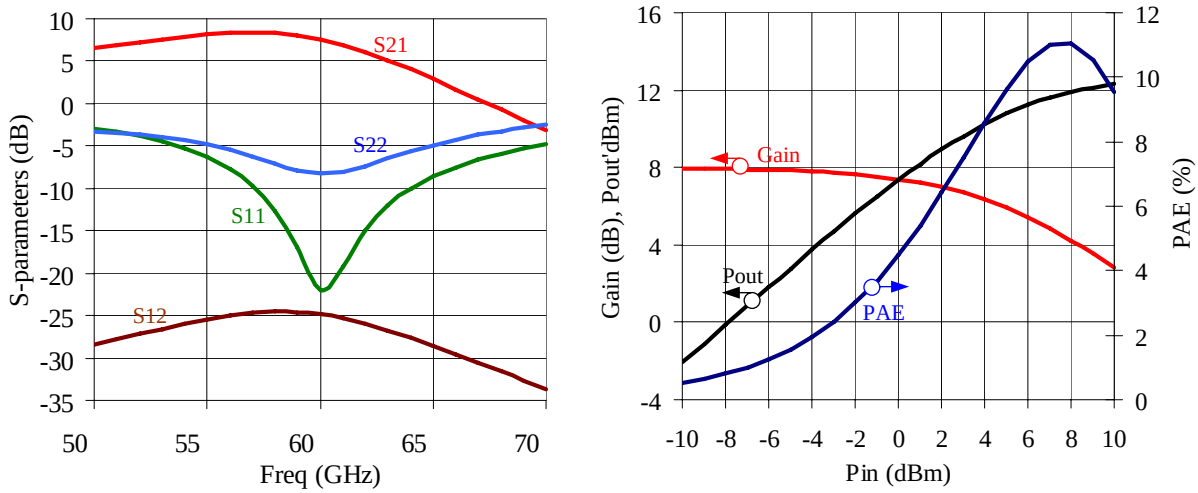


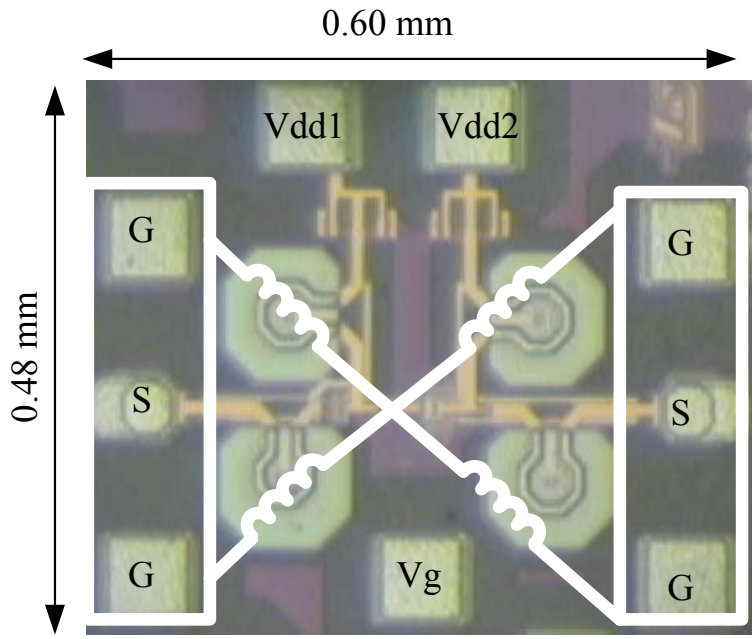
Figure A.5: Small and large signal simulation results of circuit 1

A.4.2 Measurement results

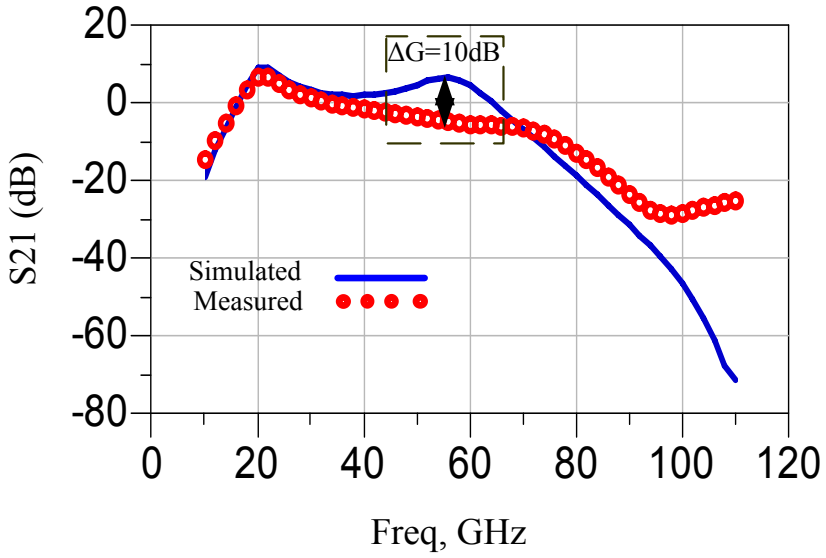
The PA is characterized by means of on-wafer measurement with a VNA for S-parameters from 10MHz to 110GHz. Figure A.6(b) compares the simulated and the measured gain. The two stages consume the expected DC current and the PA is matched at 60GHz. The PA does not provide the expected gain of 8dB. Indeed, the measurement results fit with simulation results till 40GHz. The PA has a first gain peak at 25GHz as expected on simulation but exhibits 10dB lower than expected at 60GHz.

A.4.3 Discussion

The PA gain decreases continuously with the growth in frequency and is not functional at 60GHz. As a result, the circuit is accurately analyzed by investigating redo simulations in order to determine the reasons of this dysfunction. The design errors made during the PA simulations



(a) Die photography of the circuit 1 highlighting neglected areas



(b) The gain of the circuit 1

Figure A.6: Die photography and comparison between simulated and measured PA gain

are illustrated in the layout view (cf. Figure A.6) and described as following:

- **Pad resonance**: the used RF-pad has an important intrinsic capacitance and inductance. Its intrinsic resonance frequency leads acting as a low-pass filter at the input and the output of the circuit reducing considerably the gain. More details concerning the pad model and resonance are given in chapter 2.

- **Bad current evacuation**: there is no GND-pad in the circuit. Consequently, the overall current is evacuated by the GND-pads of the RF-pads. As the return current path is very long and resistive, the ground is not well distributed and not well defined in the circuit. The most important issue concerns the ground connection with the transistor source. Indeed, connecting the transistor source to an important inductance creates a source degeneration reducing dramatically the gain. During simulation setup, this phenomena has not been observed since every component were connected to a perfect ground which is not true, according to the PA layout.

After considering those imperfections, redo simulation are performed. The results are in compliance with measurement results as depicted in Figure A.7.

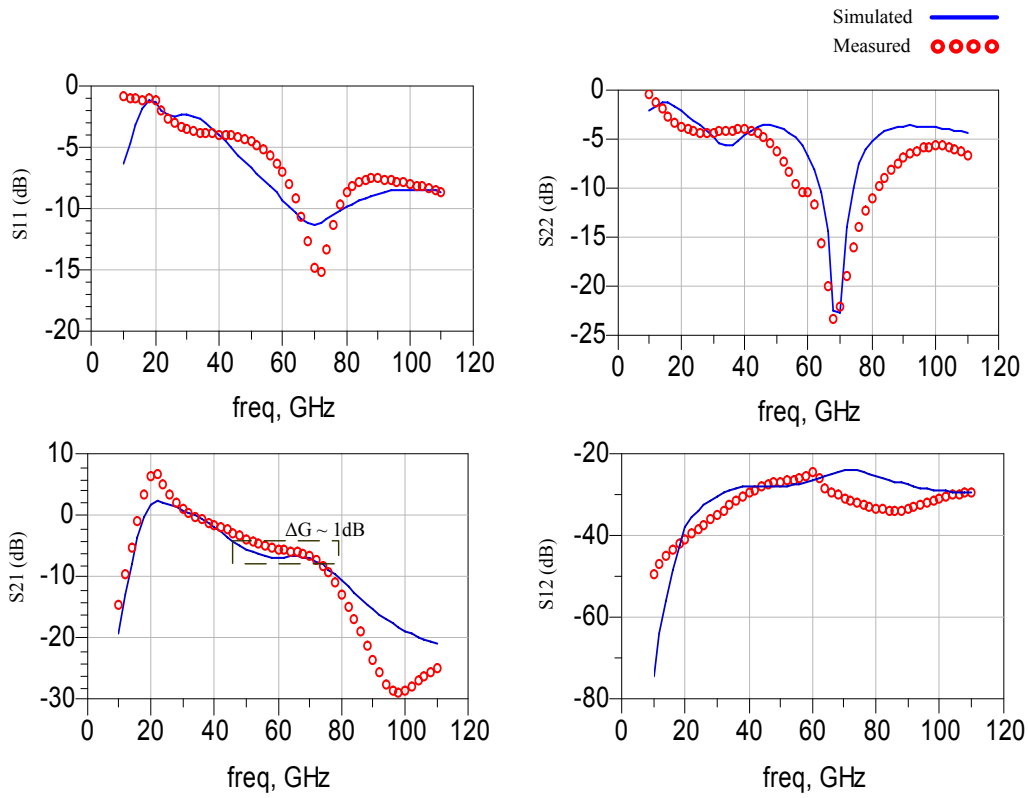


Figure A.7: Validation of redo simulation results with measurement results

A.5 Conclusion

A first realization of a 60GHz PA is presented in this section. The PA is matched with a mixed technique, using lumped and distributed elements. The simulation setup is enable to predict as well the PA behavior till 40GHz. With the growth in frequency, the assumptions that a RF-pad and the ground connections do not affect the PA performances are not available anymore. Consequently, the measurement results do not fit with simulation results depicted by a drop in gain at 60GHz. After considering those effects, redo simulation results fit with measurement results and valid our analysis. This realization allows the validation of passive active device modeling.

Appendix

B Preliminary PA design - Circuit 2

Contents

B.1 PA description and results

The fully integrated PA is a single-ended two-stage common-source structure. The power transistor is described before and the transistor of the driver stage has a width of $48*1\mu m$. Both of them are biased in the same condition $(V_{gs}, V_{dd}) = (0.95V, 1.2V)$ to have a maximum g_m. The two stages are biased by T-lines that also feature the matching since a RF-short is presented to the targeted length of the T-line. The short is made thanks to MiM capacitor of 3pF. MiM capacitors are exclusively used to perform DC blocking and supply decoupling. They offer a better Q compared to MoM capacitors. Their values are set to roughly 150fF and 3pF respectively. The output matching transforms the impedance from 50Ω to the optimum impedance determined to obtain P_{max}. The driver stage is matched to its conjugate impedance to offer the maximum gain. The input impedance is matched to 50Ω. Thanks to the absence of serial lines, the PA takes place within a compact silicon area of $0.29mm^2$ with pads. Figure B.1 and Figure B.2 show the schematic and the die photography of the PA. The ground of the circuit is distributed in all metal layers to reduce significantly the resistive and inductive effects of the ground connections. Additionally, all ground surfaces are connected to the substrate by the contact vias.

B.1.1 Small signal performances

Measured S-parameters are reported in Figure B.3. The PA has a gain of 5.7dB with an input reflection parameter S11 of -13dB. A shift at higher frequencies of 5% is noticed. Indeed, S_{21} reaches a maximum of 6.7dB at 69GHz and is equal to 5.7dB at 63GHz. The PA offers a BW-3dB of 22GHz. At 69GHz, the input matching exhibits a -17dB return loss whereas S_{22} is measured to -7dB. The isolation parameter is more than 25dB from DC to 110GHz. This shift is due to the over-estimation of the inductive effect in the T-junction interconnect, used six times in the circuit.

Indeed, the use of T-Lines for biasing and matching leads the RF signal crossing over this line. Consequently, T-junction are considered in the design of the PA to avoid frequency shift since

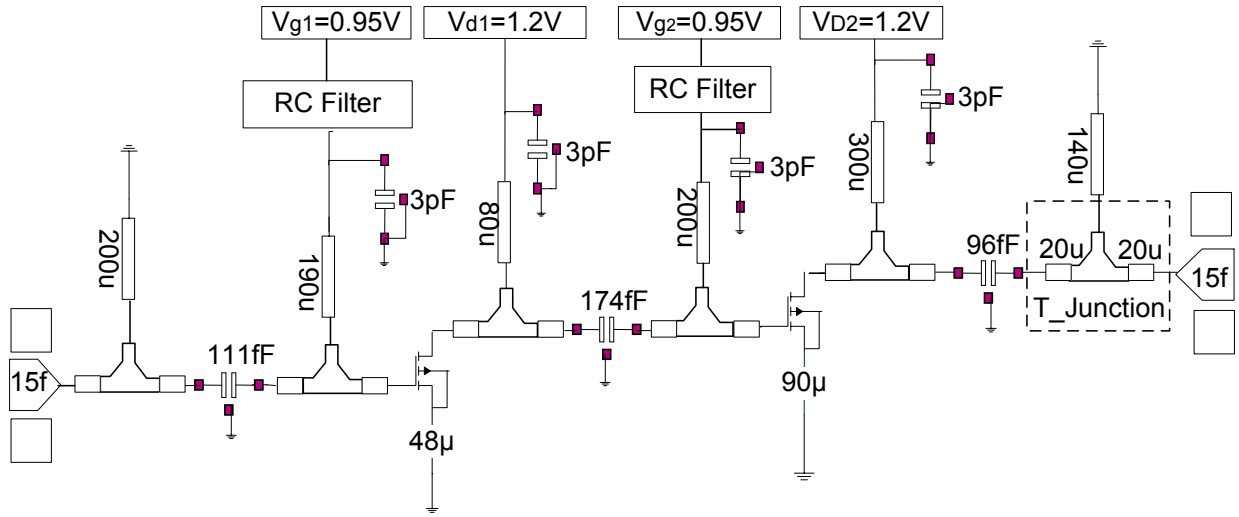


Figure B.1: Schematic of the fabricated 60GHz circuit 2

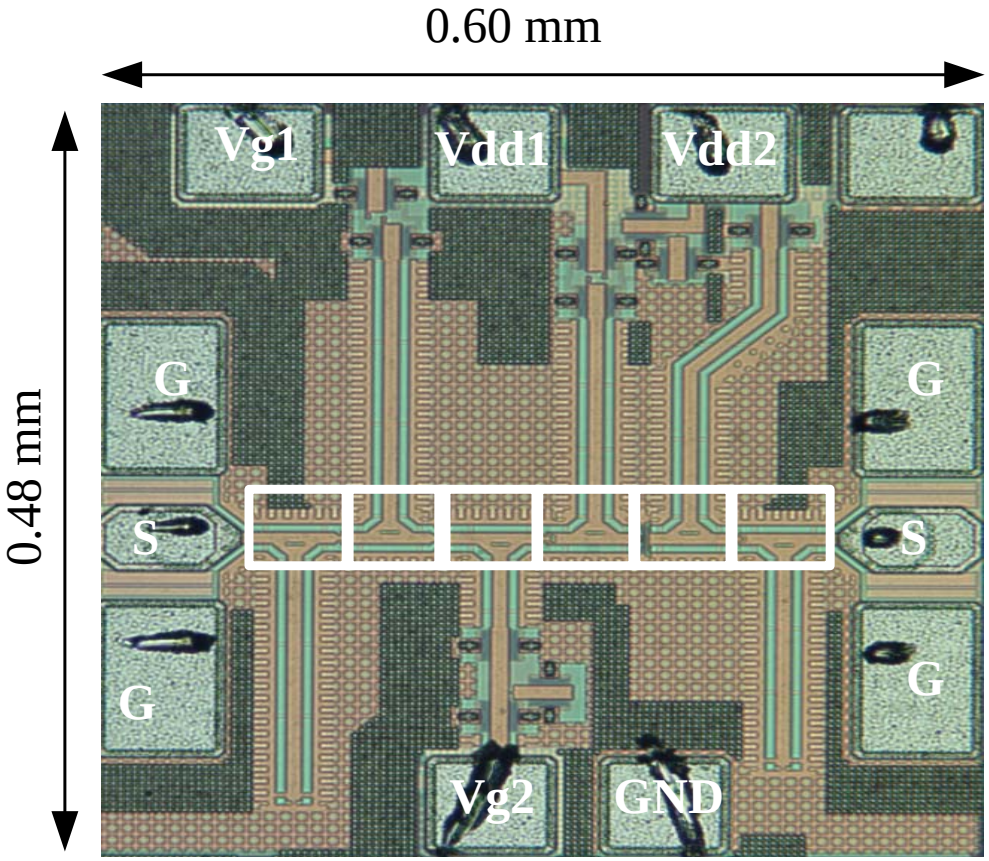


Figure B.2: Die photography of the circuit 2 highlighting neglected areas

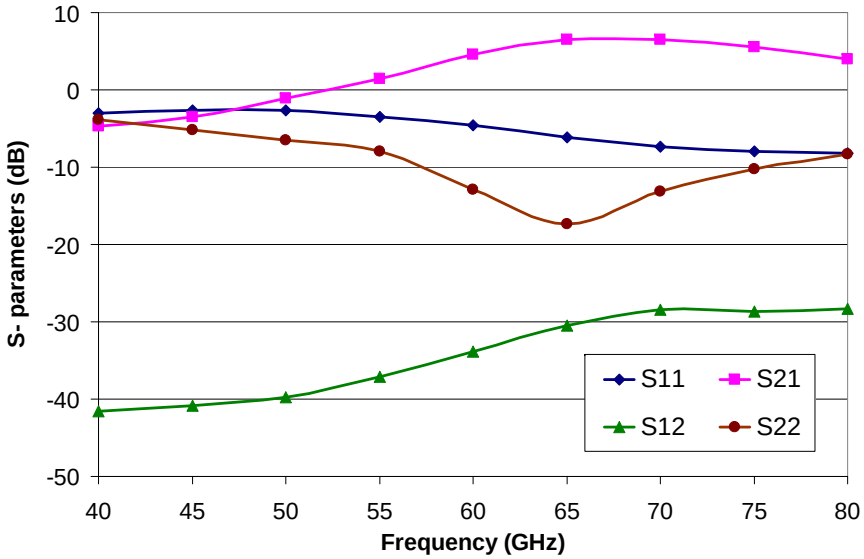


Figure B.3: Measured S-parameters at the bias point $(V_{gs}, V_{ds}) = (0.95V, 1.2V)$

they have parasitic capacitance. Figure B.4 confirms that the current flows mainly on the corners. This phenomenon is amplified by the skin effect which is responsible for the high current density concentrated on the edges of the line. A part of the metal in the center of the T-junction is cut in order to decrease the parallel capacitance. It has an inductive effect with serial resistive losses and a capacitance in parallel at the middle of the junction. This model is taken into account in the simulation schematic. However the inductive effect has been overestimated to 15pH instead of 5pH.

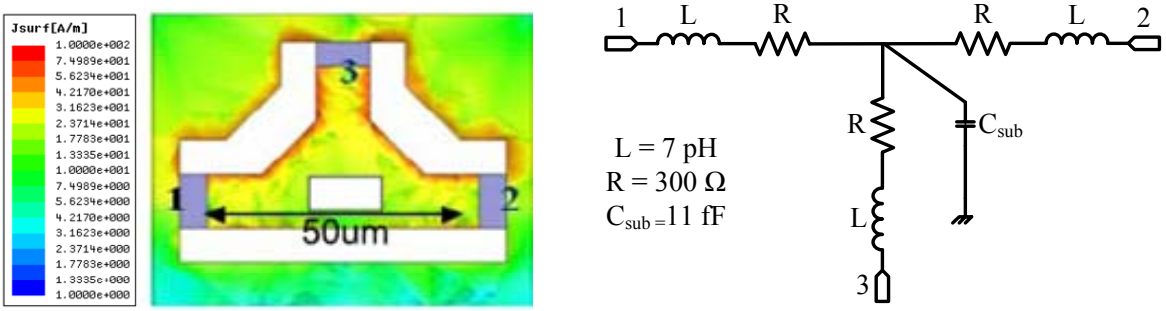


Figure B.4: Tee junction current distribution and its lumped model

B.1.2 Large signal performances

Large signal measurement results at 63GHz and 69GHz are exhibited in Figure B.5 with 50Ω at input and output. It summarizes the power characteristics. Thanks to the high bias current, the PA has an OCP_1 of 5dBm, 6.3dBm and a saturation power of 8.2dBm, 8.3dBm at 63GHz and 69GHz respectively. This design has a maximum drain efficiency of 12% at 69GHz in the compression region.

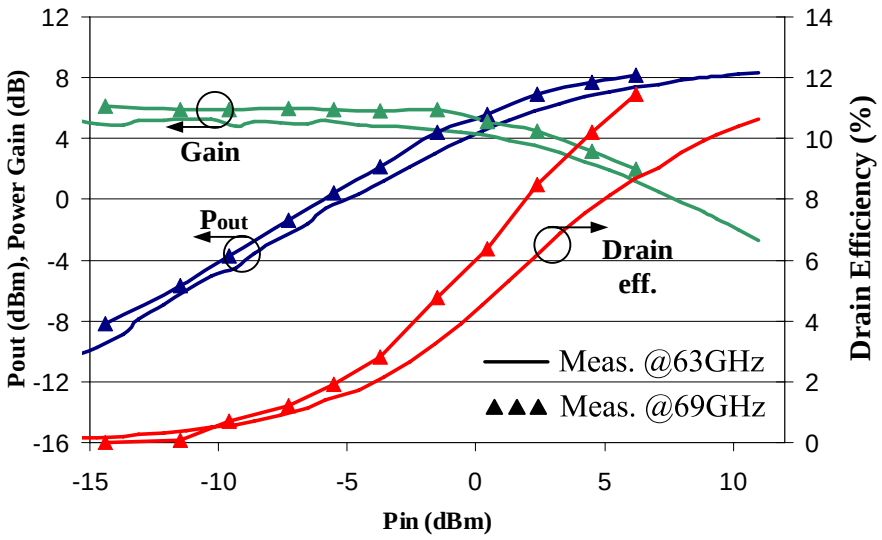


Figure B.5: Measured P_{out}, gain and η_d at 63GHz ans 69GHz at $(V_{gs}, V_{ds}) = (0.95V, 1.2V)$

B.1.3 Performance improvements with load pull setup

Thanks to load pull measurements, the optimum input and output impedances of the PA are presented at 63GHz. The power performances are plotted in Figure B.6. P_{sat} and OCP_1 remain constant while the gain and PAE are improved, as seen in Table B.1.

Table B.1: Large signal PA performances

$(Z_{in}, Z_{out})(\Omega)$	Gain (dB)	P_{sat} (dBm)	PAE (%)	$OCP1$ (dBm)	consumption mA@Volt
(50,50)	5.7	8.2	4	5	48@1.2
(Z_{Sopt}, Z_{Lopt})	7	8.2	6.4	7	48@1.2

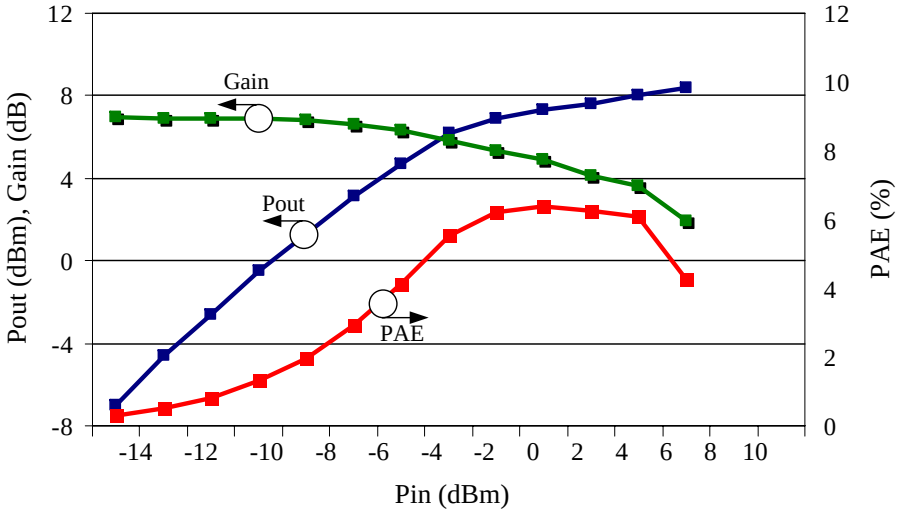


Figure B.6: Measured P_{out}, gain and PAE at 63GHz and 69GHz at $(V_{gs}, V_{ds}) = (0.95V, 1.2V)$

B.2 Conclusion

The design flow and measurement results of a fully integrated PA are presented. DC, small signal and load pull analysis of the power transistor are demonstrated. More considerations are taking into account in this realization compared to the first PA design. Indeed, the layout process is optimized. The RF-pads and the distributed ground plan overcome to ground connection issues met in the first PA design. In addition to that, CPW lines are well characterized and offer more flexibility in the design. This PA exhibits a good trade-off between gain and linearity. Only Tee-junction are overestimated and thus a shift of 6% is seen in S-parameters measurements. Thanks to load pull measurements, the PA gain and PAE are improved. The overall chip size is $0.29mm^2$ with pads.

Appendix

C PA Characterization for OFDM modulated signal

Contents

The PA can be considered as a non-linear generator which disturb other components such as VCO by pulling phenomena. A conventional design of a PA studies the optimal charge, the current density and the matching network with a sine-wave signal, as done before. Consequently, only magnitude and phase distortions due to multiple harmonics are analyzed. That characterization does not bring enough information concerning linearity to be as accurate as required for broadband and high frequency standards. As presented in chapter 1, the 60GHz WPAN standard the OFDM modulation sceme. This modulation implies a large dynamic range and a high $PAPR$. The PA is forced to have a large IBO and to operate inefficiently in the linear region. To characterize that, IMP , $ACPR$ and EVM are investigated. The single-ended PA designed with distributed elements is used because it exhibits the best performances in terms of linearity.

This part presents high fidelity behavioral modeling flow of a 65nm CMOS PA dedicated for the 60GHz WPAN features. This work is composed into two parts:

- A first step is to characterize the PA by two-tone excitations.
- A second step simulates the same PA with an OFDM scheme using a QPSK modulation signal in the [57-64]GHz frequency band.

Figure C.1 illustrates our methodology of validation of high accuracy linearity study of a PA for WPAN standard. Signal 1, Signal 2 and Signal 3 represent the one-tone (analysed in chapter 1), the two-tone and the OFDM modulated signals respectively. The PA is biased at the same conditions as in the one-tone analysis. Co-simulations are performed in PTOLEMY environment. The PA is considered here as a model depicted by a black box.

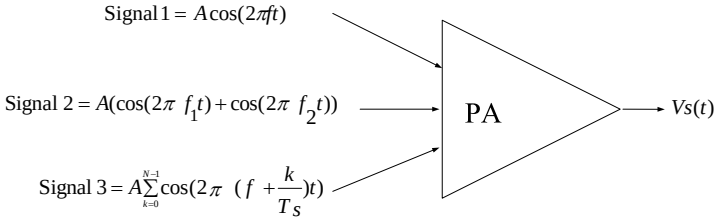


Figure C.1: Different input signals applied to the PA

C.1 Two-tone simulation

In the context of broadband applications, two parameters are observed to realize a two-tone non-linear simulation:

- The generation of multi-harmonics signals.
- The magnitude of the multi-harmonics signals with the input power sweep.

Figure C.2 shows the generation of the 3rd and 5th order harmonics in the useful band. Those harmonics, resulting from non linear behavior, can not be filtered. When the output power varies from 0dBm to 10dBm, 3rd harmonics evolve faster, from -50dBm to -20dBm. Up to 0dBm, 5th harmonics remain under $3rd$ harmonics with a difference of 30dB. Whereas at a higher output power, the difference between them is reduced to reach 10dB at 9dBm.

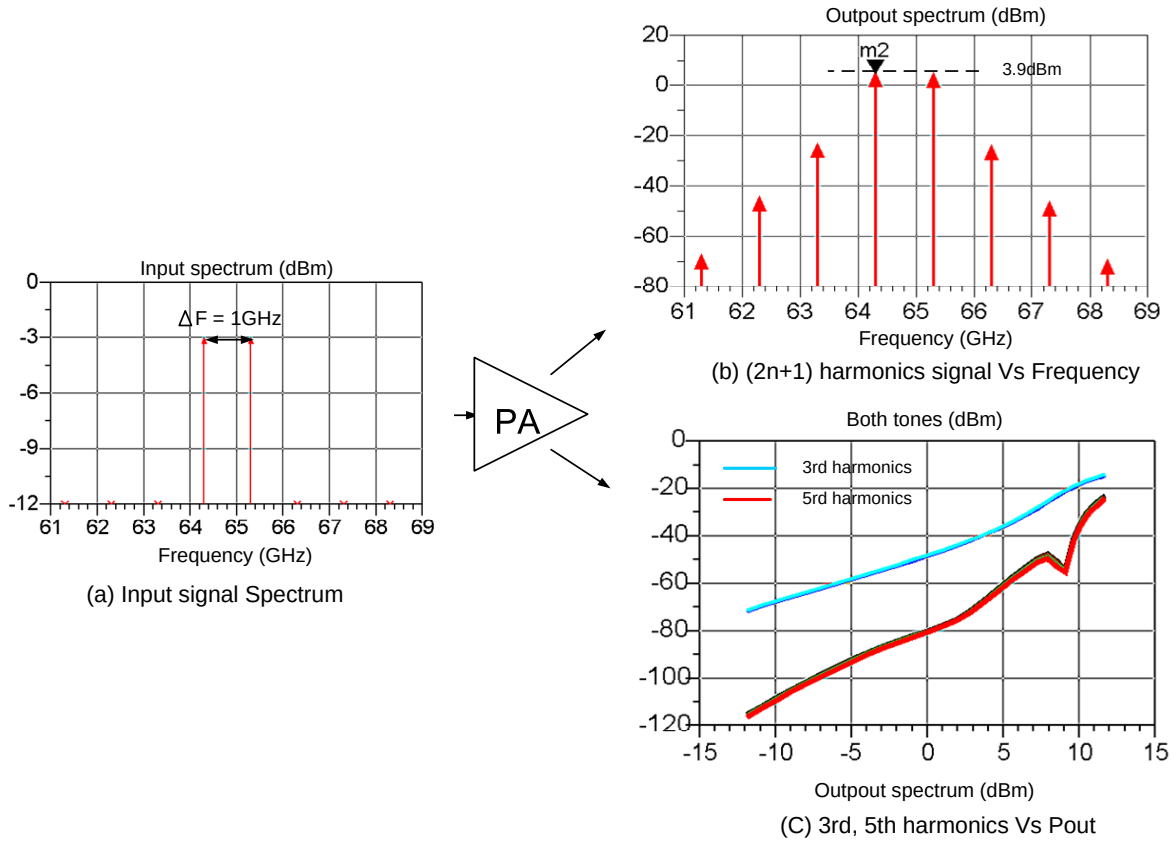


Figure C.2: Two-tone simulation

C.2 PA response to OFDM modulated signal

C.2.1 Transmitter building blocks

The ECMA specifies the multi-band scheme is adopted and plotted in fig chapter1. Reminding that the channels are spaced by 2.16GHz and display a symbol rate of 1.6Gbps. Figure C.3. The transmission chain is presented in Figure C.4. The signal waveform is depicted in frequency and time domains. An ideal NRZ format at 2Gbps is generated. A raised cosine filter is used in both I/Q plan to shape those pulses. The bandwidth of 1GHz is obtained by the roll-off factor constant (α) equal to 0.35. QPSK modulator encodes pair of bits by phase shifting of 0, $\pi/2$, π, $3\pi/4$ phase shifts for every combination of bits. The OFDM scheme is applied thanks to a buffer that transforms serial data to parallel data in 4 sub-channels. These sub-channels are mixed with a local oscillator. The total sum of the 4 sub-channels gives the OFDM modulated signal.

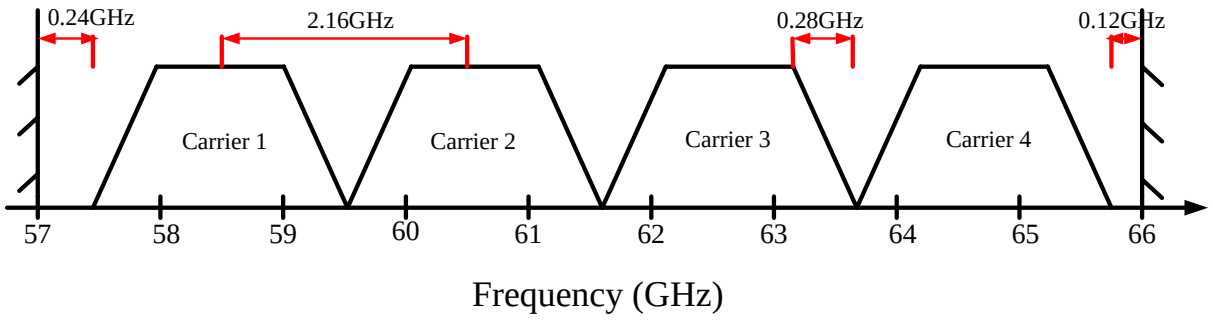


Figure C.3: WPAN spectrum overview

In the frequency domain, the signal presents the sum of four adjacent *sinc* waves. Whereas, In the time domain, the random OFDM signal consists in a temporal signal with high fluctuations of non constant envelope.

The generator delivering this OFDM modulated signal is not available. Hence, only simulation results are demonstrated here. The OFDM modulated signal is applied at the input of the PA. As seen in Figure C.4, the PA offers a quasi-constant gain of 7dB in the overall frequency band. Side lobes are generated by the PA that affect the linearity FoMs. $ACPR$ and EVM enable to characterize the PA's linearity in the 60GHz frequency band. They are discussed as follows:

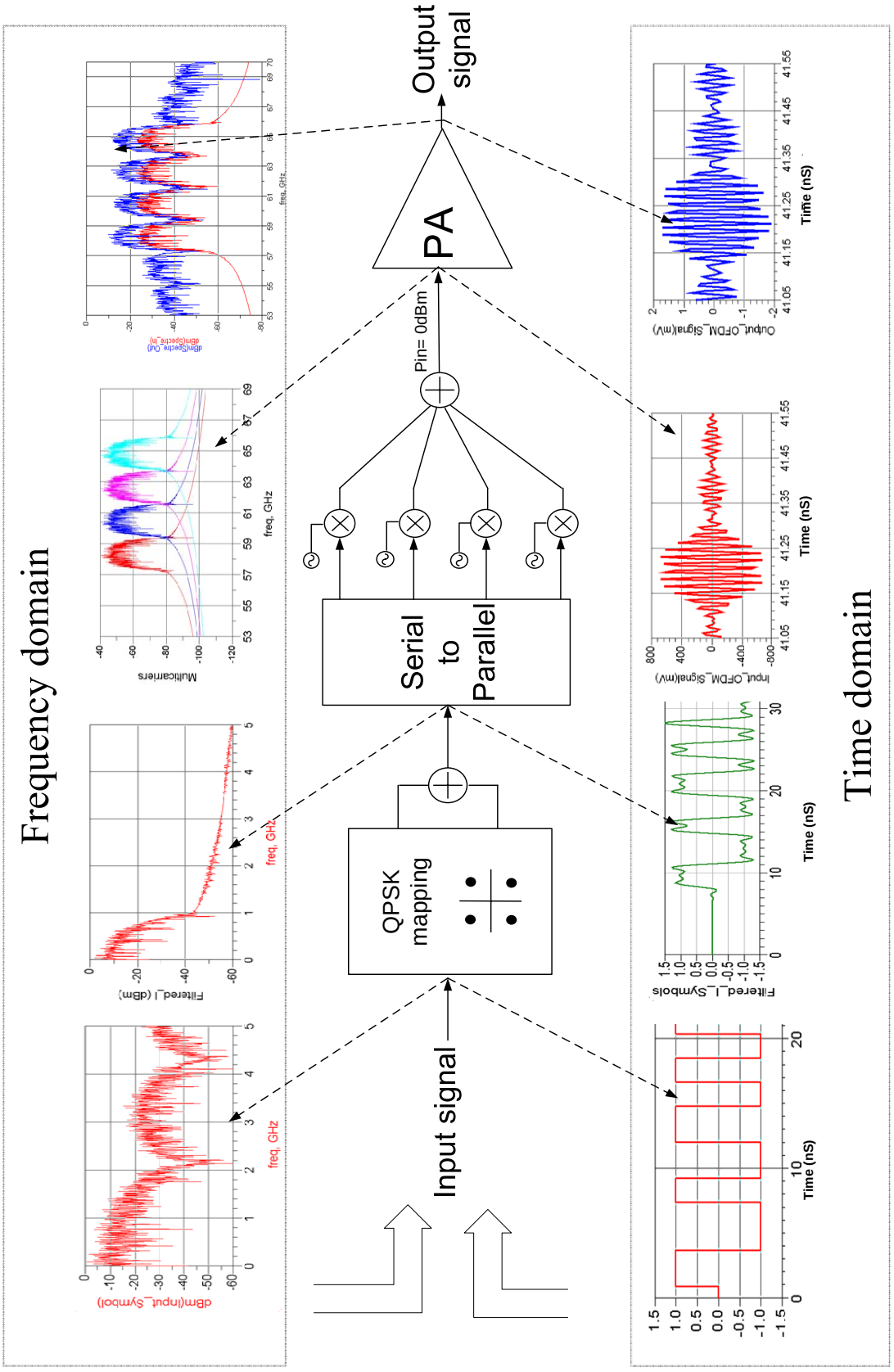


Figure C.4: Transmitter path1

C.2.2 ACPR

It shows the degradation of the transmitted signal. Indeed, distortions generate unwanted emissions in adjacent channel. $ACPR$ exhibits the difference between the power levels of the main and the adjacent channels. In Figure C.5, the $ACPR$ (right and left) does not achieve -35dBc at 1GHz offset for P_{out} up to 0dBm. When P_{out} grows, more distortions appear in adjacent channels. The PA non-linearity behavior induces a significant $ACPR$ of -15dBc at 1GHz offset for an output power of 8dBm.

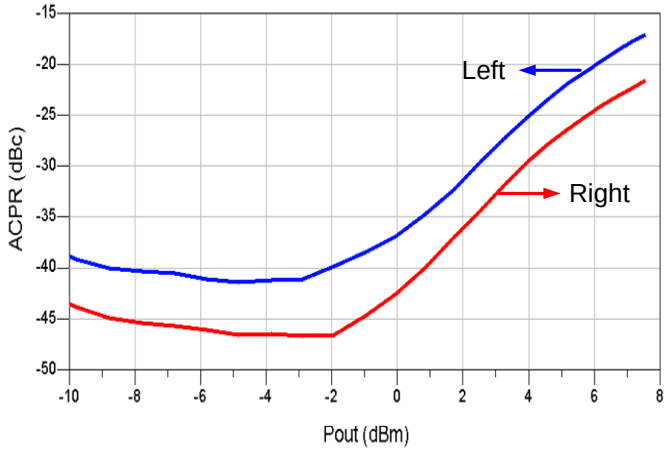


Figure C.5: $ACPR$ (left and right) vs. Pout

C.2.3 EVM

EVM depends strongly on the adopted digital modulation. It depends strongly on the magnitude of the input signal level. In the linear region, the EVM is only 6% to reach a maximum

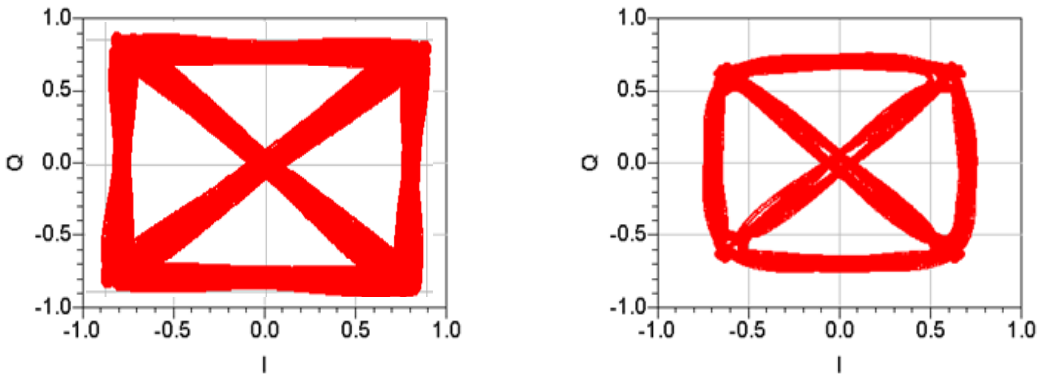


Figure C.6: QPSK Constellation in linear and saturated regime

of 20% at the compression. The constellation in Figure C.6 depicts the distorsion phenomenon at saturation.

C.3 Conclusion

In one-tone simulations, the PA reaches a good trade-off in term of linearity and PAE performances. The constraints are more drastic with a modulated signal in the case of WPAN standard, especially for linearity FoM. To characterize that, co-simulations are performed by exciting the PA, designed in CADENCE, with an OFDM signal generated in PTOLEMY environment. They show the influence on linearity when the OFDM modulated signal is applied. However, the PA demonstrates a reasonable $ACPR$ of 15dB and an EVM of 20% in compression region. This work aims to increase designer awareness face to linearity problems due to non constant envelope modulation.