A STATE OF THE ART ON ADC MODELING

P. Arpaia, P. Daponte, S. Rapuano

Dipartimento di Ingegneria, Facoltà di Ingegneria, Università del Sannio,
Palazzo Dell'Aquila Bosco Lucarelli, Piazza Roma, 82100, Benevento, Italy.
Ph. ++39 0824 305817, Fax ++39 0824 305840, E-mail {arpaia, daponte, rapuano}@unisannio.it.

Abstract *- The state of the art of the research on modelling of analog-to-digital converter-based measuring devices is surveyed. Main topics of modelling are reviewed according to the fields of prevailing scientific interest in metrological research such as quantization models, error models, and correction-aimed models. In these fields, recent developments are analysed with the aim of focusing both the contemporary situation and the imminent trends.*

1. INTRODUCTION

In the wider and wider development of analog-to-digital conversion systems, a pre-eminent role has been played by modelling techniques.

Modelling of analog-to-digital converter (ADC) components, as well as of digital measuring systems based on ADCs, allows the device behaviour to be predicted with a few of preventive experiments. For this reason, in last years a great deal of scientific interest has been directed to ADC modelling also for metrological aims. A model turns out to be useful for investigating the ADC metrological behaviour in several operating conditions during the main phases of development: *design*, *evaluation*, and *improvement*. In ADC *design*, the pre-eminent intrinsic error source is the quantization, and theoretical fundamental studies have been devoted to this topic by specialised research groups. In ADC *evaluation*, modelling is mainly used to analyse the impact of error sources on the metrological behaviour. In ADC *improvement*, the error occurrence is predicted in a range of operating conditions as wide as possible in order to compensate error source effects and correct deterministic errors. In all these fields, a lot of research activities with fruitful developments are in process.

In this paper, recent developments and current trends which are focus of prevailing scientific interest on ADC modelling are analysed by referring to: (i) *quantization models*, (ii) *error models*, and (iii) *correction-aimed models*.

2. QUANTIZATION MODELS

In last ten years, research on ADC modelling related to the quantization can be classified on the basis of the effects of quantization models on (i) the *ADC errors*, (ii) the *dithering*, and (iii) the *testing strategy*.

In the last decade, the effects of quantization models on *ADC errors* have been investigated with the main aim of assessing the conditions for the model validity [1]-[3]. Conversely, the current research trend is aimed at overcoming the limitations due to the assumption of uniform distribution of the quantization noise, and at investigating the quantization error for non ideal quantizers [4]-[6]. In particular, for a uniform [8], nonuniform [9], nonmonotonic and hysteretic quantizer [10], the probability density function (*pdf*) and the variance of the quantization error was derived.

The effects of quantization models on *dithering* have been investigated by referring to the well known idea of dithering which consists of "whitening" the autospectral density of the quantization noise by adding a suitable signal, and then reducing this noise by digital signal processing [11]-[14]. This means that a significant portion of the error power is located outside the signal band and can be eliminated by low-pass filtering. A sound theoretical background for the dithering theory was presented by Widrow et al. in their survey paper on quantization [3]. ADC linearity is usually increased through wide-amplitude dithering. A useful tool was provided by deriving relationships for the quantization error in the case of discrete binary, uniform, and Gaussian dither signals [15]. Then, a figure of merit (*"D"*) was introduced as the deviation of the ADC characteristic function from the unity gain line [16]- [17]. In last developments, for both additively and subtractively-dithered ADCs theoretical formulae were derived. [18]. Finally, the problem of designing dither-based quantizing system was addressed by giving quantitative criteria for choosing the parameters acting on resolution and accuracy [19], and for quasi-static signals corrupted with network induced interference or normally distributed white noise [12]-[14].

A *testing strategy* for ADCs necessarily implies a test signal model and a quantizer error model [20]. In particular, different model choices influence significantly the test results. A first case relates to the offset of the test signal. In [21], the well known results for null offset were generalised to the case of unknown offset by deriving the expected value and variance of the noise versus the offset and the number of levels. Besides to the offset, the amplitude of the test signal was also investigated [22]. Quantization error modelling is also very important in testing strategy. As an example, the zero-memory quantizer model looses completely significance in the case of high-speed flash ADCs [23]. The inadequacy of the reference quantizer theory behind the IEEE 1057 standard sine wave test in the case of actual nonlinear quantizers was pointed out in [6]. This situation was shown to be significantly improved by the above mentioned generalisation of the Widrow's quantization theorem to a generic quantizer (nonuniform and/or nonmonotonic).

3. ERROR MODELS

Research on ADC modelling includes predominantly a lot of works carried out in the framework of ADC design not strictly devoted to metrological aims and thus out of the scope of this paper. However, also in design, considerations on metrological performance are not fully neglected. Moreover, apart from their final aims, in some cases ADC models are strongly influenced by the conversion mechanism and, particularly, by the influence of peculiar error sources inside the architecture. Consequently, in the following, at first some general criteria and categories for the *classification of the ADC error models* are at first given. Then, on this basis, the ADC error modelling techniques recent focus of scientific interest are reviewed according to their dependence on the conversion mechanism as *architecture-independent*, and *architecture-dependent*.

3.1 Classification

ADC error modelling is generally approached at *analytical* or *heuristic* level. *Analytical* models include knowledge on the ADC error mechanism and conversion principle defined through mathematical relations and/or procedures. They are classified according to the abstraction level [24]-[25]: (i) *electrical models*, (ii) *macromodels*, and (iii) *behavioural models*. *Electrical models* details the ADC metrological behaviour at level of electronic components typical of the architecture. This allows the error effects to be finely tuned by the designer by analysing the influence of each electronic component of the architecture circuitry. Conversely, they are not easily utilisable in all those applications where all the details on the electrical behaviour are not needed owing to the high computing times. *Macromodels* analyse the ADC behaviour through electrical equivalent circuits simpler than the actual ones (such as e.g. Thevenin or Norton-based). Such an approach is limited by the practical difficulty of finding a suitable equivalent topology without loosing significant information on the real ADC metrological behaviour. *Behavioural models* do not take account the physical realisation of the ADC at all. The device is characterised by input-output analytical or numeral relations, without going in deep into the internal structure. Behavioural models are further classified according to their flexibility in [26-28]: (i) *table models*, (ii) *explicit models*, and (iii) *implicit models*. *Table models* memorises the input-output characteristic in a look-up table. This strategy turns out to be effective in the verification generally following the design, but is rigid because depends on the specific ADC under analysis: each aleatory variation of model parameters requires a new table generation, i.e. minimum flexibility. Moreover, the look-up table implementation requires significant times and memory space. *Explicit models* describe the ADC behaviour by an analytical relation in a closed form ease to be represented in a programming language. However, this consists also in their main limit because easy software packages are not always immediately available. Main advantage is the possibility of introducing in the analytical relation suitable parameters to describe different working conditions. This makes flexible the model structure, though the specific ADC architecture is not easy to be left out of consideration. *Implicit models* characterises the converter either in the time or frequency domain, by differential equations with suitable parameters to account for different architectures as well as device classes. They allows the maximum flexibility in the description of the ADC behaviour because they can be oriented to the design of a specific converter, a particular architecture. More in general, a whole class of devices can be described by parametrising the model as a whole and by assigning from time to time the parameter values according to the ADC under analysis. By creating a library of such a model, this allows a simulation environment to be created for verify and optimise the metrological performance of a Whatever ADC in all the design cycle. Finally, in several cases, electrical-behavioural mixed models are utilised. They describe some ADC sections in terms of electrical models while other as behavioural models. This allows the description detail of the error effects to be tailored directly in the more interesting specific sections.

Heuristic models include and describe knowledge on ADC error sources and conversion mechanism having empirical character (e.g. human skill), and/or particular nonlinear patterns (e.g. two-dimensional error frames). In particular, Artificial Neural Networks (ANNs) have found fruitful applications in ADC error modelling owing to their capability of successfully modelling complex nonlinear behaviours [29]. Behavioural modelling limitations due to either or the particular ADC architecture [30]-[31], or to the used parameter identification technique [32] were overcome by ANNs with ease of use, generalisation capabilities, and usefulness of obtainable results. The neural modelling approach is based on the use of an ANN which is capable, after a proper set-up phase, of providing an output digital code corresponding to the one that can be obtained from the actual ADC to be modelled. The approach proposed in [29], [33] is architecture-independent and uses the well known identification techniques based on ANNs [34].

Apart from the knowledge definition, the modelling approach can be "*a-priori*" or "*a-posteriori*" [25], [35]: the former exploits available information such as on the architecture and/or on the conversion principle, whereas the latter utilises only experimental output data.

The choice of the modelling approach depends on the use of the model: as an example, an electrical model can be fruitfully used in ADC design, whereas a behavioural model allows the ADC to be simulated as a component in the design of a more complex system such as a digital measurement system. In any case, a general criterion for selecting the modelling approach is based on the trade-off between the model accuracy and the corresponding simulation burden.

3.2 Architecture-Independent Error Models

A classification on architecture-independent error models can be carried out also according to the *static* or *dynamic* nature of the ADC input, and consequently to the ADC error nature. Static models characterise the converter for constant or slowly variable input signals, whereas dynamic models are used for higher frequency input signals.

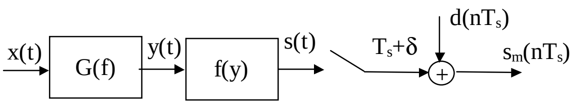

Fig.1 ADC behavioural error model including the major error mechanisms (*x(t)*: input signal, *G(f)* dynamic errors of the transfer function, *f(y)*: static nonlinear distortions, *d*: time jitter, *s(t)*: actual signal before sampling and quantization, T_s: sampling period, and $d(nT_s)$: additive noise (random+spurious) and quantization errors, $s_m(nT_s)$:actual digital output signal).

The most general and simple *static error model* was developed at behavioural level with the aim of describing the ADC nonlinearity [36]. This static memory-less approach [35] was followed also by other authors with the aim of describing the nonlinear transfer characteristic of the ADC. A more accurate model turns out to be also more architecture-oriented. An example though still general in its concept is the behavioural model proposed by Ruan for the three more diffused ADC architectures (successive approximation, dual slope and flash) [37]. Finally, the problem of the harmonic noise due to the nonlinearity of the transfer function of an actual ADC was faced by the analytical modelling of INL (integral nonlinearity) through simple power functions [38]. An investigation on the influence of architecture on the static modeling strategy is reported in [39].

Research on dynamic modeling is really reach and promising. It can be classified as:

(i) *jitter models:* research in the last decade was mainly aimed at investigating error effects and its bounds [40]-[42]. These results were derived in the most general case of lack of synchronisation between signal generator and data acquisition. However, they can not applied in all those practical cases of synchronised measurement systems (signal generation + data acquisition). In this case, Schoukens studied the influence of time jitter on the error by deriving explicit expressions for the related measurement errors [43]. Stenbakken in its jitter testing discussion used two different models: one based on a sawtooth wave and another based on a sine wave superimposed to a ramp, by discussing they adequacy for a digital scope [44].

(ii) *models of the actual acquisition channel:* in this field, in the last decade, research was mainly aimed at deriving a model of the actual data acquisition channel as a whole; in the years, the model was progressively complicated and made more robust from the theoretical and identification point of view. Further error sources, such as time base distortion, amplitude nonlinearity, were added, by mainly following a theoretical approach of parameter estimation and system identification (Fig.1) [43],[45]-[52]. A proposal of standardizing the modelling, identification, and optimisation was advanced [53].

(iii) *nonlinearity models*: a significant research effort was devoted to the model the ADC nonlinearity. Several and different approaches were

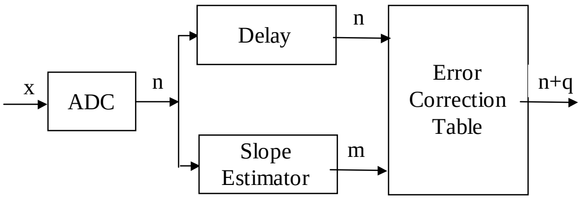

Fig.2 Block diagram of the phase-plane compensation architecture (*x*: ADC input, *n*: ADC uncorrected output code bin, *m*: estimated slope of the input signal, *q*: error correction).

devoted to the challenge of deriving mathematical relationships between distortion, input signal parameters and ADC nonlinearity errors [44]-[60].

(iv) *statistical models*: another approach was aimed at describing the device behaviour via a suitable statistical methodology [61]-[64]. As an example, the transfer characteristic of the ADC is described via a suitable conditional probability function, estimated through a modified version of the popular histogram test.

(v) *software models*: especially at electronic manufacturer level, a significant contribution on modelling research was devoted for describing as much accurately as possible the actual dynamic behavior of ADC devices. This was necessary to the designer for diagnostic and evaluation purposes in the design phase. Specific software simulation tools were developed both at behavioural and at electrical-circuit level [65]-[68] **.**

3.3 Architecture-dependent error models

Low-level modelling proposals reported in literature are necessarily architecture-dependent. Owing to their extreme working conditions, those devoted to such as *sigma- delta ADCs* will be remarked.

As above remarked in the general case of ADCs, also for *sigma-delta ADCs* a great effort has been spent by designer in order to improve dynamic performance through modelling [69]-[70]. However, modelling specifically aimed at analysing error effects with metrological scope only recently has become focus of scientific interest owing to the advent of new high-accuracy sigma-delta ADCs for instrumentation [71]. Model proposals specifically aimed at metrological aims. are referred to the analysis of the main error sources directly inside the sigma-delta ADC architecture, and (ii) for their effects on the overall metrological performance [72]-[77].

4. CORRECTION-AIMED MODELS

Error modelling has played a main role also in generating a correction of the ADC actual metrological

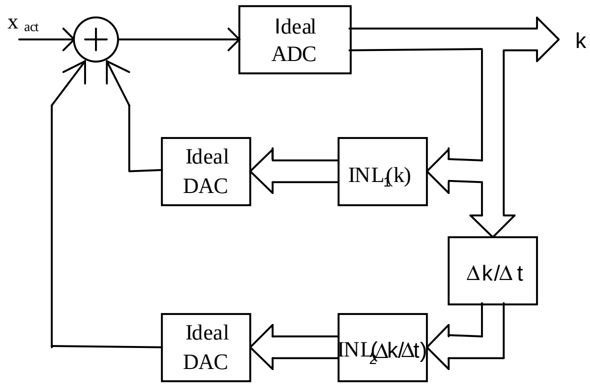

Fig.3 Block diagram of the a priori phase-plane error compensation architecture (x_{act}: actual input, INL_1 and INL_2: static and dynamic additive components).

behaviour. Various solutions were proposed either (i) independently of the architecture in order to maximise generality, or (ii) exploiting the architecture peculiarities, in order to maximise effectiveness.

Architecture-independent strategies were based initially on an on-line correction obtained by subtracting the modelled dynamic error to each output sample of the actual ADC [35]-[36],[78]-[79]. The addition of the time slope of the input signal as a second dimension allowed varies frequencies and amplitude for a larger class of input signals to be discriminated (Fig. 2) [36]. In this way, the ADC error is described as a function of the output code as well as the time slope of the input, i.e. in the "phase-plane". This permits the modelling of both the in-phase and in-quadrature phase distortions closer to actual ADCs, having memory behaviour or not real transfer function. Investigation on the possibility of adding a third dimension for modelling second-order derivative effects demonstrated that error is mainly dominated by first-order effects [80].The ADC correction based on phase-plane modelling showed to work adequately in several cases [81]-[85]. Apart from improvements strictly related to correction mechanism [86], phase plane modelling was improved mainly in model identification, and, namely, in: (i) the calibrating signals [87]-[89], and (ii) the experimental burden [83], [85], [87], [90]. However, such a modelling approach, completely a-posteriori in its concept, has main limitation just in its generality: the error model needs for its identification a burdensome experimental work. An alternative architecture-dependent idea has been based on an analytical a-priori approach to phase-plane modelling for most popular ADC architectures (integrating, successive-approximation, and flash ADCs), both for the static [39] and for the dynamic case (Fig. 3). Knowledge on the error source action inside the ADC architecture is exploited to mathematically derive a peculiar shape of the phase-plane surface [91]-[92].

5. CONCLUSIONS

The state of the art and the leading trends of the research in the field of ADC modeling have been discussed. The paper is aimed at providing young researchers interested in ADCs with a helping tool for orientating and more quickly become effective in this research field.

The capability of this field of attracting the scientific focus of interest is testified by the large amount of scientific contributions devoted by high-level research centres active in the field from several years.

References

[1] H.B. Kushner, M. Meisner, A.V. Levy, "Almost uniformity of quantization errors", IEEE Trans. on Instrumentation and Measurement, vol. 40, No. 4, pp. 682 –687, Aug. 1991.

[2] I. Kollar, "Bias of mean value and mean square value measurements based on quantized data", IEEE Trans. on Instrumentation and Measurement, vol. 43, No. 5 , pp. 733 –739, Oct. 1994.

[3] B. Widrow, I. Kollar, L. Ming-Chang, "Statistical theory of quantization", IEEE Trans. on Instrumentation and Measurement, vol.45, No. 2 , pp. 353 –361, Apr. 1996 .

[4] M. Bertocco, C. Narduzzi, P. Paglierani, D. Petri, "A noise model for quantized data", Proc. of IEEE IMTC/98, vol. 2, pp. 1243 –1247, May 1998.

[5] T.M. Souders, "Code probability distributions of A/D converters with random input noise", IEEE Trans. on Instrumentation and Measurement, vol. 47, No. 5 , pp. 1042 –1045, Oct. 1998.

[6] A. Pacut, K. Hejn, "Analog-to-digital converters: towards a generalization of Widrow's theorem", Proc. of IEEE IMTC/98, vol. 2, pp.1190–1197, May 1998.

[7] A. Pacut, K. Hejn, "Equivalence of Widrow's and Gray's approaches to uniform quantizers ", Computer Standards and Interfaces, vol. 19, No.3-4, pp. 205-212, 1998.

[8] M.F. Wagdy, W.M. Ng, "Validity of uniform quantization error model for sinusoidal signals without and with dither", IEEE Trans. on Instrumentation and Measurement, vol. 38, No. 3 , pp. 718 –722, June 1989.

[9] D. Bellan, A. Brandolini, A. Gandelli, "ADC uncertainties and sine-wave amplitude measurement", Proc. of Intern. Conf. on Electronics, Circuits and Systems, Sept. 1998.

[10] D. Bellan, A. Brandolini and A, Gandelli, "Quantization error for a sine wave: a comprehensive approach", Proc. of IMEKO TC-4 3rd Int. Workshop on ADC Modeling and Testing, pp. -128, vol. 1, pp. 399-404, Sept. 1998.

[11] D. Petri, "Dithered quantizing systems," Proc. of IMEKO TC-4 Int. Workshop on ADC Modelling, pp.119-128, May 1996.

[12] O. Aumala, J. Holub, "Dithering design for measurement of slowly varying signals", Measurement, vol. 23, No. 4, pp. 271-276, 1998.

[13] O. Aumala, "Turning interference and noise into improved resolution", Measurement, vol. 19, No.1, pp. 41-48, 1996.

[14] O. Aumala, "Dithering design of data acquisition of noise or interference corrupted measurement signals", Proc. of XIV IMEKO World Congress, vol. 4A, pp. 195-200, June1997.

[15] P. Carbone, C. Narduzzi, D. Petri, "Dither signal effects on the resolution of nonlinear quantizers", IEEE Trans. on Instrumentation and Measurement, vol. 43, No. 2, pp. 139 –145, Apr. 1994.

[16] M.F. Wagdy, M. Goff, "Linearizing average transfer characteristics of ideal ADC's via analog and digital dither", IEEE Trans. on Instrumentation and Measurement, vol. 43, No. 2, pp. 146 –150, Apr. 1994.

[17] M.F. Wagdy, "Effect of additive dither on the resolution of ADC's with single-bit or multibit errors", IEEE Trans. on Instrumentation and Measurement, vol. 45, No. 2 , pp. 610 –615, Apr. 1996.

[18] M.F. Wagdy, "Simulation results on A/D converter dithering", Proc. of IEEE IMTC/98, vol. 1, pp. 78 –83, May 1998.

[19] P. Carbone, "Quantitative criteria for the design of dither-based quantizing systems", IEEE Trans. on Instrumentation and Measurement, vol. 46, No. 3, pp. 656 –659, June 1997.

[20] G. Chiorboli, C. Morandi, "ADC modeling and testing", Proc. of IEEE IMTC 2001, vol. 3, pp. 1992-1999, May 2001.

[21] K. Hejn, A. Pacut, "Generalized model of the quantization error-a unified approach", IEEE Trans. on Instrumentation and Measurement, vol. 45, No. 1, pp. 41 –44, Feb. 1996.

[22] G. Chiorboli, G. Franco, C. Morandi, "Uncertainties in quantization-noise estimates for analog-to-digital converters", IEEE Trans. on Instrumentation and Measurement, vol. 46, No. 1 , pp. 56 –60, Feb. 1997.

[23] C. Morandi, L. Niccolai, "An improved code density test for the dynamic characterization of flash A/D converters", IEEE Trans. on Instrumentation and Measurement, vol. 43, No. 3 , pp. 384 –388, June 1994.

[24] A. Baccigalupi, M. D'Apuzzo, "ADC modeling techniques: A review", Measurement, vol.19, No.3-4, Nov.-Dec. 1996.

[25] P. Arpaia, F. Cennamo, P. Daponte, M. D'Apuzzo, "A behavioural model for scan converter-based transient digitizers", Measurement, vol. 17, No. 2, pp.103-114, Feb. 1996.

[26] E. Bilhan, P.C. Estrada-Gutierrez, A.Y Valero-Lopez, F. Maloberti, "Behavioral model of pipeline ADC by using Simulink", Proc. of Southwest Symp. on Mixed-Signal Design 2001, pp. 147-151, Feb. 2001.

[27] G. Ruan , "A behavioral model of A/D converters using a mixed-mode simulator", IEEE Journal on Solid-State Circuits, vol. 26, Mar. 1991.

[28] F. Maloberti, P. Estrada, A. Valero, P. Malcovati, "Behavioral modeling and simulation of data converters", Proc. of IMEKO 2000, vol. 10, pp. 229-236, Sept. 2000.

[29] A. Bernieri, P. Daponte, D. Grimaldi, "ADC neural modeling", IEEE Trans. on Instrum. and Meas., vol. 45, No. 2, pp. 627 -633, Apr. 1996 ,.

[30] E.G. Soenen, P.M. VanPeteghem, H.C. Liu, S. Narayan, J.T. Cummings, "A framework for design and testing of analog integrated circuits", IEEE Trans. on Instrumentation and Measurement, vol. 39, No. 6, pp. 890 –893, Dec. 1990.

[31] S. Brigati, V. Liberali, F. Maloberti, "Precision behavioural modelling of circuit components for data converters", Proc. of 2nd Int. IEE Conf. on Advanced A/D and D/A Conversion Techniques and their Applications, pp.110-115, July 1994.

[32] A. Baccigalupi, P. Daponte, M. D'Apuzzo, "An improved error model of data acquisition systems", IEEE Trans. on Instrumentation and Measurement, vol. 43, No. 2, pp. 220-225, Apr. 1994.

[33] A. Baccigalupi, A. Bernieri, C. Liguori, "Error compensation of A/D converters using neural networks", IEEE Trans. on Instrumentation and Measurement, vol. 45, No. 2, pp. 640-644, Apr. 1996.

[34] A. Bernieri, M. D'Apuzzo, L. Sansone, M. Savastano, "A neural network approach for identification and fault diagnosis on dynamic systems", IEEE Trans. on Instrumentation and Measurement, vol. 43, No. 6, pp. 867 –873, Dec. 1994.

[35] M. Van den Bossche, J. Schoukens, J. Renneboog, "Dynamic testing and diagnostics of A/D converters", IEEE Trans. on Circ. and Sys., vol.CAS-33, No.8, pp.775-785, Aug. 1986.

[36] F.H. Irons, "Dynamic characterization and compensation of analog to digital converters", IEEE Int. Symp. o n Circ. and Sys., pp.1273-1277, May 1986.

[37] G. Ruan, "Behavioral model of A/D converters using a mixed-mode simulator", Proc. of IEEE Custom Integrated Circuits Conference, pp. 5.7/1 -5.7/4, May 1990.

[38] K. Kim, "Analog-to-digital conversion and harmonic noises due to the integral nonlinearity", IEEE Trans. on Instrumentation and Measurement, vol. 43, No. 2, pp. 151-156, Apr. 1994.

[39] P. Arpaia, P. Daponte, L. Michaeli, "Influence of the architecture on ADC error modeling", IEEE Trans. on Instrumentation and Measurement, vol. 48, No. 5, pp. 956-966, Oct. 1999.

[40] Y.C. Jenq, P. Crosby, "Sinewave parameter estimation algorithm with application to waveform digitizer effective bits measurement", IEEE Trans. on Instrumentation and Measurement, vol. 37, No. 4, pp. 529-532, Dec. 1988.

[41] H. Wei-Da, Y.C. Jenq, "Waveform estimation with jitter noise using stochastic up anddown method", IEEE Trans. on Instrumentation and Measurement, vol. 43, No. 2, pp. 200-203, Apr. 1994.

[42] S.S. Awad, M.F. Wagdy, "More on jitter effects on sinewave measurement", IEEE Trans. on Instrumentation and Measurement, vol. 40, No. 3, pp. 549 –55, June 1991.

[43] R. Pintelon, J. Schoukens, "An improved sine-wave fitting procedure for characterizing data acquisition channels", IEEE Trans. on Instrumentation and Measurement , vol. 45, No. 2, pp. 588 –593, Apr. 1996.

[44] G. Stenbakken, J. Deyst, "Comparison of time base nonlinearity measurement techniques", IEEE Trans. on Instrumentation and Measurement, vol. 47, No.1 pp. 34-39, Feb. 1998.

[45] R. Pintelon, J. Schoukens, "Measurement of frequency response functions using periodic excitations, corrupted by correlated input/output errors", IEEE Trans. on Instrumentation and Measurement, vol. 50, No. 6, pp.1753-1760, Dec. 2001.

[46] G. Vandersteen, Y. Rolain, J. Schoukens, "An identification technique for data acquisition characterization in the presence of nonlinear distortions and time base distortions", IEEE Trans. on Instrumentation and Measurement, vol. 50, No. 5, pp.1355-1363, Oct. 2001.

[47] R. Pintelon, J. Schoukens, "Measurement of frequency response functions in the presence of correlated input/output errors", Proc. of IEEE IMTC 2001, vol. 1, pp. 2-7, May 2001.

[48] G. Vandersteen, Y. Rolain, J. Schoukens, "System identification for data acquisition characterization", Proc. of IEEE IMTC/98, vol. 2, pp. 1211-1216, May 1998.

[49] J. Schoukens, R. Pintelon, G. Vandersteen, "A sinewave fitting procedure for characterizing data acquisition channels in the presence of time base distortion and time jitter", IEEE Trans. on Instrumentation and Measurement, vol. 46, No. 4, pp.1005-1010, Aug. 1997.

[50] J. Schoukens, "A critical note on histogram testing of data acquisition channels", IEEE Trans. on Instrumentation and Measurement, vol. 44, No. 4, pp. 860-863, Aug. 1995.

[51] I. Kollar, R. Pintelon, Y. Rolain, J. Schoukens, "Another step towards an ideal data acquisition channel", IEEE Trans. on Instrumentation and Measurement, vol. 40, No. 3, pp. 659-660, June 1991.

[52] D. Mirri, G. Iuculano, F. Filicori, G. Pasini, G. Vannini, "Modeling of non ideal dynamic characteristics in S/H-ADC devices", Proc. of IEEE IMTC/95, p. 27, Apr. 1995.

[53] M. Savino, "The problem of the standard characterization of ADC and digitising waveform recorder", Proc. of V IMEKO TC-4 Workshop on ADC Modeling and Testing, pp.301-305, Sept. 2000.

[54] M.F. Wagdy, "Diagnosing ADC nonlinearity at the bit level", IEEE Trans. on Instrumentation and Measurement, vol. 38, No. 6, pp. 1139-114, Dec. 1989.

[55] K. Hejn, I. Kale, "Some theorems on Walsh transforms of quantizer differential and integral nonlinearity", IEEE Trans. on Instrumentation and Measurement, vol. 41, No. 2, pp. 218-225, Apr. 1992.

[56] D. Bellan, A. Brandolini, A. Gandelli, "Effects of ADC nonlinearities in sine-wave amplitude measurement", IEEE International Conference on Electronics, Circuits and Systems, vol. 3, pp. 449-452, May 1998.

[57] D. Bellan, A. Brandolini, A. Gandelli, "ADC nonlinearities and harmonic distortion in FFT test", IEEE IMTC/98, vol. 2, pp.1233-1238, May 1998.

[58] D. Dallet, F. Valeze, P. Kadionik, M. Benkais, P. Marchegay, "Dynamic testing of A/D converters: how many samples for a given precision?", IEEE IMTC/96, vol. 2, pp. 1298-1303, June 1996.

[59] P. Arpaia, A. Manuel da Cruz Serra, C.L. Monteiro, "A critical note to IEEE 1057-94 standard on hysteretic ADCdynamic testing", IEEE Trans. on Instrumentation and Measurement, vol. 50, No. 4, pp. 941-948, Aug. 2001.

[60] C.L. Monteiro, P. Arpaia, A.C. Serra, "Phase-spectrum analysis for detection of ADC hysteretic distortion", Proc. of IEEE IMTC 2001, vol. 3, pp. 1677-1683, May 2001.

[61] N. Giaquinto, M. Savino, A. Trotta, "Testing and optimizing ADC performance: a probabilistic approach", IEEE Trans. on Instrumentation and Measurement, vol. 45, No. 2, pp. 621-626, Apr. 1996.

[62] A.P. Bykov, V.I. Didenko, A.L. Movchan, J.S. Solodov, "Minimization of parameters number describing accuracy of data acquisition system", Proc. of IEEE Int. Workshop on Intelligent Data Acquisition and Advanced Computing Systems: Technology and Applications, pp.148-151, July 2001.

[63] N. Kolev, S. Yordanova, P. Tzvetkov, "Computerised investigation of robust measurement systems", IEEE Int. Workshop on Intelligent Data Acquisition and Advanced Computing Systems Technology and Applications, pp.211-214, July 2001.

[64] R. Kochan, O. Berezky, A. Karachka, I. Maruschak, O. Bojko, "Development of the integrating analog to digital converter for distributive data acquisition systems with improved noise immunity", IEEE Int. Workshop on Intelligent Data Acquisition and Advanced Computing Systems Technology and Applications, pp. 193-196, July 2001.

[65] V. Liberali, V.F. Dias, M. Ciapponi, F. Maloberti, "TOSCA: a simulator for switched-capacitor noise-shaping A/D converters", IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 12, No. 9, pp. 1376-1386, Sept. 1993.

[66] B. Carroll, C. Wegener, M.P. Kennedy, "LEMMA-ADC: the linear error mechanism modelling algorithm applied to A/D-converters", Proc. of 3rd IEEE Int. Conference on Advanced A/D and D/A Conversion Techniques and Their Applications (Conf. Publ. No. 466), pp. 145 –148, July 1999.

[67] Z. Weibiao, X. Huimin, R. Al-Omari, M. Hassoun, "Symbolic synthesis of analog-to-digital conversion architectures using direct-mapping techniques", Proc. of IEEE International Conference on Electronics, Circuits and Systems, vol. 3, pp.215-218, Sept. 1998.

[68] D. Dallet, P. Daponte, E. Mancini, S. Rapuano, "Modelling and characterization of pipelined ADCs", in press on Proc. of IEEE IMTC 2002, May 2002.

[69] S.R. Norsworthy, R. Schreier, G.C. Temes, "Delta-sigma data converters - Theory, design and simulation", IEEE Press., New York, 1997.

[70] http://rf.rfglobalnet.com/software_modeling/software/2/551.htm.

[71] Cirrus Logic, Crystal, http://www.cirrus.com/design/products/overview/detail.cfm?d=266.

[72] K. Hejn, P. Murphy, I. Kale, "Measurement and enhancement of multistage sigma-delta modulators," Proc. of IEEE IMTC/92, pp. 715-719, May 1992.

[73] P. Arpaia, F. Cennamo, P. Daponte, H. Schumny, "Modeling and characterization of sigma-delta analog-to-digital converters", Proc. of IEEE IMTC/98, pp. 96-100, May 1998. In press on IEEE Trans. on Instrumentation and Measurement.

[74] G. Fischer, A.J. Davis, "Wideband cascade delta-sigma modulator with digital correction for finite amplifier gain effects", Electronics Letters, vol. 34, No. 6, pp. 511-512, Mar. 1998.

[75] M. Kozak, M. Karaman, I. Kale, "Efficient architectures for time-interleaved oversampling delta-sigma converters", IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing, vol. 47, No. 8, pp. 802 –810, Aug. 2000.

[76] M. Kozak, I. Kale, "Novel topologies for time -interleaved delta-sigma modulators", IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing, vol. 47, No. 7, pp.639-654, July 2000.

[77] G. Fischer, A.J. Davis, "Alternative topologies for sigma-delta modulators-a comparative study", IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing, vol. 44, No.10, pp. 789-797, Oct. 1997.

[78] F.H. Irons, A.L. Chaiken, "Analog-to-Digital Converter compensation precision effects", Proc. of 29th Midwest Symposium on Circuits and Systems, pp. 849-852, 1987.

[79] T.A. Rebold, F.H. Irons, "A phase-plane approach to the compensation of high-speed analog-to-digital converters", Proc. of IEEE Int. Symposium on Circuits and Systems, pp. 455-458, May 1987.

[80] J.P. Deyst, J.J. Vytal, P.R. Blasche, W.M. Siebert, "Wideband distortion compensation for bipolar flash analog-to-digital converters", Proc. of IMTC/92, pp.290-294, May 1992.

[81] J.P Deyst, T.M. Souders, "Phase plane compensation of the NIST sampling comparator system", Proc. of IMTC/94, vol. 2, pp. 914-916, May 1994.

[82] J. Tsimbinos, K.V. Lever, "Applications of higher-order statistics to modelling, identification and cancellation of nonlinear distortion in high-speed samplers and analog-to-digital converters using the Volterra and wiener methods", Proc. of IEEE Signal Processing Workshop on Higher-Order Statistics, pp. 379-383, June 1993.

[83] J. Tsimbinos, K.V. Lever, "Improved state-space and phase-plane error table compensation of analog-to-digital converters using pseudo-random calibration signals", Proc. of 2nd IEE Int. Conf. on Advanced AD and DA Conversion Techniques and their Applications, pp-130-135, July 1994.

[84] J. Tsimbinos, K.V. Lever, "Improved error table compensation of analog-to-digital converters using pseudo-random calibration signals", Electronic Letters, vol. 30, No. 6, pp-461-462, Mar. 1994.

[85] A. Baccigalupi, A. Bernieri, C. Liguori, "Error compensation of A/D converters using neural networks", IEEE Trans. on Instrumentation and Measurement, vol. 45, No. 2, pp. 640-644, Apr. 1996.

[86] D.M. Hummels, J.J. McDonald II, F.H. Irons, "Distortion compensation for time-interleaved analog to digital converters", Proc. of IMTC/96, pp.728-731, June 1996.

[87] D.M. Hummels, S.P. Kennedy, "Improved dynamic compensation of ADCs using an iterative estimate of the ADC calibration signal", Proc. of 35th Midwest Symposium on Circuits and Systems, pp. 68-71, Aug. 1992.

[88] F.H. Irons, D.M. Hummels, S.P. Kennedy, "A novel architecture for dynamic error correction of Analog-to-Digital Converters", Proc. of 26th Annual Princeton Conf. on Inform. Science and Sys., Mar. 1992.

[89] D.M. Hummels, F.H. Irons, I.N. Papantonopoulos, "Characterization of Analog-to-Digital Converters using a non-iterative procedure", Proc. of IEEE Int. Symp. On Circ. and Sys., pp. 5-8, May-June 1994.

[90] S. Acunto, P. Arpaia, F.H. Irons, D.M. Hummels, "A new bidimensional histogram for the dynamic characterization of ADCs", Proc. of IEEE IMTC 2001, vol.3, pp. 2015-2020, May 2001.

[91] P. Arpaia, P. Daponte, L. Michaeli, "Analytical a priori approach to phase-plane modeling of SAR A/D converters", IEEE Trans. on Instrumentation and Measurement, vol. 47, No.4, pp. 849-857, Aug. 1998.

[92] R. Holcer, L. Michaeli, "DNL ADC testing by the exponential shaped voltage", Proc. of IEEE IMTC 2001, vol. 1, pp. 693 -697, Mayn 2001.