Almost Perfectly Symmetric SWCNT-Based CMOS Devices and Scaling

Zhiyong Zhang,[†,*] Sheng Wang,[†] Zhenxing Wang,[†] Li Ding,[†] Tian Pei,[†] Zhudong Hu,[†] Xuelei Liang,[†] Qing Chen,[†] Yan Li,[‡] and Lian-Mao Peng[†,*]

[†]Key Laboratory for the Physics and Chemistry of Nanodevices and Department of Electronics, Peking University, Beijing 100871, China, and [‡]Key Laboratory for the Physics and Chemistry of Nanodevices and College of Chemistry and Molecular Engineering, Peking University, Beijing 100871, China

ABSTRACT Symmetric n- and p-type field-effect transistors (FETs) have been fabricated on the same undoped single-walled carbon nanotube (SWCNT). The polarity of the FET is defined by controlled injection of electrons (n-type, *via* Sc electrodes) or holes (p-type, *via* Pd electrodes) into the SWCNT, instead of *via* chemically doping the SWCNT. The SWCNT-based FETs with different channel lengths show a clear trend of performance improvement for channel length scaling. Taking full advantage of the perfect symmetric band structure of the semiconductor SWCNT, a perfect SWCNT-based CMOS inverter is demonstrated, which gives a voltage gain of over 160, and for the two adjacent n- and p-type FETs fabricated on the same SWCNT, high field mobility is realized simultaneously for electrons (3000 $cm^2/V \cdot s$) and holes (3300 $cm^2/V \cdot s$).

KEYWORDS: carbon nanotube · CMOS · inverter · mobility · scaling

Complementary metal−oxide−semiconductor (CMOS) is a major class of integrated circuits and shares over 75% market of the semiconductor industry due to its tremendous advantages of high noise immunity and low static power consumption. CMOS is also sometimes referred to as complementary symmetry metal−oxide−semiconductor (or COS-MOS) to emphasize the fact that typical digital circuitry design style uses complementary and symmetrical pairs of p-type (hole) and n-type (electron) MOS field-effect transistors (FETs) for logic functions.[1] Unfortunately, perfect symmetric CMOS has never been realized. This is because for all important semiconductors the band structures are intrinsically not symmetric around their band gaps or between the conduction and valence bands. Typically, electrons have a smaller effective mass than that of holes, and the performance of n-FETs is much better than that of p-FETs. As a result of this intrinsic asymmetric band structures of Si and all major semiconductor (including III−V and II−VI compounds) holes move much slower in MOS FET devices than electrons,[2,3] dragging the overall performance of the CMOS circuits. In this work, we will show, by using single-walled carbon nanotube (SWCNT) as the conduction channel material, that almost perfect symmetric CMOS devices and circuits can be realized. This is because the band structure of a semiconductor SWCNT is almost perfectly symmetric between its conduction and valence bands. A careful evaluation of a SWCNT-based CMOS inverter reveals that electron and hole mobilities of over 3000 $cm^2/V \cdot s$ are realized simultaneous on the adjacent SWCNT-based n- and p-type FETs fabricated on the same SWCNT, leading to an almost perfect CMOS inverter with perfect logic high and low states, a voltage gain of over 160, and extremely low power dissipation.

The recent announcement by Intel company on the completion of its development of a 32 nm process[4] raises once again the concern that silicon-based CMOS is quickly approaching its end, and further improvements in transistor speed and performance will have to come from new materials rather than from scaling silicon further.[5] Several possibilities have been considered for beyond Si technology, in particular those based on III−V compounds and nanowires, graphene, and carbon nanotubes (CNTs).[5] Indeed, extensive investigations have been carried out during the past decade on semiconducting CNTs for their potential use as the conduction channel material to replace Si.[6−8] Among other advantages, CNTs have a unique one-dimensional (1D) structure which leads to much reduced scattering and very high carrier mobility and sometimes even ballistic transport on devices of the length scale of less than 200 nm. A semiconductor CNT also has an almost perfect

*Address correspondence to zyzhang@pku.edu.cn, lmpeng@pku.edu.cn.

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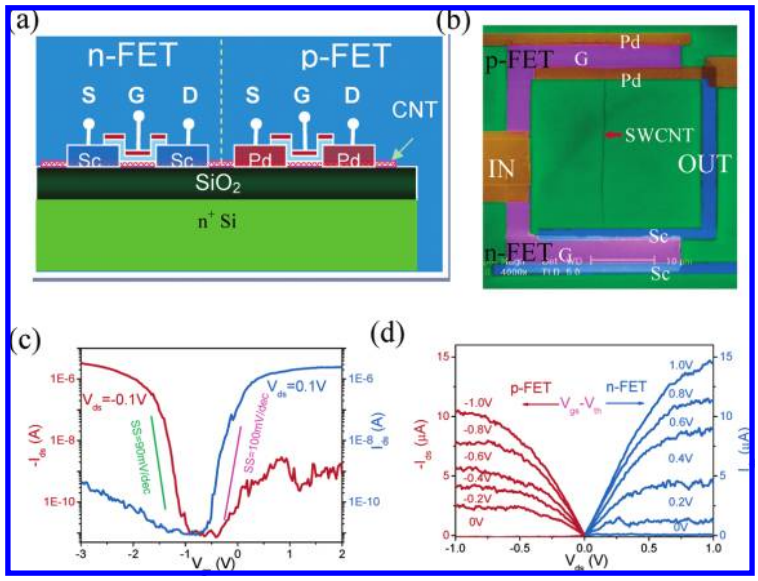

Figure 1. SWCNT-based CMOS FETs with self-aligned top gate. (a) Side view schematic of SWCNT CMOS devices with a pair of p- and n-FETs. (b) SEM image showing a SWCNT CMOS inverter which is composed of a p-FET (top) and a n-FET (bottom). The gate length for both FETs is 4 μm. (c) Field transfer characteristics ($I_{ds}-V_{gs}$) and (d) output characteristics ($I_{ds}-V_{ds}$) of a pair of SWCNT CMOS FETs with gate length L_g = 1.0 μm.

symmetric band structure between its conduction and valence bands[9] and consequently essentially the same effective mass for electrons and holes. This band structure symmetry may in principle lead to the same electron and hole mobilities and similar performance for n- and p-type FETs which are necessary for perfect CMOS performance. Unfortunately, perfect symmetric CNT-based CMOS devices and integrated circuits (ICs) have not been realized, and this is largely due to the laggard developments on n-type devices. It has long been realized that the as-grown CNTs usually exhibit p-type field characteristics, and the performance of the p-type CNT FET was pushed almost to its limit in 2004 immediately after the discovery that Pd forms almost perfect ohmic contact with the CNT and can be used as the source (S)/drain (D) electrodes for high-performance p-type CNT FETs.[10,11] Although a number of SWCNT-based CMOS devices and ICs have been fabricated,[12−16] the full advantage of the symmetric band structure of the CNT was not demonstrated adequately due to the cumbrance from n-type FETs. In an earlier paper, we demonstrated that Sc may be used to form almost perfect ohmic contact to the conduction band of the CNT,[17] and the performance of n-type CNT FETs was pushed almost to their performance limit by combining the Sc-contacted CNT FETs with a novel self-aligned metal gate with high-k gate dielectric.[18,19] The time is now ripe for developing perfect symmetric CNT-based CMOS technology.

Unlike conventional Si-based CMOS, where the polarity of the FETs is defined by doping the conduction channel of the device with suitable dopant atoms, in CNT-based CMOS,[17,20] the polarity of the FETs can be defined by controlling the injection of carriers to the channel. While Pd may be used to inject holes barrier-free into the valence band of the CNT to form high-performance p-type FETs,[10,11] Sc may be used to inject electrons barrier-free into the conduction band of the CNT to form almost perfect n-type FETs.[17−20] This is a doping-free process. Both high-performance p- and n-type FETs can then be fabricated on the same intrinsic SWCNT, which may in principle lead to perfectly symmetric CMOS devices and circuits. Although symmetric n-type and p-type CNT FETs were fabricated with back-gate structure in our earlier works,[17,20] these back-gate devices cannot deliver near perfect performance due to the intrinsic limitation of the back-gate geometry. In this paper, we are concerned with the high-efficient self-aligned top-gate geometry[19] that affords the almost perfect performance of the CNT FETs as demonstrated by the many examples given in this paper.

RESULTS AND DISCUSSION

Figure 1a depicts a side view of the CNT-based CMOS device structure, and Figure 1b shows a top view scanning electron microscopy (SEM) image of a real CNT-based CMOS inverter, which we will discuss later. Current−voltage characteristics for a pair of typical p- and n-FETs fabricated on the same SWCNT with a diameter of 2 nm and a gate length of 1.0 μm are shown in Figure 1c,d. All electrical measurements were carried out in air using a probe station without intentionally protecting or packaging the devices. Figure 1c shows clearly that the Sc-contacted CNT FET is n-type (blue curve) and the Pd-contacted CNT FET is p-type (red curve), and the field transfer characteristics are in many important aspects symmetric with each other. For example, the maximum ON/OFF current ratio I_{on}/I_{off} is larger than 10^5 at V_{ds} = 0.1 V, and the subthreshold swing [SS = $dV_{gs}/d(\log I_{ds})$] is about 90 mV/decade for the Pd-contacted p-type CNT FET, and the corresponding values for the Sc-contacted n-type CNT FET are 10^5 and 100 mV/decade, respectively. The linear $I_{ds}-V_{ds}$ characteristics shown in Figure 1d indicate that ohmic contacts are formed for both p-type and n-type FETs at room temperature, and earlier studies showed that this behavior persists down to about 4.2 K.[10,17] The two sets of $I_{ds}-V_{ds}$ curves for the p-type FET (red curve) and n-type FET (blue curve) are again similar for the whole range of values $|V_{gs} - V_{th}|$ (V_{th} being the threshold voltage of the FET) from 0 to 1.0 V. To quantitatively assess the performance of both the n- and p-type CNT FETs, here we consider some key device parameters for a fixed supply voltage V_{dd} = 1.0 V. The first device param-

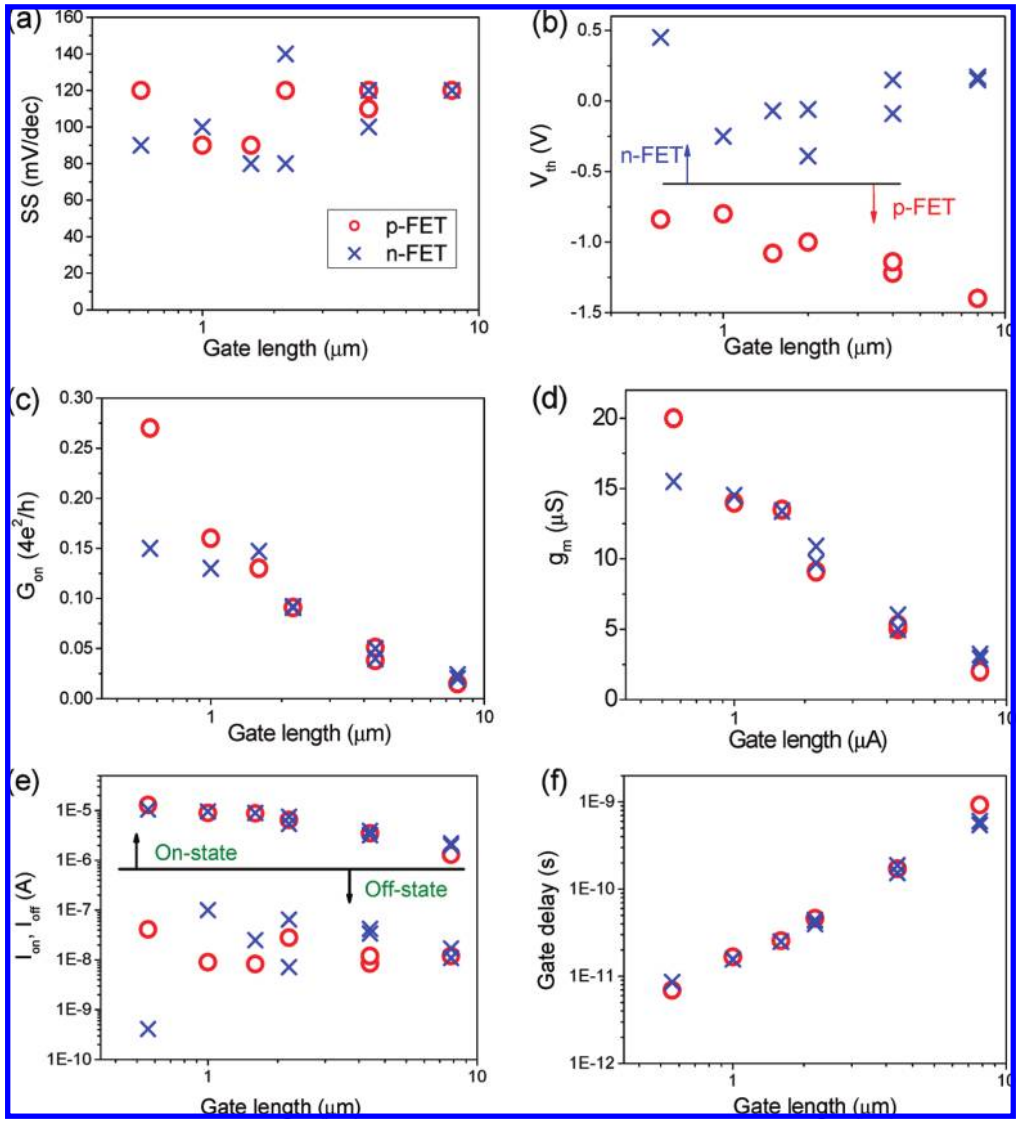

Figure 2. Comparison of seven device parameters between seven n-type and eight p-type CNT FETs, which are fabricated on the same SWCNT with a diameter of 2 nm. All of the parameters are plotted *vs* gate length from 0.6 to 8 μm. (a) Subthreshold swing SS. (b) Threshold voltage V_{th}. (c) ON-state conductance G_{on}. (d) Peak transconductance g_m. (e) I_{on} and I_{off} and (f) intrinsic gate delay. In all of these figures, red circles represent p-FETs and blue forks represent n-FETs. All of the parameters are calculated assuming the device operating under the bias of V_{dd} = 1.0 V.

eter is the ON-state channel conductance (normalized by $4e^2/h$), G_{on}, which is defined as $G = dI_{ds}/dV_{ds}$ at low bias (V_{ds} = 0.1 V) and $|V_{gs} - V_{th}| = 1$ V. The second device parameter is the peak transconductance, g_m, which is defined as $g_m = dI_{ds}/dV_{gs}$ and may be obtained from the $I_{ds}-V_{gs}$ curves under the bias of $|V_{ds}| = 1$ V. Other parameters include the ON- and OFF-state currents, I_{on} and I_{off}, which are determined by anchoring the V_{gs} window around V_{th} on the $I_{ds}-V_{gs}$ curves at $|V_{ds}| = 1$ V with V_{gs} swing at 0.67 V above V_{th} for determining I_{on} and 0.33 V below V_{th} for determining I_{off}.[21] Using the field transfer characteristics shown in Figure 1c, we obtain the ON-state conductance G_{on} 0.13 × $4e^2/h$ for the n-type FET and 0.16 × $4e^2/h$ for the p-type FET, and from Figure 1d, we obtain the corresponding g_m =14.5 μS for the n-FET and 17.0 μS for the p-FET. It is noted that this is the first time that the g_m value exceeds 10 μS simultaneously for both the n-FET and p-FET fabricated on the same SWCNT.[13−16]

For IC applications, it is highly desirable to fabricate all of the devices with uniform performance. Fifteen transistors are fabricated on the same SWCNT with a diameter of 2 nm, as shown in Figure 1b, but the devices were fabricated with different gate lengths ranging from 8 to 0.6 μm to explore the scaling behavior of CNT FETs. Among the 15 FETs, seven are p-type and eight are n-type. All 15 transistors have similar subthreshold swing SS ranging from 80 to 140 mV/decade, as shown in Figure 2a. The threshold voltages for all 15 FETs are shown in Figure 2b. These threshold voltages divide clearly into two groups; those between −0.8 and −1.4 V are associated with p-type CNT FETs, and those between −0.4 and 0.45 V are associated with

n-FETs. The separation of the threshold voltages V_{th} between n- and p-type FETs is important to ensure that the p-FET and n-FET do not open simultaneously so that no direct path exists between the supply and ground rails under steady-state operating conditions and hence to lower power dissipation. Four additional device parameters (G_{on}, g_m, I_{on}, and I_{off}) are calculated from experimental current−voltage characteristics to assess the electrical performance of these FETs, and these parameters are plotted *versus* gate length in Figure 2c−e. These figures show clearly that the n-type and p-type FETs of the same gate length exhibit very similar behavior, resulting in very similar values for all four important device parameters. Toward shorter gate length and in particular for I_{off}, the device parameter shows noticeable fluctuations. These fluctuations might result from contaminations or defects in the SWCNT channel, at the SWCNT/metal electrode interface,[22] or from the inhomogeneous HfO_2 gate dielectric. In principle, we can minimize or sometimes even eliminate some systematic performance fluctuations among devices through optimizing the process in the further. The leakage current I_{off} is a key parameter which reflects the standby power consumption of the device. For all devices examined here (Figure 2e), I_{off} is smaller than 1×10^{-7} A and typical at the level of tens of nA when the device operates at $V_{DD} = 1$ V.

Three important device parameters, G_{on}, g_m, and I_{on}, show clear trend on the gate length scaling, suggesting that we can improve the performance of the SWCNT-based CMOS devices and integrated circuits by shrinking the gate length similar to the scaling as used in semiconductor industry in the past four decades; that is, the SWCNT-based CMOS devices are scalable. Figure 2c shows that G_{on} will exceed $0.1 \times 4e^2/h$, and Figure 2d shows that g_m will become larger than 10 μS for both the p- and n-type devices when gate length becomes smaller than 2 μm. When normalized by d (d is the diameter of the SWCNT and represents the channel width), the values of g_m become more than 5000 μS/μm for both n- and p-FETs with a gate length shorter than 2.0 μm, and these values should be compared to the most recent values of about 2000 μS/μm for p-FETs and 2200 μS/μm for n-FET announced by Intel for its 32 nm process.[4]

It is well-known that electron has smaller effective mass than a hole in silicon due to its asymmetric band structures.[23] Consequently, the electron mobility is about two times larger than that of the hole in silicon, and the performance of n-FETs is much better than that of the p-FETs with the same gate length and width. Although the dc characteristics of the p-FET can be improved to match the n-FET through enlarging the channel width 2−3 times that of the n-type FET, the switching speed of the p-FET cannot be made as good as that of the n-FET. As a result, the speed of Si CMOS circuit is dragged by the p-FET. This problem does not exist in CNT-based CMOS technology. This is because, in CNT, the conduction band and valence band are symmetric about the band gap of the CNT.[9] In CNT-based CMOS technology, n- and p-type devices are intrinsically symmetric, leading to symmetric performance not only on dc characteristics but also on switching speed. Here we use the intrinsic gate delay as the performance metric to describe the intrinsic switching speed of the transistors. The gate delay is defined as CV_{ds}/I_{on}, in which C is the total gate capacitance.[21] All CNT-based FETs discussed in this paper are fabricated on the same SWCNT with a diameter of $d = 2.0$ nm, which is covered on top by a gate dielectric HfO_2 thin film with a thickness $t = 15$ nm and $\varepsilon_r = 15$. The gate capacitance for this top gate device geometry is estimated to be $C = 1.5$ pF/cm. The gate delay values *versus* gate length for all 15 n-type and p-type CNT FETs are depicted in Figure 2f. This figure shows beautifully that the n-FET and p-FET with the same gate length have almost identical gate delay, and this delay exhibits again a clear decreasing trend as the gate length decreases. It is thus demonstrated that an almost perfect match has been realized for CNT-based CMOS devices not only for their dc performance *via* symmetry in, for example, G_{ON}, which can also be realized in Si-based CMOS by varying the width of the device, but also in dynamical operation *via* gate delay, and this is not an easy thing to do in the Si-based CMOS process.

A CMOS inverter is the simplest and perfect CMOS circuit for illustrating the advantages of CMOS circuits. Figure 1b shows a top view SEM image of a CNT-based CMOS inverter. This inverter is composed of a pair of adjacent n- and p-type FETs fabricated on the same SWCNT with $d = 2$ nm and the same gate length of $L_g = 4.0$ μm. The field transfer (Figure 3a) and output characteristics (Figure 3b) are almost perfectly symmetric between the n- and p-type FETs. The field-dependent mobility for both electrons (n-type) and holes (p-type) can be calculated from the transfer characteristics (Figure 3a) using the relation[25]

$$\mu = \frac{L}{CV_{ds}} \frac{dI_{ds}}{dV_{gs}}$$

The mobility curves (Figure 3c) show a peak mobility of about 3000 $cm^2/(V \cdot s)$ for electrons and about 3300 $cm^2/V \cdot s$ for holes for the two adjacent n- and p-type FETs on the same SWCNT. Although the peak mobility for either electron or hole, as shown in Figure 3c, is not the highest mobility reported for SWCNT with similar diameter,[19,24,25] this is the first time that high performance is achieved in CMOS circuit simultaneously for both the n-type and p-type FETs. The near-perfect symmetry on the mobility between electron and hole manifests experimentally the intrinsic symmetric band structure of the CNT.

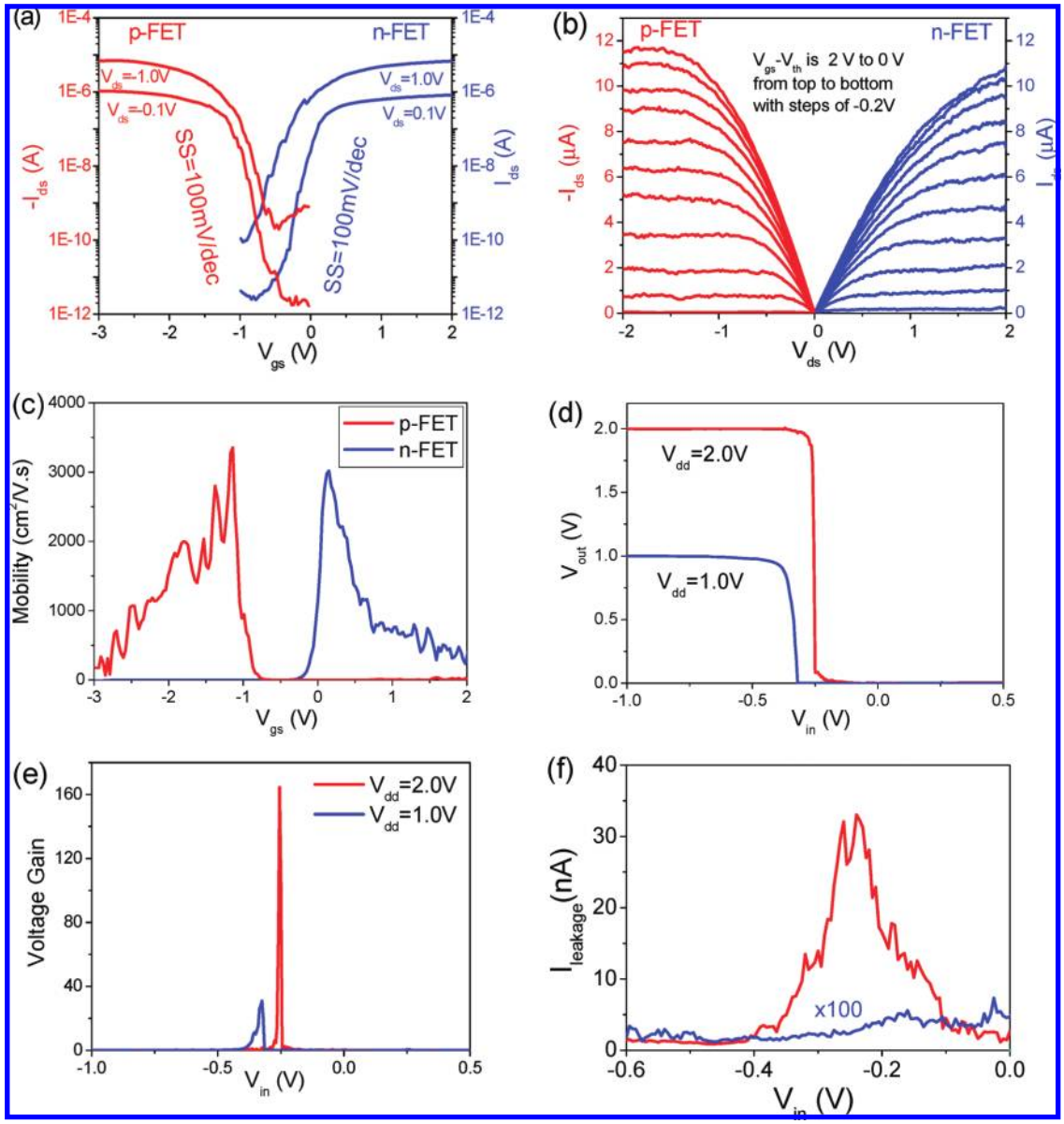

Figure 3. Characteristics of the CNT-based CMOS inverter as shown in Figure 1b. The gate length for both the n- and p-FETs of the CMOS inverter is L_g = 4.0 μm. (a) Field transfer characteristic ($I_{ds}-V_{gs}$), (b) output characteristic ($I_{ds}-V_{ds}$), and (c) field-dependent carrier mobility for both the n- and p-type FET devices at low bias of V_{ds} = 0.1 V. (d) Voltage transfer characteristics ($V_{out}-V_{in}$), (e) field-dependent voltage gain, and (f) operating current curves ($I_{leakage}-V_{in}$) of the inverter under bias of V_{dd} = 2.0 and 1.0 V.

The voltage transfer characteristics of the CNT-based CMOS inverter were measured and shown in Figure 3d for two bias voltages V_{dd} = 2.0 and 1.0 V. Profiting from the symmetric performance between the n-type and p-type FETs, the voltage transfer characteristics exhibit a perfect output "high" or "1" state with $V_{out} = V_{dd}$ for small input with $V_{in} < -0.5$ V, and a perfect "low" or "0" state output with V_{out} down to the ground level of 0 V for both V_{dd} = 1.0 and 2.0 V. For small input or V_{gs} for both the p- and n-type FETs, the p-FET is open and n-FET is closed, resulting in a very small current (~nA, for V_{dd} = 2.0 V; see Figure 3f) and voltage drop V_{ds} ~ mV on the p-FET and therefore an almost perfect output with $V_{out} = V_{dd}-V_{ds} \sim V_{dd}$. For large input V_{in}, the p-type FET is closed and n-type FET is open, leading to a very small output voltage $V_{out} = V_{GND} + V_{ds}$ ~ mV, that is, an almost perfect "0" output. In previously published CNT-based inverters,[13−16,26,27] the high level was much smaller than V_{dd} due to the limited performance of the n-type FETs used, which leads to large standby current and undesired power dissipation. Output transition from "high" state to "low" state starts to occur when the p-FET begins to enter its off-state, that is, when $V_{gs} \approx V_{in} - V_{dd} \leq V_{th}$ or $V_{in} \leq V_{dd} + V_{th}$ for the p-type FET. Therefore, the larger the applied voltage V_{dd} is, the higher the inverter threshold voltage (at which the output transition occurs) is, and this is clearly demonstrated in Figure 3d, which shows that

the inverter threshold voltage shifts toward smaller value when V_{dd} decreases from 2.0 to 1.0 V.

The highly symmetric n- and p-FETs result in an extremely sharp transition in the dc voltage transfer characteristic, as shown in Figure 3d, leading to the highest-to-date voltage gain of 160 under the supplied voltage of $V_{dd} = 2.0$ V and therefore high noise immunity. The voltage gain decreases rapidly with decreasing supplied voltage but remains more than 30 for $V_{dd} = 1.0$ V, and this is large enough for logical circuit design.

The power dissipated by the IC chip is a very important concern, and in particular the FET off-current leakage is perhaps the greatest problem facing the continued scaling of Si-based CMOS technology. In dc (or standby) operation, the dc power dissipation of the CMOS inverter may be estimated as

$$P_{dc} = V_{dd}(I_{low} + I_{hight})/2 \quad (1)$$

where I_{low} is the standby current I at V_{in} = low and I_{high} at V_{in} = high. I_{low} is typically 0.01−2 nA, which rises to about I_{high} = 0.03−5 nA at V_{in} = high (Figure 3f). The dc operation thus results in $P_{dc} \sim 0.03$ nW for $V_{dd} = 1$ V and 7 nW for $V_{dd} = 2$ V. For a large supplied voltage (*e.g.*, $V_{dd} = 2$ V), the invert current increases significantly from the standby value of about 2−5 nA to more than 30 nA at the transition region between −0.4 and 0.1 V. However, when V_{dd} is lowered to 1.0 V, the peak in the inverter current disappears, and for the full range of input voltage, the current is on the order of tens of pA, which is submerged by the noise signal, as shown in Figure 3f. Huge benefit is thus expected to be gained when we lower the supplied voltage from 2.0 to 1.0 V. While this decrease in V_{dd} results in about five times reduction in the voltage gain from 160 to about 30, the dc power dissipation of the inverter reduces more than 2 orders of magnitude from about 7 to 0.03 nW. The dynamic operation of the CNT-based CMOS inverter is even more advantageous in supplied voltage scaling. This is because at lower V_{dd} both n- and p-type FETs are never fully open at the same time, and the short circuit or leakage current (Figure 3f) of the inverter does not show any significant peak or increase in the transition region.

CNT-based CMOS devices are not only more symmetric, operating faster and consuming less power than Si-based CMOS devices, but their fabrication is also simpler. We compare the main process steps between CNT-based and standard twin-well Si CMOS technology[28] before an interconnection process in Table 1, showing clearly that the CNT-based CMOS technology is much simpler than that of the Si-based CMOS. This is largely due to the doping-free and isolating-free process we developed for the CNT-based CMOS process. This process also requires fewer steps in other main processes than that of the Si-based CMOS, including fewer lithography, etching, and film growth steps.

TABLE 1. Comparison of Main Process Steps between SWCNT-Based and Standard Twin-Well Si CMOS Technology with Shallow Trench Isolation[28] before Interconnection[a]

	lithography	etching	ion implantation	film growth	total
Si-CMOS	10	6	8	8	32
SWCNT CMOS (this work)	5	5	0	7	17

[a]The process for fabricating assistant electrodes to select semiconducting SWCNTs is considered in SWCNT CMOS. The etching process includes wet etching, dry ecting, CMP, and lift-off, and the flim growth process includes thermal growth and deposition growth.

CONCLUSION

In conclusion, high-performance n-type (Sc-contacted) and p-type (Pd-contacted) FETs with self-aligned gates are fabricated on the same SWCNT. This SWCNT-based CMOS technology is much simpler than Si-based CMOS technology due to its doping-free and isolating-free process. Detailed examination of 15 FETs shows that n-type and p-type FETs are almost perfectly symmetric both on dc performance and dynamical operation *via* gate delay, and this symmetry results from the intrinsic symmetry in the band structures of the CNT. Both n- and p-type CNT FETs are scalable; that is, their performances can be boosted up as the gate length scaling down. The voltage transfer characteristics of the CNT-based CMOS inverter show a perfect "1" (with $V_{out} = V_{dd}$) and "0" state (with $V_{in} = V_{GND}$) and the highest-to-date voltage gain of over 160. High field carrier mobility is simultaneously realized in the two adjacent n-type FET (3000 $cm^2/V \cdot s$) and in p-type FET (3300 $cm^2/V \cdot s$), which are fabricated on the same SWCNT in a CMOS inverter.

EXPERIMENTAL SECTION

Ultralong SWCNTs about a few hundred micrometers were directionally grown on a heavily n-doped silicon wafer *via* a catalytic chemical vapor deposition, and the wafer was covered with a layer of thermally grown SiO_2 (500 nm).[29] The silicon substrate is used as the back gate with the SiO_2 being the gate dielectric, and semiconducting SWCNTs were identified *via* field-effect measurement using the back gate and then used for following CMOS device and circuit fabrications. p-Type CNT FETs with self-aligned gate structure were fabricated at first. Windows for source and drain electrodes were first patterned *via* electron beam lithography. Pd film of 80 nm was then deposited by e-beam evaporation followed by lift-off. The gate window was then patterned *via* electron beam lithography, and a 15 nm HfO_2 film with dielectric constant of about 15 was grown by ALD at 90° followed by 10 nm Pd film deposition by e-beam evaporation. The standard lift-off process was then used to form the self-aligned HfO_2/Pd gate stack to finish the fabrication of p-FETs.[19] n-FETs were fabricated with a process similar to that for p-FETs, but Sc was used instead of Pd as the S, D, and gate electrodes.

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