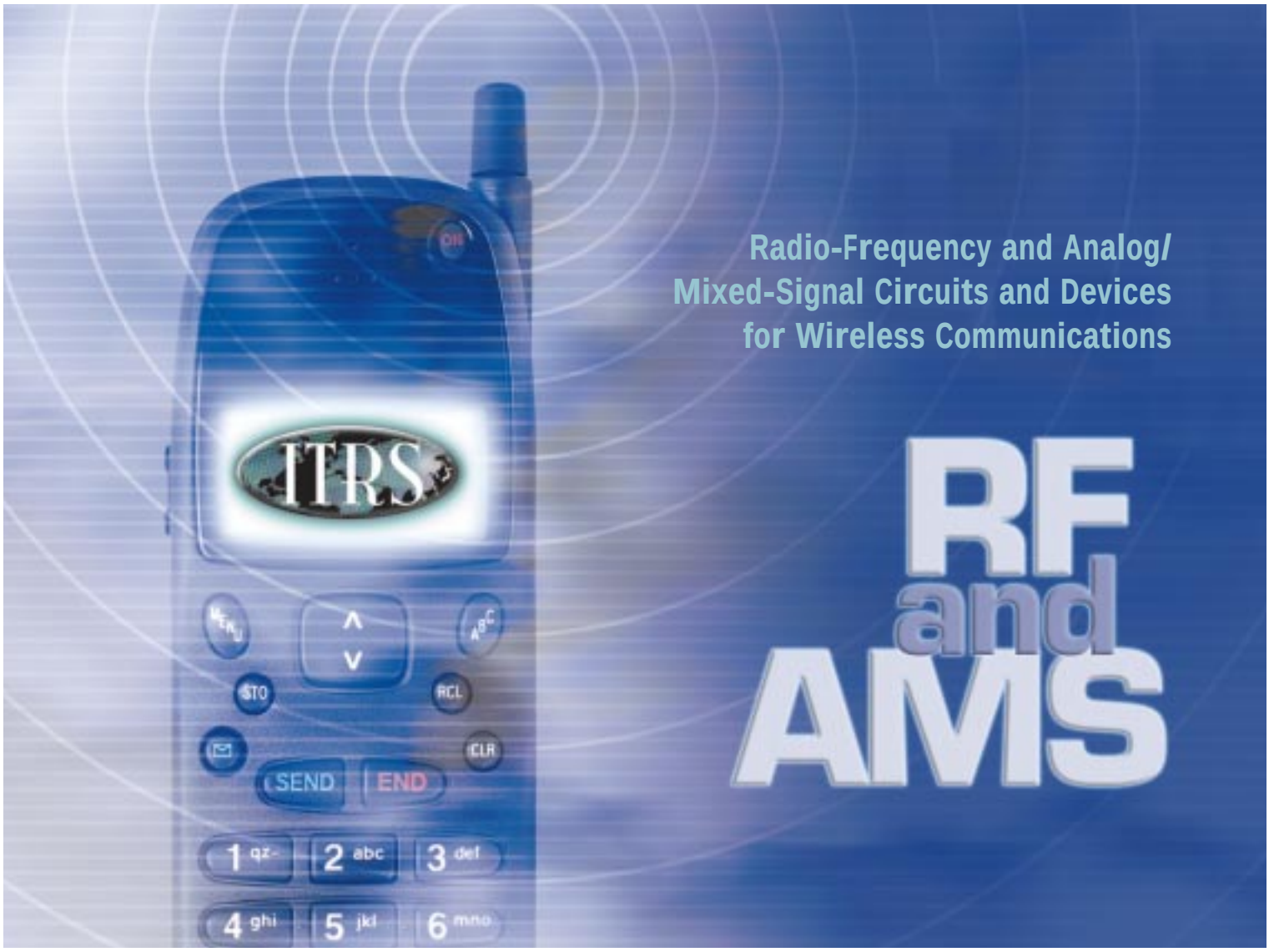

Radio-Frequency and Analog/ Mixed-Signal Circuits and Devices for Wireless Communications

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Wireless communications have evolved from traditional radio and TV broadcasting to a broad spectrum of exciting applications in bidirectional and interactive communications such as cellular system/phones, smart handheld devices, wireless local area networks (WLANs), Bluetooth technology, global positioning systems (GPSs), broadband satellite communication solutions, phased array radio frequency (RF) systems, and other emerging wireless communication applications. RF and analog/mixed-signal (AMS) integrated circuits (ICs) are the critical and enabling elements for the success of these wireless communications. The demands to bring new and advanced features in various wireless communication products and systems continue to drive the revenue growth for semiconductors used in wireless communication systems.

Today, semiconductor revenue for wireless communications represents a significant portion of the total worldwide semiconductor market. Just for cellular handsets, the semiconductor market is estimated at more than US$20 billion in 2003, and about 38% of this revenue (more than US$7.5 billion) comes from RF and AMS ICs for cellular handsets [1]. The cellular handset semiconductor market itself represents almost 13% of the total worldwide semiconductor market. In addition to cellular handsets, other wireless communication products and systems, such as those used in cellular infrastructure, WLANs, and satellite communications, will continue to drive the growth of semiconductor revenue for wireless communications.

A key factor for continued semiconductor market growth in wireless communication applications is the advance of RF and AMS ICs and the related very large scale integrated circuit (VLSI) technologies. In contrast to digital VLSI technology, RF and AMS technologies depend on many very different materials systems, some of which are compatible with complementary metal oxide semiconductor (CMOS) processing and others which are not compatible with CMOS processing (e.g., compound semiconductor electronics)—at least on a single die.

The 2003 International Technology Roadmap for Semiconductors (ITRS) [2] recognizes wireless applications enabled by

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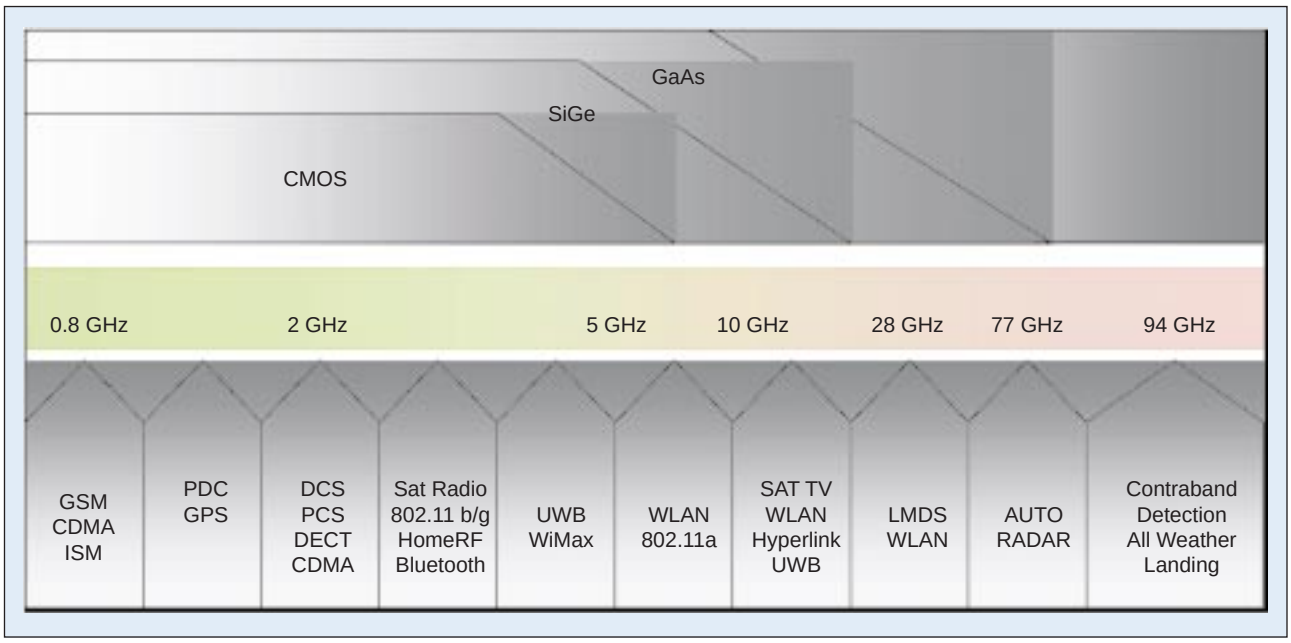
RF and AMS devices and circuits as a separate new system/technology driver. Moore's First Law predicts a doubling of transistor density about every 18–24 months [3] and is a major metric for assessing mainstream CMOS logic technology. In contrast to all other ITRS drivers [dynamic random-access memory (DRAM), multiprocessing unit (MPU), and application-specific integrated circuit (ASIC)], the correlation between feature size and circuit performance is weaker for analog and RF circuitry. Instead, analog and RF technologies have to meet many other technology features and device

Acronyms

AA	anti aliasing
A–D	analog-to-digital
ADC	analog to digital converter
AGC	automatic gain control
AMS	analog/mixed signal
ASIC	application-specific integrated circuit
BAW	bulk acoustic wave
BiCMOS	bipolar-complementary metal oxide semiconductor
BVCBO	breakdown voltage between collector and base, emitter open
BVCEO	breakdown voltage between collector and emitter, base open
CDMA	code division multiple access
CMOS	complementary metal oxide semiconductor
CPU	computer processing unit
CV	current-voltage
D–A	digital-to-analog
DAC	digital to analog converter
dc	direct current
DCS	digital cellular system
DECT	digital European cordless telephone
DRAM	dynamic random-access memory
DSP	digital signal processor
E/D	enhancement/depletion
EDA	electronic design automation
f	frequency
FBAR	film bulk acoustic resonator
FD-SOI	fully depleted silicon on insulator
FET	field effect transistor
FOM	figure of merit
F_{ref}	reference frequency
F_t	transit frequency
F_{max}	maximum frequency of oscillation
GaAs	gallium arsenide
GaN	gallium nitride
GPS	global position system
GSM	global system for mobile communications
HBT	hetero bipolar transistor
HEMT	high electron mobility transistor
HFET	heterojunction field effect transistor
HV	high voltage
I	current
IP	intellectual property
IC	integrated circuit
InP	indium phosphide
I/O	input/output
ISM	industrial, scientific, medical frequency band (unlincensed)
ITRS	International Technology Roadmap for Semiconductors
LAN	local area network
LDMOS	laterally diffused metal oxide semiconductor
LF	low frequency
LMDS	local multipoint distribution services
LNA	low-noise amplifier
MEMS	microelectromechanical systems
MESFET	metal semiconductor transistor
MHEMT	metamorphic high electron mobility transistor
MMIC	monolithic microwave integrated circuit
MOS	metal oxide semiconductor
MPU	multiprocessing unit
NF	noise figure
NMOS	n-type channel MOS
PA	power amplifier
PAE	power added efficiency
PCS	personal communication service
PDC	personal digital cellular
PD-SOI	partially depleted silicon on insulator
PHEMT	pseudomorphic high electron mobility transistor
PM	power management
Q	quality factor
RF	radio frequency
RFIC	radio frequency integrated circuit
SAT	satellite terminal
SAW	surface acoustic wave
SiC	silicon carbide
SiGe	silicon germanium
SIP	system-in-package
SOC	system-on-chip
SOI	silicon on insulator
SS	small signal
T/R	transmit/receive
UWB	ultra wideband
VCO	voltage controlled oscillator
VLSI	very large scale integrated circuit
V	voltage
Vdd	drain supply voltage
$V_{dd,\ analog\ speed}$	maximum supply voltage for analog speed device
Vth	threshold voltage
W	Watt
WCDMA	wideband code division multiple access
WLAN	wireless local area network
3D	three dimensional
2G	second generation wireless network (digital)
3G	third generation wireless network (multimedia)



1. Application spectrum. (Adapted from Figure 1 in the D. Barlas et al. article in Microwave Journal*, page 22, June 1999. Printed with permission.)*

parameters that do not scale in the same manner as logic device metrics [e.g., current-voltage/current (CV/I)] do [4].

The most important drivers for wireless communications systems are cost, available frequency bands, power consumption, functionality, size of mobile units, very high volumes of product, appropriate performance requirements, and standards and protocols. Standards and protocols significantly influence parameters such as operating frequency, channel bandwidth, and transmit power. Such standards and protocols impact overall system performance and include regulations from various governments that determine frequency availability. They often affect advances in RF and AMS technologies much more than they affect advances in many of the mainstream CMOS technologies described in the 2003 ITRS.

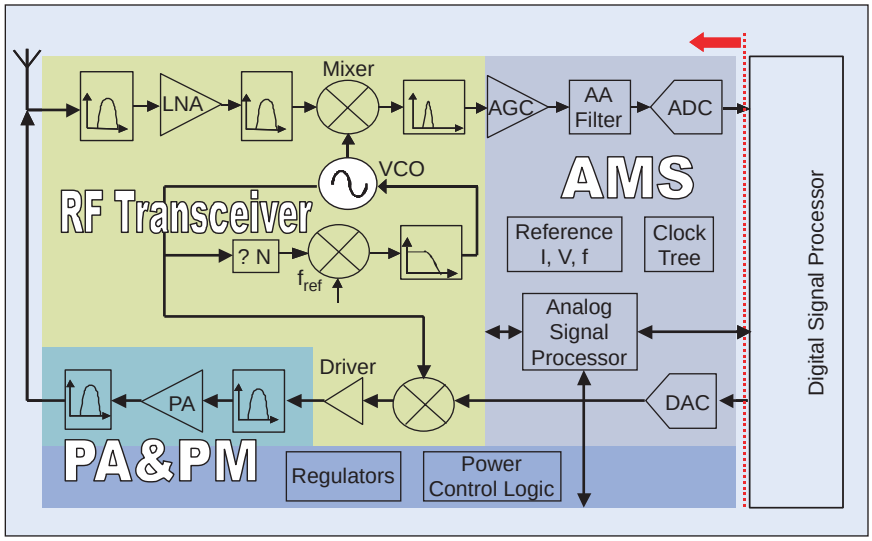
Figure 1 schematically presents the scope of this article in terms of the interplay among commercial wireless communication applications, available spectrum, and the kinds of elemental and compound semiconductors likely to be used. Developing RF and AMS technologies for such applications is not straightforward. Cost versus performance is one of the key factors determining the location of boundaries between the kinds of RF semiconductors (e.g., Si, SiGe, GaAs, and InP) shown in the top part of Figure 1. These boundaries are broad and diffuse, and they change with time and application. Two or more technologies may coexist with one another for certain applications. This means that we have to address and discuss the intersection of Si-based technologies, such as CMOS, BiCMOS (bipolar and CMOS), and SiGe heterojunction bipolar transistors (HBTs), with III-V compound semiconductors and other potential technologies, such as microelectromechanical systems (MEMS), bulk acoustic wave (BAW) devices, and passive components. In addition, we must consider the frequency of operation and other criteria such as costs and specifications given by the different communication standards. Together, they will determine device needs and even the choice of technology.

Figure 2 shows the circuit functions of a typical mobile communication system operating between 0.8 and 10 GHz. These frequencies refer to the operating or carrier frequencies of the wireless systems (and not to device corner frequencies or circuit clock frequencies). The four basic circuit functions shown therein are RF transceiver, AMS, power amplifier (PA) and power management (PM), and digital signal processor (DSP). In this article, we emphasize the first three circuit functions, which drive analog and RF technology needs. The DSP is addressed by other parts of the ITRS roadmap and will not be discussed here. Each of those three major parts in a RF front-end for a wireless system will be discussed in a separate section with special emphasis on the device needs and technology choices for those blocks and with main focus on the frequency range from 0.8 to 10 GHz. A section on millimeter wave circuits and devices will cover device and technology integration issues for applications in the frequency range starting from 10–100 GHz. Strictly speaking, millimeter wave frequencies begin near 30 and not 10 GHz. We use 10 GHz for the approximate beginning because the technical challenges between 10 and 30 GHz from a technology roadmapping perspective are similar. Finally, we will discuss the evolution of technology choices, integration issues, and potentially new emerging devices, all within the timeframe for the 2003 ITRS roadmap (2003–2018).

ANALOG AND MIXED-SIGNAL: REQUIREMENTS AND CHALLENGES

Mixed-signal ICs contain analog and digital circuitry. Analog circuitry refers to circuits such as amplifiers or filters for which the signals vary continuously. Digital circuitry refers to circuits for which the signals have two values or states. Mixed-signal circuits

or chips often utilize both analog and digital functions such as analog-to-digital (A–D) and D–A conversion. The focus of "purely" analog circuitry is shifting to higher and higher frequencies due to the increasing performance of post-analog digital signal processing. However, A–D and D–A conversion performance becomes increasingly important as it opens the door to new high-volume but low-cost applications. The commodity driver applications for mixed-signal ICs are projected to remain in consumer and communication markets where off-chip interfaces require analog signals. Analog devices must often reuse and leverage mainstream digital CMOS technology to remain low cost and meet the demand for high performance and reliability.



2. Circuit functions of a typical mobile communication system.

Successful mixed-signal technologies will benefit from mainstream digital technologies by integrating more value-added features and functions. Key ingredients to successful mixed-signal integration are the addition of special higher voltage analog precision transistors, high-quality passive elements, adequate signal isolation, and compatible active devices. Precision transistors have thicker oxides and longer gate lengths compared to standard digital CMOS transistors and have certain benefits that will be discussed later. High-quality passive devices often require additional processing steps in the back end of the line.

This section includes discussions of analog high-speed devices, analog precision MOS devices, and capacitors and resistors. All devices are optimized for precision, matching performance, 1/f noise, low nonlinearity, and low temperature gradients. The acceleration of the CMOS roadmap in recent years has hastened the integration possibilities of analog in logic processes. Continued focus on 1/f noise, passive component density, and device matching is imperative to satisfy the increasing demands on power, speed, and area efficiency.

The change from constant voltage to constant field scaling in the 1990s had consequences for analog scaling. The dynamic range of operation for an analog circuit is given by the difference between the maximum available signal (~ supply voltage) and the minimum detectable signal (determined by noise and distortion). Since supply voltages for CMOS tend to decrease with each new technology generation, the upper boundary for dynamic range decreases as well. At least, to maintain a constant dynamic range available for circuit design, noise and distortion have to decrease for each new CMOS technology.

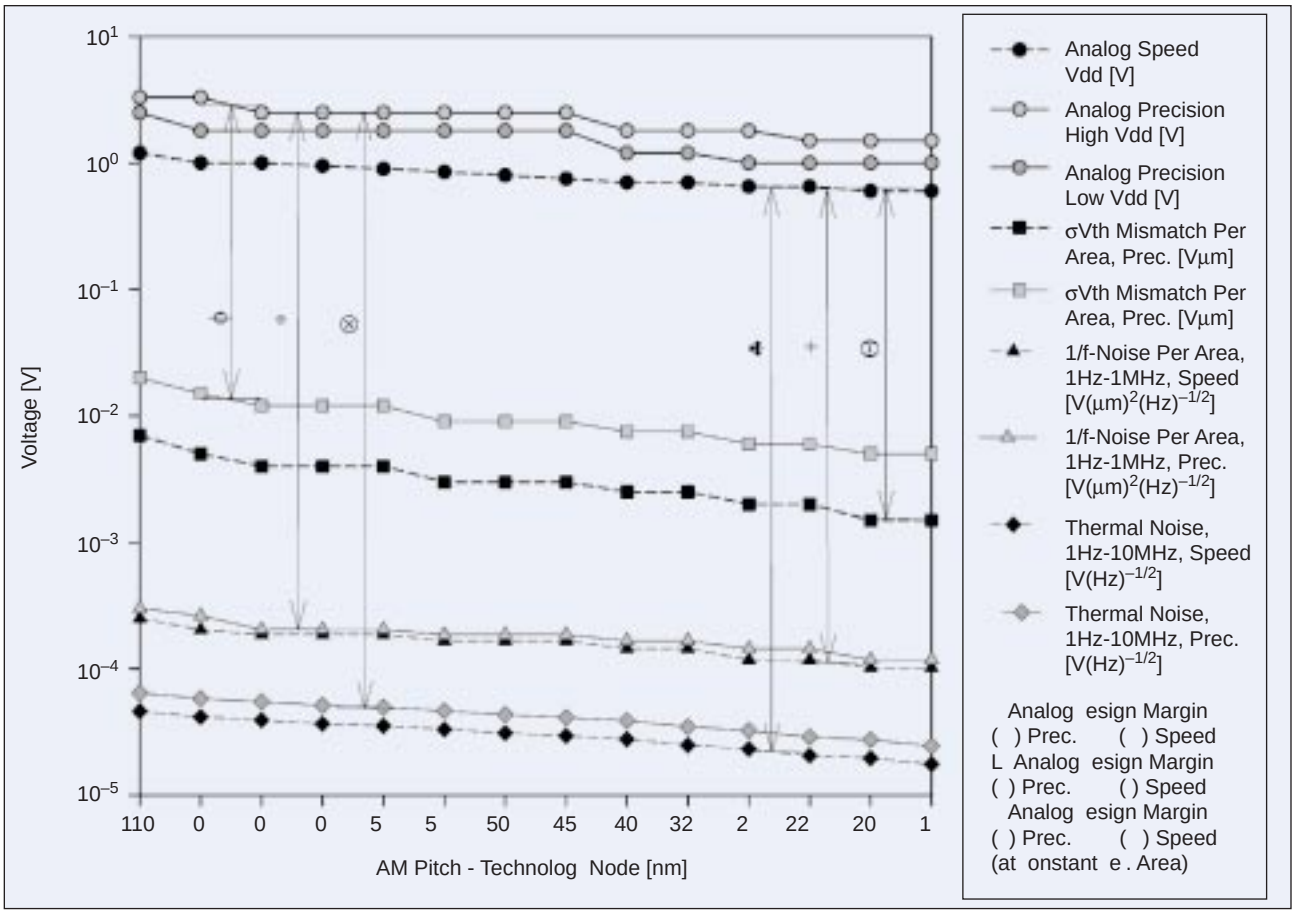
Figure 3 shows the evolution of the supply voltages and the most important types of distortion and noise for MOS transistors in circuits for the three different frequency bands of dc, low frequency (LF), and RF at the technology nodes given in the 2003 ITRS. Here the supply voltage is given in volts, but some noise numbers are given in volts per square-root of frequency, and other noise numbers are given in volts per square-root of frequency and per unit area. Having the same dimensions for all parameters would make direct comparisons easier. However, because frequency and area are parameters used by circuit designers, we keep the three different dimensions and define three analog margins as follows:

1) the product of supply voltage and mismatch per unit area
2) the product of supply voltage and 1/f-noise per unit area
3) the product of supply voltage and thermal noise.

The above three margins give three relative numbers that relate to the dynamic ranges available in a given technology for low, medium, and high frequencies. These margins depend on circuit topology and designers' choice for frequency. Even though slightly different parameters are used, the difference between supply voltages and noise levels approximate the trends in the dynamic ranges that are available for analog design at each CMOS technology node. Figure 3 shows that the analog margins remain approximately constant over technology generations for the case of a constant area occupied by the devices.

Continued circuit performance improvement with scaling is a demand in analog circuit design, but it is not assured from these dynamic performance numbers. Increasing the device area in many cases results in increasing analog voltage margins, but at the penalty of increasing analog chip area and/or power consumption. Progress in analog technology is achieved by increasing the speed of the devices in new CMOS technologies (see Figure 4). Speed is driven by F_{max} as shown in Figure 4. Other possible performance tradeoffs are even overcompensated in this way. A more detailed view on the interplay of device and circuit performance is given in [5].

Due to the increased available signal swing and the need to reuse analog IP-blocks over two or more technology nodes, a second, mixed-signal supply voltage for analog precision devices is often introduced in the process platform. It normally lags that of high-performance digital supply by two or more generations and shows a slightly higher analog margin. A combination of multiple gate oxide thickness, multiple thresholds, and dc–dc conversion is needed to support the steadily increasing mixed-signal requirements. To accommodate higher voltages, analog



3. Performance metric of several analog active device parameters from the 2003 ITRS roadmap versus technology node.

precision transistors have thicker gate oxides than standard logic transistors have. This use of thicker gate oxides has two benefits: it continues to support interfaces to the outside world and simultaneously meets the high signal-to-noise requirements for mixed-signal applications. The latter are achieved at the expense of some matching and 1/f noise scaling performance but at a slight increase in analog margin, as shown in Figure 3.

Many challenges will arise when trying to achieve technology integration of the foregoing device features with scaled technologies. For low mismatch, circuit design techniques like active mismatch compensation are already under discussion. Active mismatch compensation is the active calibration of an analog circuit by adding more calibration circuitry. New technologies like fully depleted silicon on insulator (FD-SOI) may relax problems in achieving sufficient matching performance for new technology nodes [6].

A major challenge for 1/f-noise especially in analog high-speed devices will be the adoption of high-κ gate stacks for digital MOS devices, starting with the 65 nm node. Because interface state density is expected to be strongly enhanced here compared to SiO_2 gate dielectrics, this will result in much higher 1/f-noise for those devices. However, initial results for 1/f-noise with high-κ dielectrics show that this probably will not be an analog show-stopper [6].

Solutions in active threshold regulation, substrate biasing, and novel design architecture will be required to decrease signal swings at lower supply voltages. An alternative to full analog integration is the use of system-in-package (SIP), which combines circuits from different technologies and is optimized for the desired functions.

The trend of moving discrete passive elements from board level to chip level is driven by cost and by demand to reduce board space and increase analog design freedom. Alternatively, some passives may be integrated into the printed board or package as a method of cost reduction and simplification. Finally, cost-efficient solutions for achieving discrete-equivalent precision on-chip passive components are expected. Integrated capacitors with new high-κ dielectrics are needed to reduce their area, mismatch, and distortion properties at a constant leakage current. Integrated resistors need low parasitic capacitance and high-temperature linearity at a low mismatch and 1/f-noise level.

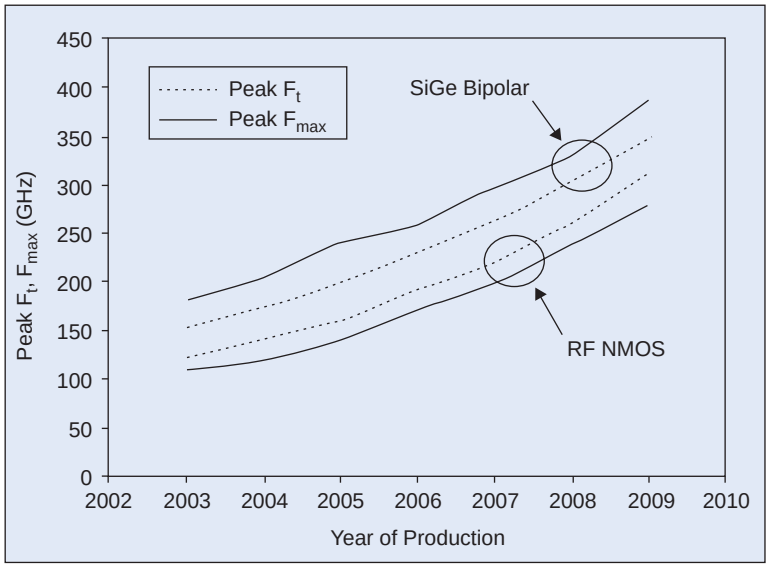
The most important parameters for relative accuracy of the devices with respect to available signal swing, which again is determined mainly by the supply voltage, are shown in Figure 5. For capacitors, they include relative device mismatch and low integral nonlinearity. The integral nonlinearity relative to signal swing is given by the product of device nonlinearity in ppm/V^2 and the supply voltage. For resistors, the most important parameters include low mismatch and low 1/f-noise.

Challenges for passive device integration arise from low cost (low area, low additional mask count) and from the integration of new materials, especially from high-κ dielectrics for capacitors.

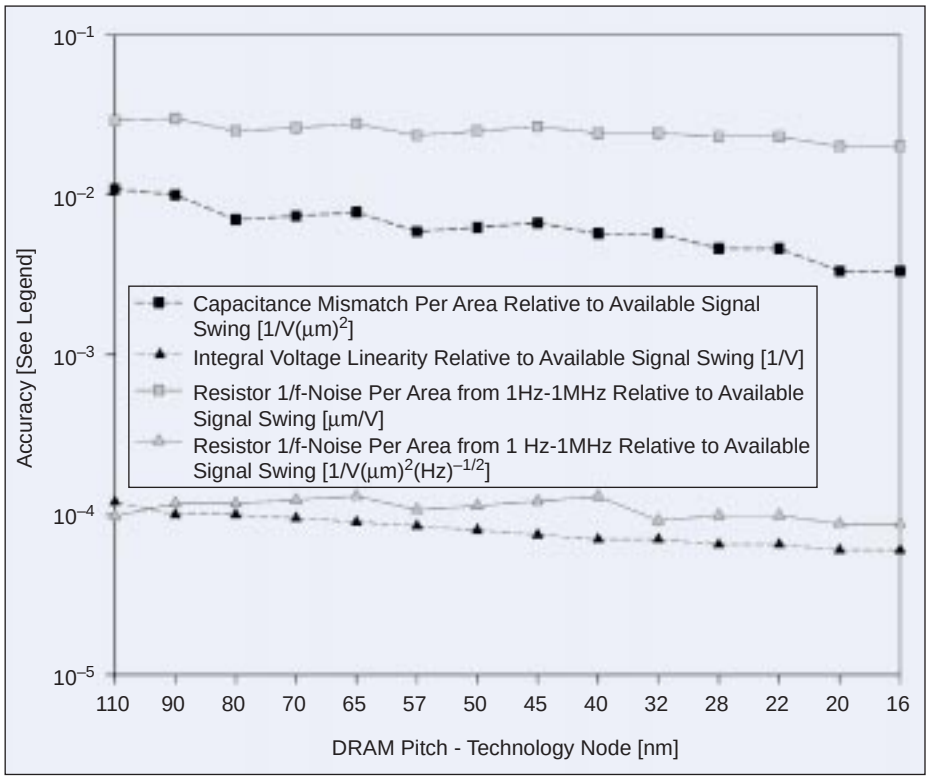
As the integration density increases and the operation frequency rises, protection of noise-sensitive analog circuits from "noisy" digital circuits will become increasingly difficult. Signal isolation is managed through a combination of substrate (e.g., high resistance), interconnect, and package solutions. Today, circuit blocks are protected by oxide isolation, guard rings, and buried wells (triple wells). Integrated shielding structures may be required for protection of circuits and interconnects in the future. Novel design architectures may be employed to enhance circuit signal/noise performance. The introduction of SOI—though positive for signal isolation—will pose additional challenges for mixed-signal circuits. Analog device performance for the SOI process is an area of research. Thermal and floating-body effects as well as high-resistive substrate connections pose challenges for circuit design. FD-SOI may relax most of the problems associated with isolated body devices [6]. However, in contrast to partially depleted (PD)-SOI, we do not even know the detailed electrical behavior and yield characteristics of those devices in complex analog circuits. Finally, any cost-effective solution addressing these problems and challenges must be compatible with the mainstream CMOS technology of the time.

With the steady improvement in high-frequency performance and decrease in speed-power product of CMOS, this technology will continue to gain on traditional BiCMOS and bipolar implementations. BiCMOS processes will continue to be strong in the high-performance application areas that require high speed together with high dynamic range, especially when output power is needed to drive off-chip, low-impedance loads. This strength in high performance occurs because the bipolar devices are carefully optimized and have intrinsic but nonscaling advantages in gain, noise, and matching. In contrast, CMOS analog devices have equally good frequency behavior combined with lower cost and steadily improved but slightly lower performance on the other parameters.

Continuously increasing digital processing capabilities enable more signal treatments to be done in the digital domain. It is expected that full-digital implementations in CMOS will replace most historically analog functions (e.g., most analog filtering) and that digital clock frequencies will increasae with technology node except for signal amplification and A–D conversion. This trend started in the mid-1990s and will continue with decreasing energy consumption per logic operation, decreasing area per function, and increasing parallel processing capabilities of modern digital circuits. Besides analog-related technology improvements, this has been and will continue to be a major driver for the success of signal processing applications.



4. Peak F_t and F_{max} at 5 GHz for SiGe bipolar and RF NMOS devices as predicted by the 2003 ITRS.



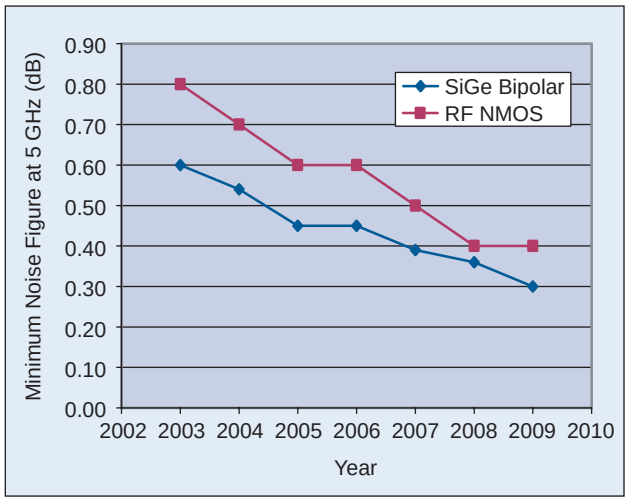
5. Performance metric of several analog passive device parameters relative to the available signal swing (roughly determined by the supply voltage) from the 2003 ITRS roadmap versus technology node.

RF TRANSCEIVERS: REQUIREMENTS AND CHALLENGES

RF transceivers include both receive and transmit chains that perform amplification, filtering, and frequency conversion. The receiver and transmitter chain may be on one or multiple ICs and convert the carrier frequency to a lower frequency which can be used by the A–D converters (ADCs) or D–A converters (DACs) discussed in the previous section. This conversion can occur in one step in a *direct conversion* architecture or multiple steps in a *heterodyne* architecture. While the two architectures drive slightly different requirements in performance and linearity, major building blocks of an RF transceiver are depicted schematically in Figure 2 for both cases. These building blocks include the low-noise amplifier (LNA), the frequency synthesizer that makes use of voltage controlled oscillators (VCOs), mixers for the down and up frequency conversion, and drivers which amplify outgoing signals for transmission by a PA described in the next section.

Technologies used today to realize RF transceivers include silicon BiCMOS, SiGe BiCMOS, and RF CMOS. BiCMOS technologies (Si and SiGe) dominate today the RF transceiver markets for carrier frequencies below 10 GHz. BiCMOS technologies enable the use of bipolar devices for LNAs, low-power pre-scalers and power drivers and CMOS devices for frequency synthesizers and for small amounts of logic. However, RF CMOS transceivers are being introduced for less demanding applications.

The most stringent technology requirements for an RF transceiver are driven by the demands of the LNA/mixer, VCO, and power driver. We will discuss these in more detail in this section. LNA/mixer design involves a tradeoff between power consumption, gain, noise figure (NF), and linearity. This tradeoff is related to basic device parameters described by the 2003 ITRS roadmap such as F_t, F_{max}, and minimum NF. Figures 4 and 6 depict the 2003 ITRS roadmap for peak F_t, peak F_{max}, and minimum NF at 5 GHz for both SiGe bipolar and RF CMOS devices. The abscissa in these figures is the year of volume production. Based on the roadmap, SiGe devices are expected to maintain a performance advantage over CMOS for each of these figures of merit at each technology node. To close this gap, it is typical to use more advanced CMOS nodes (by one or two generations) to realize similar performance to older SiGe BiCMOS nodes.



6. Minimum noise figure at 5 GHz for SiGe bipolar and RF NMOS devices as predicted by the 2003 ITRS.

Performance of the VCO is typically measured by phase noise (magnitude of the signal at an unwanted frequency relative to the magnitude of the signal at the center frequency). Phase noise, and, thus, VCO performance, are typically linked to the quality of inductor and varactor elements that are resonating at the center frequency and to the 1/f noise of active devices. Bipolar devices have a significant advantage over RF CMOS devices in 1/f noise. This advantage is expected to increase with more advanced technology. But good performance VCOs have been realized in RF CMOS despite their 1/f noise. Inductor performance is less a function of the underlying device technology (RF CMOS versus BiCMOS) and more a function of the metal and substrate resistivities. High-resistivity substrates and low-resistivity thick metal layers are being deployed both in RF CMOS and BiCMOS technologies to offer improvements in inductor quality factors (Qs) and enable integration of higher performance VCOs.

Drivers are responsible for preamplifying an outgoing signal to feed a PA module. Because large output power is desired, the ability to handle higher voltages is a desirable feature. For this reason, high-voltage (HV) transistors are integrated both in CMOS and SiGe technology. Figure 7 shows the maximum voltage-handling capability of HV SiGe bipolar devices [limited by breakdown voltage between collector and base, emitter open (BVCBO)] and HV CMOS devices (limited by reliability), and Figure 8 shows the F_{max} of the these HV devices as defined by the ITRS roadmap. A large advantage exists for SiGe technology, both in voltage-handling capability and F_{max}, that is not reduced in advanced CMOS nodes. Laterally diffused MOS transistors (LDMOS) or drain-extended MOS transistors offer possible solutions to this problem for RF CMOS technology at the expense of a couple of additional masking layers.

In summary, we have shown that current architectures lend themselves to implementation in either RF CMOS or Si and SiGe BiCMOS technology, with BiCMOS technology dominating the market at present for carrier frequencies below 10 GHz. As RF CMOS is scaled, it can compete better in performance with SiGe bipolar devices. But, other advantages of SiGe technology, such as the ability to integrate efficiently power drivers, can actually become more significant as CMOS supply voltage is reduced. Cost favors a CMOS transceiver in a given technology node, but, if a more advanced RF CMOS node is required versus an older BiCMOS node to meet performance requirements, cost may or may not be on the side of the RF CMOS solution. Finally, the cost of the overall radio is being reduced by the integration of more functionality on fewer components. Integration of the transceiver with the analog and digital sections of the radio favors an RF CMOS solution while integration of the PA and PM functions with the transceiver favor a BiCMOS solution. It is likely that these multifaceted constraints will drive different decisions for different markets and standards such that both BiCMOS and RF CMOS transceivers will co-exist in the market for the foreseeable future.

PAs AND PM: REQUIREMENTS AND CHALLENGES

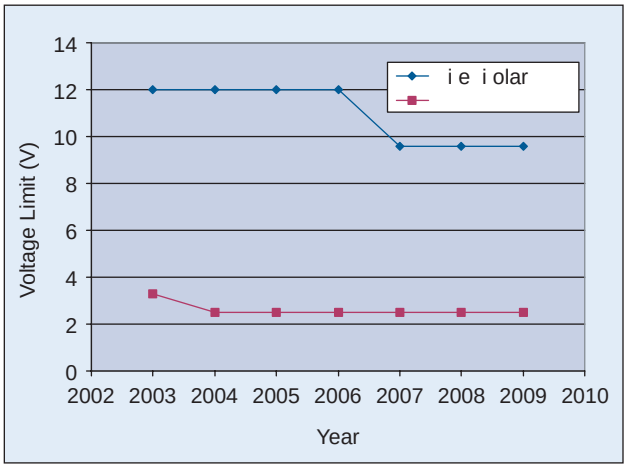
In 2003, the bulk of the consumer market (subscriber) for PA technologies continued to be RFICs and modules for cellular subscriber handsets, with handset volume yearly sales exceeding 400 million units. The cellular PA industry is already supporting components in large volume for two-and-one-half and third-generation handsets that are capable of delivering much higher data rates necessary for convenient wireless Web access functions. WLAN applications have also become another significant driver of integrated PA modules, with volumes expected to exceed tens of millions of units in 2003. Both applications have very strict RF performance specifications and are extremely sensitive to price/performance tradeoffs. This tradeoff continuously drives the industry towards highly integrated low-cost system solutions. The market for PAs is increasingly migrating away from packaged single die (RFICs) to multiband, multimode, integrated modules, delivering a complete amplifier solution. These RF modules typically integrate all or most of the matching and bypassing networks and may also provide power detection, PM, filtering, and RF switches for both transmit/receive (T/R) and band selection.

As a logical extension of the integrated PA module, there is increased activity in the integration into the module of all other radio functions, such as transceivers, frequency synthesis, filters, and digital sections, amongst others. Such integration provides a true single radio module solution in a small footprint with a digital interface to the handset's DSP/CPU. There is little doubt that such SIP single radios will eventually become commonplace in the industry. The challenges for the semiconductor technology community will likely be how to meet the cost and performance targets, with as much integration as possible available in the semiconductor technologies.

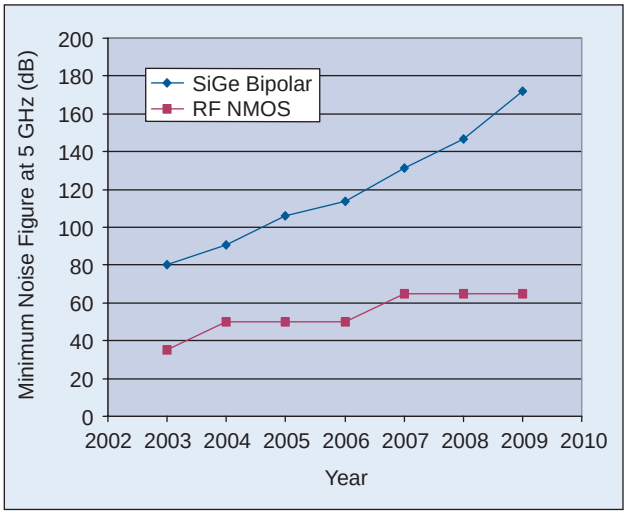
Because RF PAs have large signals, they require significant ruggedness and higher breakdown voltages than available in standard CMOS submicron technologies. In addition, since these amplifiers operate in battery-powered devices with typically 3 V, semiconductor technologies must have their performance optimized for low voltages. Today, these PAs are typically built as standalone components with either GaAs HBT, Si LDMOS, or GaAs pseudomorphic high electron mobility transistor (PHEMT) technologies. At this time, InP-based HBT devices do not appear to have found a niche in commercial PA applications due largely to increased cost and fabrication complexity. There are significant research and initial product releases for SiGe BiCMOS and standard Si CMOS technologies for use in cellular PAs. But, no market penetration of these technologies has occurred to date. The integration of the RF power function into the silicon system-on-chip (SOC) solution requires significant device optimization and development efforts. These efforts are not just aimed at realizing the required RF functionality, but also the required isolation necessary for effective system integration.

PM ICs are required for all but the simplest of wireless applications. Power management ICs condition the power demands of the RF PA and other wireless circuit blocks, regulate battery/charger surges, detect power levels, and provide the appropriate temperature/ ruggedness/leakage control for efficient system operation. This PM function is typically accomplished with HV CMOS technologies and typically requires very large periphery pass FET devices. The periphery of a pass FET refers to the combined width of all fingers that comprise the device. The combined width typically exceeds hundreds of millimeters in order to achieve very low series resistance. It is expected that the PM function will also be integrated as part of the SOC technology, instead of a separate IC within a module.

Since the module footprint is continually shrinking while the module complexity is continually growing, a technology capable of integrating more of the radio functions will ultimately be the technology of choice for cellular handsets. Two of these RF functions are filters and T/R switches. If MEMS switch reliability improves and their voltage requirements decrease, they can potentially offer a post-processing integration solution



7. Maximum voltage limit of HV bipolar devices and HV RF NMOS devices plotted as a function of year. The y-axis is determined for SiGe bipolar devices by their BVCBO given in the 2003 ITRS and for RF NMOS devices by their reliability imposed power supply limits.



8. Peak F_{max} plotted for HV SiGe bipolar and HV RF NMOS devices as described by the 2003 ITRS roadmap.

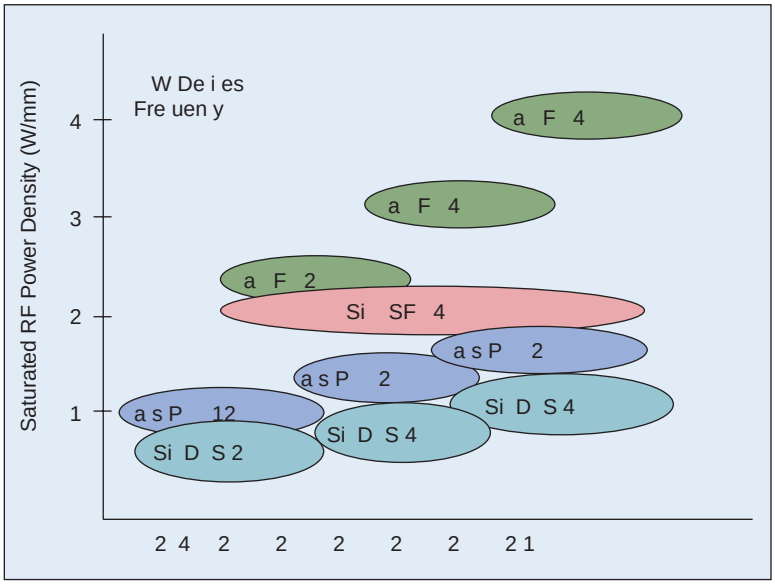
for both GaAs and Si technologies. Integration of filter functions also presents an issue for inclusion in semiconductor technology. To date, only thick film bulk acoustic resonator (FBAR) technologies and MEMS resonators have appeared as possible candidates for integration.

The signal isolation specifications necessary for the system integration of cellular chipsets represents a very significant challenge to both technologists and electronic design automation (EDA) tools providers. With the exceedingly high RF voltage created by the PA and PM circuits, in addition to the numerous frequencies generated internally by the IF blocks, signal isolation may become the most difficult obstacle preventing full SOC implementation.

Cellular base stations also present unique challenges to semiconductor technologies. Base stations provide the communications infrastructure to handle many local subscribers, require much larger RF power and linearity levels, and have much higher reliability specifications. The 2003 base station semiconductor market is primarily at 2 GHz and below. The future market is projected to expand to higher frequencies as new applications and frequency bands are allocated. Cost as measured by dollars per RF watt is projected to steadily decrease from about US$1/W today to less than US$0.50/W by 2008. The application space is undergoing a conversion from ceramic to plastic packaging that will drive much of the cost reduction. In 2003, Si LDMOS FETs are the dominant semiconductor technology, easily commanding a 95% market share with GaAs FETs picking up the rest. SiC and GaN FETs are now appearing over the technology horizon, but significant research and development is required before these technologies approach mainstream manufacturing.

A major trend for all semiconductor device technologies is the move to higher operating voltage that will increase power density and reduce device size for the same output power. The reduced device size requires less complex impedance matching networks, reduces power loss, and increases power efficiency. The RF power density trend for 60-W devices at frequencies less than 5 GHz versus time for various semiconductor technologies (Si LDMOS, GaAs PHEMT, SiC MESFET, and GaN HFET) is shown in Figure 9. The power density of RF power FETs is usually given in terms of watts-per-millimeter of gate width. The major trends shown in Figure 9 are the increase in operating voltage and the resulting increase in RF power density from 2004 to 2010. The power density of Si LDMOS, the present workhorse of the base-station industry, will increase from about 0.7 W/mm at 28 V to 1.2 W/mm at 48 V in the 2009 timeframe. GaAs PHEMT power densities are expected to increase from 0.7 W/mm to 1.5 W/mm in the same timeframe. GaAs PHEMT operating voltages will increase from 12 V today to 28 V in 2006. The power density of SiC MESFETs will remain relatively constant over this time frame at 2 W/mm with an operating voltage of 48 V because research dollars for wide bandgap semiconductors will be directed at GaN HFETs which have the potential for even higher power densities. The first commercial 30-W GaN HFETs will appear in 2006 with a power density of 2.5 W/mm at 28 V. By 2008, GaN HFETs with 4 W/mm operating at 48 V will be commercially available. Currently, GaN HFETs are fabricated on a variety of different substrates because of the lack of a GaN substrate. At this time, the most commonly used substrate for GaN HFETs is SiC because of its very high thermal conductivity. However, progress towards high-volume manufacturing is hindered by the small size and high cost of 2-in semi-insulating SiC wafers.

The base station application space is moving away from saturated to more linear PAs to support the digital modulation formats of CDMA and WCDMA. The available linear power from a given device is about half the saturated power from the same device. The power-added efficiencies for devices operated in linear applications are substantially lower by between 15 and 25% than they are for devices operated in saturated applications. Maximum RF output power from a single device will not increase above approximately 240 W unless there is a major change in the design of PA systems. Although LDMOS enjoys a near monopoly in current cellular base stations, there is a concern that its performance at frequencies higher than 2 GHz will not be sufficient to meet the necessary specifications. Failing to meet this challenge will result in the utilization of the other more expensive technologies. A major challenge for GaAs FETs is the move to a higher operating voltage that is closer to the operating voltage of LDMOS (28 V). The major challenge for GaN technology is achieving the very high level of device reliability that has been demonstrated using LDMOS and GaAs. High-heat dissipation packaging will need to be developed to take full advantage of the potential of GaN technology.



9. Power density versus year.

MILLIMETER WAVE: REQUIREMENTS AND CHALLENGES

Today, compound semiconductors dominate the 10–100 GHz range. The device types most com-

monly used for analog millimeter-wave applications are HEMT, PHEMT, and metamorphic HEMT (MHEMT), while MESFET and HBT predominate for mixed-signal and high-speed applications. Except for MESFET and SiGe HBTs, all device types employ epitaxial layer stacks that are composed of ternary or quaternary compounds derived from Columns III and V of the periodic chart.

Because device properties are critically dependent on the selection of materials, thickness, and doping in the stack, which are proprietary to the manufacturer, there is great diversity in the nature and performance of these devices. Tradeoffs among power, efficiency, breakdown, NF, linearity, and other performance parameters abound. One consequence of these tradeoffs is that the "lithography node" is not the primary driver for millimeter-wave performance, although lithography dimensions are certainly shrinking with the drive to high frequency figures of merit (e.g., maximum F_t and F_{max}). Performance trends are driven more by a combination of desirable tradeoffs and "bandgap engineering" of the epitaxial layer stack in concert with shrinking lithography.

Compound semiconductor technologies have a number of similarities with silicon technologies yet, in many ways, are distinctly different. While III-Vs have benefited from the advances in manufacturing equipment and chemistries, the development of these tools and chemicals is focused on the silicon industry and is not necessarily optimum for compound semiconductor processing. Six-inch diameter semi-insulating GaAs wafers are routinely available and are becoming the de facto standard, although some foundries are still at four-inch. The move to six- and eight-inch substrates will be driven not only by economies of scale and chip cost, but also by equipment availability, as the tool industry focuses on products to handle larger wafer sizes used in the silicon industry.

GaAs tends to be two generations behind Si in wafer size, with InP a further generation behind. It is crucial that substrate size keep up with Si advances if the III-V industry is to benefit from advances in processing equipment. This continued pace in substrate size is particularly true for InP and SiC, the latter of which still suffers from a significantly high defect density. Today, there is no production source of GaN substrates; most GaN device epitaxy is done on SiC substrates. Significant technology breakthroughs will be required before GaN becomes commercially viable. Unresolved issues remain regarding SiC versus GaN substrates for GaN HEMTs. Advances in high-resistivity Si substrates must also be addressed as SiGe HBT and RF CMOS push toward the millimeter-wave spectrum.

Device challenges, some of which are unique to III-Vs, include the following:

1) the requirement for substrate vias for low-inductance grounds in microstrip millimeter-wave circuits
2) techniques for heat removal including wafer thinning and low parasitic air-bridge interconnects,
3) high breakdown voltages for power devices
4) nonnative oxide passivation.

While these issues have been mostly solved for GaAs, they need to be applied successfully to emerging III-V technologies of InP, SiC, and GaN. One of the critical challenges for high-power III-V devices is thermal dissipation. This challenge is especially true for high-power density devices such as GaN.

The major classes of millimeter wave transistors are listed in the following paragraphs. While the transport mechanisms and structure within each type are similar, there are vast differences in performance attributable to the selection of substrate material and design of the epitaxial layer stack. See [7]–[9] for more in-depth descriptions of these device technologies.

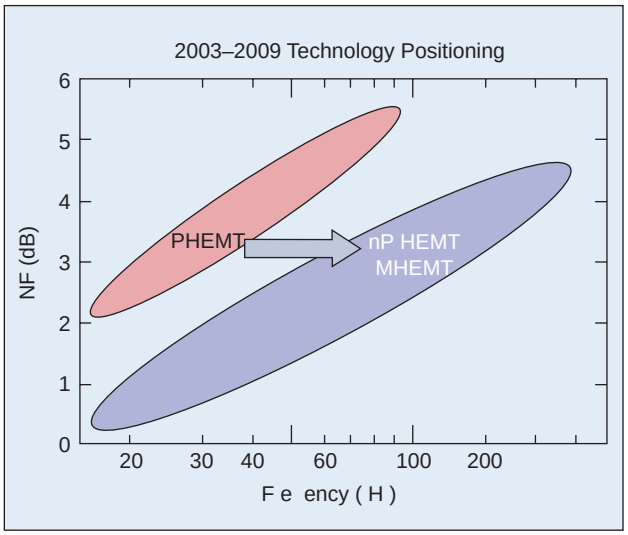
Field effect transistors (FETs) are majority carrier devices in which electron transport is in a thin layer parallel to the wafer surface. The major types are as follows:

1) *MESFETs* are composed of homogeneous layers in which electron transport occurs in an intentionally doped layer and are generally GaAs-based.
2) *HEMTs* are composed of layers of different bandgap materials on a lattice-matched substrate. Carriers in HEMTs are provided by a highly doped layer, and carrier transport occurs in an adjacent undoped layer, resulting in much higher mobility due to the lack of ionized charge scattering. HEMTs are generally InP- and GaN-based.
3) *PHEMTs* are composed of layers with different bandgap materials on a substrate in which the lattice constant of the layers are close, but not matched, to the lattice constant of the substrate. PHEMTs have higher mobility than HEMTs and are generally GaAs-based.
4) *MHEMTs* are composed of layers of different bandgap materials on a substrate in which the lattice constants of the layers are mismatched to the substrate. The resulting strain is taken up by a specially designed buffer layer. MHEMTs offer the highest degree of flexibility in design and in millimeter-wave performance. Generally, they are made on GaAs substrates to take advantage of the more mature materials and processing technologies.

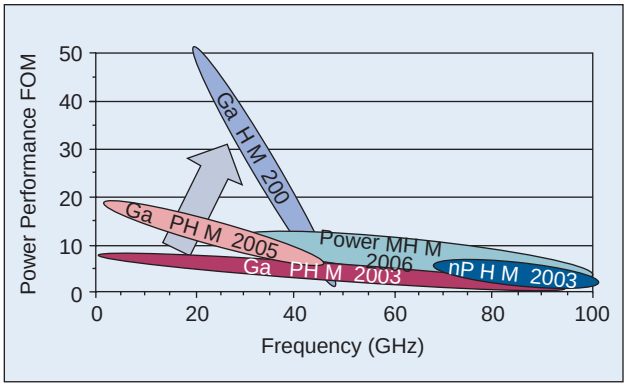
HBTs are minority carrier devices in which carrier transport is perpendicular to the wafer surface. The major types are as follows:

1) *InP HBTs* are composed of ternary and quaternary layers that contain elements from groups III and V, such as In, Ga, As, Sb, and P, and are closely lattice matched to InP substrates. GaAs HBTs are generally used below 10 GHz.
2) *SiGe HBTs* are composed of a single crystal mixture of Si and Ge on a Si substrate.

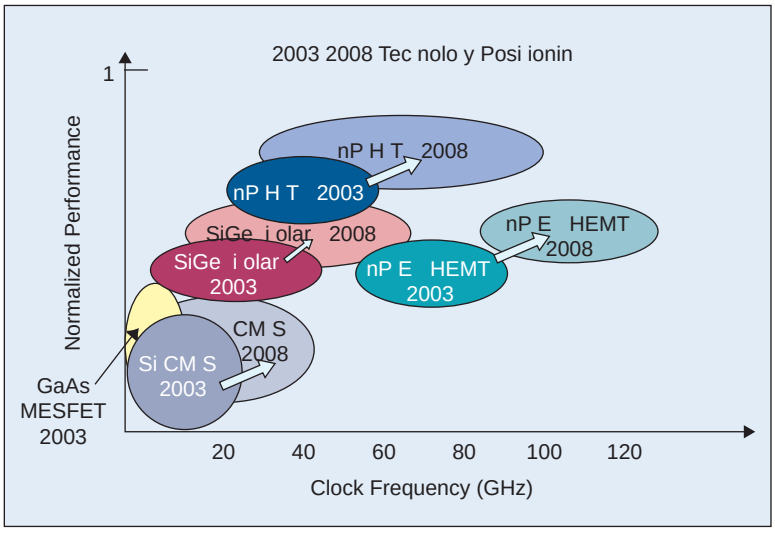
InP HBTs and SiGe are ideal for high-speed logic and mixed-signal applications. These applications are due to the much better threshold control in bipolars, in which the threshold is a function of bandgap (a materials property) rather than the Schottky Barrier and Fermi Level (a processing property). HBTs are also the devices of choice for low-phase noise oscillators. MESFETs are likely to become obsolete for new applications in about 2005 as InP and SiGe cost and performance advantages overtake MESFETs. Although the gap between InP and SiGe is closing, InP will always have the



10. LNAs.



11. The evolution of production power devices 2003–2009. The performance figure of merit is MMIC power density (W/mm) times MMIC SS gain per stage (dB) at application center frequency (typically 10–20% bandwidth).



12. Mixed-signal/ultra high-speed digital: the metric for performance depends on the class of circuit. It can include dynamic range, signal-to-noise, bandwidth, data rate, and/or inverse power.

advantage of higher breakdown, while SiGe BiCMOS holds the advantage for integration density.

The ovals in Figures 10–12 portray the projected technology trends among the various device types over the near term. In Figure 10, the PHEMT oval represents the NF versus frequency for devices commercially available today. While PHEMTs are the mainstay of low noise devices in the millimeter-wave spectrum at present, it is expected that they will quickly be supplanted by InP in the near term and eventually MHEMT by the end of the decade. This projection is exhibited by the InP/MHEMT bubble region that portrays the region in the NF/frequency realm of reported research results through 2003. Current R&D results project future commercial trends. Not only do InP HEMTs and MHEMTs exhibit lower NFs, but also the required dc power dissipation is roughly four times lower for equivalent NF and gain performance.

Figure 11 shows the evolution of millimeter-wave power performance over time. The power performance figure of merit (FOM) is MMIC power density (W/mm) times MMIC small signal (SS) gain per stage (dB) at application center frequency for a typical 10–20% bandwidth. The power bandwidth product for the different device technologies could have also been used and would have provided a similar trend. GaAs PHEMT and InP HEMT are the premier millimeter-wave power devices available today in production, with GaAs PHEMT the preferred technology for frequencies less than 77 GHz. However, present-day GaAs PHEMTs and InP HEMTs do not have the power performance to meet future systems requirements. Continued evolution of GaAs PHEMTs and InP HEMTs will offer increased performance but will still fall short of evolving demands.

In engineering a millimeter power device, the engineer is faced with a dilemma: increased power (or power density) necessitates operating devices either at higher operating voltages or high current densities. For a given device technology, in addition to the tradeoff between operating voltage and current density, increasing operating voltage comes at the expense of high frequency operation or gain. As an example, GaAs PHEMTs that can operate at higher voltages compared to InP HEMTs tend to be gain limited in the upper millimeter frequency range. On the other hand, today's InP HEMTs that have superior high-frequency gain are limited to low-voltage (and subsequently low-power) operation. The challenge for the device engineer is to develop a device structure that combines the best attributes of both GaAs PHEMTs (higher voltage operation) and InP HEMTs (high-frequency gain).

One approach currently under development is MHEMT technology, which takes advantage of bandgap engineering to create a device structure that exhibits the best compromise between the relatively HV operation of GaAs PHEMTs and the high gain of InP HEMTs. As shown in Figure 11, power MHEMT technology is expected to eclipse

both GaAs PHEMT and InP HEMT performance in the 40–100+ GHz frequency range and will be available in production in the 2006+ timeframe.

Another promising approach is the wide bandgap semiconductor GaN. At microwave frequencies, GaN HEMTs have exhibited five to ten times the power density of GaAs PHEMTs, and GaN HEMTs have shown potential for operation through Ka-band. GaN HEMTs achieve this revolutionary power performance through a combination of high current density and significantly higher operating voltage with only modest reduction in gain compared to GaAs PHEMTs. With continued development within the next five years, GaN HEMTs are projected to become the premier and preferred device technology for millimeter-wave power applications through Ka band.

Figure 12 shows the evolution of mixed-signal technology for millimeter-wave applications. Such applications are driven by high center frequency, precise transistor matching, low-noise operation, and high linearity in the underlying technology. With continuous scaling, CMOS technology is expected to address low-resolution circuits up to 10–20 GHz. SiGe bipolar extends the region of silicon performance to 40–50 GHz, but will likely be limited in dynamic range due to the breakdown voltage (BVCEO) being less than 2 V. InP HBTs are the ultimate performance technology once the core transistor technology is aggressively scaled. InP HBTs will be limited by substrate size that is typically at 100 mm, but with 150 mm being sampled. InP enhancement/depletion (E/D) HEMTs offer higher frequency operation than InP HBTs when scaled to less than 100 nm.

E/D technology is also lower power than the HBT alternative, but the threshold voltage control of the HEMT is not as good. The HEMT also does not have as good 1/f noise performance as the HBT. E/D technology should operate at lower power than similar HBT circuits.

For applications where high dynamic range is required (e.g., auto radar), bipolar devices are often preferred due to their high linearity and low 1/f noise. The market for advanced mixed-signal circuits will most likely drive increased wireless communications bandwidth through the real-time correction and synthesis of analog signals using digital technologies. To do this, the associated digital and mixed-signal circuits must run three to ten times faster than the analog carrier frequency. Additional opportunities exist for performing the control and routing in optical networks.

Compound semiconductors must take advantage of the advances in lithography and processing equipment that are evolving now in the digital silicon industry. In order to accomplish this, wafer diameter needs to be within one or two generations of the silicon industry. Six-inch semi-insulating GaAs wafers are in production now with InP not far behind. However, the III-V industry needs to continue to push to larger wafer sizes as silicon transitions from 8- to 12-in diameter wafers. While significant advances are being made in optical lithography tools, the cost of masks is prohibitive for most of the relatively low volume III-V applications. Direct-write electron beams are a solution to the mask cost, but wafer throughput (measured in hours per wafer, as opposed to wafers per hour) needs to be improved with high-current electron sources and fast alignment systems.

Substrate quality is still problematic for emerging wide bandgap devices. Research on GaN templates is continuing, but, in the interim, SiC substrates will become more viable as defect density is improved. If SiGe is to challenge the millimeter-wave spectrum, high-resistivity low-loss silicon needs to be addressed.

Thermal dissipation is the major challenge for wide-bandgap III-V power devices. While GaN and SiC substrates have higher thermal conductance values compared to GaAs and InP, the 5× to 10× higher power densities typically present in these wide bandgap semiconductors somewhat offsets the advantage in higher thermal conductance. These circumstances make thermal dissipation a critical device design aspect. Proven techniques include thin (0.002 in) wafers, thermal shunts, and bathtub vias [10]. These techniques, as well as more innovative solutions, need to be applied to wide bandgap devices.

HV breakdown is desirable for both mixed-signal as well as high-power devices. As dimensions are scaled downward for higher frequency performance, operating voltage suffers. This is particularly troublesome for mixed-signal devices that require more headroom for analog functions than for digital functions. In this regard, InP HBTs offer a distinct advantage over SiGe HBTs, although the integration level offered by SiGe will be orders of magnitude greater. Careful device scaling and wide-bandgap collectors can help maintain breakdown in InP HBTs. For power FETs, gate recessing has been used successfully to achieve higher breakdown, but this has yet to be applied to GaN. Tailoring of the vertical dimensions of the source-drain region to optimize surface electric fields is a potential solution. Continued improvement of passivation and hot carrier effects is also needed.

Finally, high-frequency performance in III-Vs is driven as much by epitaxy (vertical scaling) as by lithography (horizontal scaling). Carrier velocity and mobility in the transport layer can be tailored by proper engineering of the epitaxial layer stack. Continued improvement in all of the III-V devices can be expected through bandgap engineering.

IS THE FUTURE FOR RF AND AMS IN EMERGING RESEARCH DEVICES?

Emerging research devices, such as resonant tunneling devices, spin transistors, carbon nanotubes, molecular electronics, planar double-gate transistors, and 3-D structures including vertical transistors [11], may have possible future RF and AMS applications. In some cases, these possibilities are based on promising first performance laboratory results. All emerging research RF and AMS devices are expected to present severe challenges for high-volume manufacturing, but may also present opportunities for RF and AMS applications that demand increased performance, reliability, and functionality. A common technical challenge for most, if not all, RF and AMS applications of research devices is to understand the chemistry and physics of the electrical contacts at

the nanoscale well enough so that the RF and analog properties are controlled and reproducible in high volumes. Such nanoscale understanding will be enhanced by computationally efficient physical models for carrier transport in elemental and compound semiconductors and accurate, fast, and predictive RF/analog compact models. Also, the figures of merit such as 1/f noise, power added efficiency, linearity, bandwidth, gain, ruggedness, and reliability are not known well enough to advance nanoscale RF and AMS devices. Measuring and determining such figures of merit will present new areas for significant research and development. Today, it is not even clear which, if any, nanometer structures could send enough power to an antenna to be worthwhile and which circuit architecture would be the best choice for wireless systems based on those devices. All this research will exploit the additional degrees of engineering freedom that many emerging research devices offer. Two examples of additional degrees of engineering freedom are independently controlling the voltage of multiple-gated devices and using an electric field applied perpendicularly to the axis of carbon nanotubes to alter their band structures.

SUMMARY AND CONCLUSIONS

Table 1 summarizes the major trends in the RF and AMS technologies presented here. RF and AMS technologies now represent essential and critical technologies for the success of many semiconductor products. There is increased demand for high-end electronic products and products involved with the convergence of computing, digital video, and communications. Such products serve the rapidly growing wireless communications market. They depend on many materials systems, some of which are compatible with CMOS processing, such as SiGe, and others of which are not compatible with CMOS processing, such as those compound semiconductors composed of elements from groups III and V in the periodic table.

The consumer portions of wireless communications markets are very sensitive to cost. As a result, developing RF and AMS technologies for such applications is not straightforward. The boundary between the Group IV semiconductors Si and SiGe and the III-V semiconductor GaAs has been moving to higher frequencies with time and for other applications the boundary between GaAs and InP is tending to shift to lower frequencies. Eventually, MHEMTs may displace both GaAs PHEMTs and InP HEMTs. The wide bandgap semiconductors such as SiC and GaN, which are not shown in Figure 1, will be used for infrastructures such as base stations at frequencies typically above about 2 GHz. Increased interests for the 94-GHz band arises from its applications for all weather landing and contraband detection. III-V compound semiconductors have additional metrics than those usually associated with CMOS processes. These other metrics include carrier frequency for wireless applications and the printed gate length.

The frequency range between about 10–40 GHz is the region in which the interplay and competition among elemental and compound semiconductors is expected to occur. Today, group IV semiconductors (Si and SiGe) dominate below 10 GHz, and III-V compound semiconductors dominate above 40 GHz. This range in frequencies for competition amongst elemental and

Table 1. Summary of major trends.

Analog Mixed Signal

- More and more analog functions are being realized by digital implementation instead of by analog implementation. However, increasing mixed-signal performance will drive new applications and cheaper implementations of existing applications.
- AMS functions tend now to be integrated together with other digital CMOS functions or sometimes alternatively with RF or PM ICs on the same die because cost is the by far the most important driver. Process choice may either be BiCMOS or CMOS technology.
- Cost may be even more important for AMS functions than for the other transceiver functions. CMOS implementation is occurring in some cases even without high-precision analog transistors or precision passives that require additional masks.

RF Transceivers

- RF transceivers are migrating from heterodyne to direct conversion or low-IF architectures. These architectures directly convert the carrier frequency to a low frequency that feeds the AMS functions, thereby simplifying frequency conversion by eliminating intermediate steps and reducing the number of external components.
- RF transceivers are built today in Si, SiGe BiCMOS, and RF CMOS. Both BiCMOS and RF CMOS transceivers will co-exist for the foreseeable future to address the varied market needs of wireless communication devices. Technology choice is dominated by tradeoffs that include the following:

1) required performance of the standard
2) market being addressed—SiGe BiCMOS typically has higher performance
3) level of integration—RF CMOS enables integration with more digital functions while SiGe enables integration with more PM or PA functions
4) cost—RF CMOS is less expensive than SiGe BiCMOS of the same generation node.

PA and PM

- Highly integrated PA modules will be realized on multilayer laminates or ceramics with embedded passive technologies. In addition to the active power die, these modules will also provide all necessary matching, bypassing, band switching, PM, and filtering (SAW/BAW) functions.
- There will be a trend to improve the performance of silicon technologies (MOS and bipolar) towards cellular RF amplification through both technology and circuit design optimization.
- Plastic will become the dominant packaging format for base station semiconductor devices and will significantly reduce the component cost.
- The use of compound semiconductors and higher operating voltages will increase the RF power density of base station devices.

Millimeter-Wave

- SiGe will challenge InP HBT for applications up to 40 GHz, while InP will predominate for mixed signal applications up to 100 GHz in the near term. In the far term, SiGe may challenge InP for high-volume applications such as 77-GHz auto radar.
- MHEMT will supplant GaAs PHEMTs and InP HEMTs through out the spectrum for low noise/front end and power applications above 40 GHz, while GaN will make inroads up to 40 GHz by the close of the decade.

compound semiconductors changes with time and is expected to move to high frequencies. Nevertheless, while SiGe has shown capability in the 10–40 Gb range, it is an open question whether it will be able to replace III-Vs in applications where either high power gain or ultra-low noise is required.

In future years, we expect the frequency axis in Figure 1 will lose its significance in defining the boundaries among technologies for some of the applications listed therein. This expectation occurs because most of the technologies in Figure 1 can provide very high operating frequencies. The future boundaries will be dominated more by such parameters as NF, output power, power-added efficiency, linearity, and cost. Performance tends to increase in the following order: Si CMOS, SiGe, GaAs, and InP metamorphic. Two or more technologies may coexist with one another for certain applications, such as cellular transceivers, modules for terminal PAs, and millimeter-wave receivers. Today, BiCMOS in cellular transceivers has the biggest share in terms of volume compared to CMOS. But, the opposite may occur in the future. Today, both GaAs HBT and discrete LDMOS devices in modules for terminal PAs have big market shares compared to GaAs PHEMT and GaAs MESFET devices. In the future, silicon based technologies having higher integration capabilities will gain importance. Today, we see GaAs PHEMT and InP HEMT in millimeter-wave receivers. In the future, we may see competition from SiGe HBT, GaAs MHEMT, and InP HEMT.

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