

An Accurate Current Source With On-Chip Self-Calibration Circuits for Low-Voltage Current-Mode Differential Drivers

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Abstract—An accurate CMOS current source for current-mode low-voltage differential transmitter drivers has been designed and fabricated. It is composed of binary weighted current mirrors with built-in self-calibration circuits. The proposed self-measurement and calibration circuits can calibrate upon the collective effects of different error contributors due to process, power supply, and temperature variations. The design has been fabricated in standard 0.35- μm CMOS technology. Measurement results show that the differential output voltage can be self-calibrated to $\pm 1\%$ accuracy with 16% reference current variation, 60% power supply variation, or 13% load resistance variation, respectively.

Index Terms—Built-in self-measurement, CMOS integrated circuits, current-mode transmitter driver, low-voltage, self-calibration.

I. INTRODUCTION

TO ACHIEVE long transmission distance without causing strong emission, low-voltage current-mode transmitter drivers require accurate current sources so that the differential output voltage (V_{od}) is within a specified range. For higher speed, longer distance, and multilevel data communications, higher accuracy is necessary. The differential output voltage is the product of the current of the current source and the load resistor. The accuracy of the current source is mainly determined by the accuracy of bandgap references and the current mirror, which are affected by process, voltage supply, and temperature variations.

To improve the accuracy of the current mirror, the following three types of methods has been used. The first targets to reduce the drain-source voltage V_{DS} mismatch between the two sides of the mirror, as well as to reduce mismatch between the transistors. Cascaded mirrors have been used to ensure better V_{DS}

matching, however, it is not suitable for low-voltage applications. Then, feedback structures [1]–[3] have been developed to force the matching of the V_{DS} without stacking devices. They are very useful in reducing the V_{DS} mismatch, but cannot compensate for errors caused by transistor mismatch such as size and threshold voltage. The transistor mismatch can be reduced by utilizing common-centroid layout and relatively large transistor sizes [4].

The second type uses dynamic mirror structure [5]–[8] to compensate for the operating condition changes. Typically, two clock phases are necessary to realize auto-zero function, which introduces output ripples. This is not suitable for high-speed data communications.

The third method to improve current mirror matching is to trim the circuit, such as laser trimming [9], [10], electronically connecting/disconnecting resistor networks using Zener-zaps or fusible links [11], [12], current pulse trimming using polysilicon resistors [13], [14], and analog resistive trimming using “trimistor” elements [15]. By using one of these trimming methods after fabrication, the requirements of good drain-source voltage matching and device matching are relieved, i.e., a relatively simple mirror structure with small transistor sizes can be used to reduce the layout area. However, the manufacturing cost of the trimming steps are typically very high. In addition, the trimming can only be done once after fabrication in most cases. They compensate the fabrication mismatches and process variations but cannot dynamically compensate for the variations of operating conditions, such as reference current variation, power supply variation, load impedance variation, temperature variation, and component aging. Trimming techniques based on floating gate devices [16]–[21], on the other hand, can be performed repetitively to dynamically compensate for the above variations. The programming voltage for the floating gate has been reduced, however, it is still relatively high, e.g., about 15 V for the 0.35- μm process. This has been achieved by using high-voltage charge pump units.

The binary-weighted CMOS current mirrors [22], [23] do not require high-voltage charge pump units. With low-voltage operation, they can be digitally tuned to achieve high precision; better than 0.1% accuracy has been reported. This paper utilizes the binary-weighted current mirrors to provide the current sources in the low-voltage current-mode driver. An on-chip self-measurement and self-calibration scheme is proposed to automatically tune the binary-weighted current sources, so that

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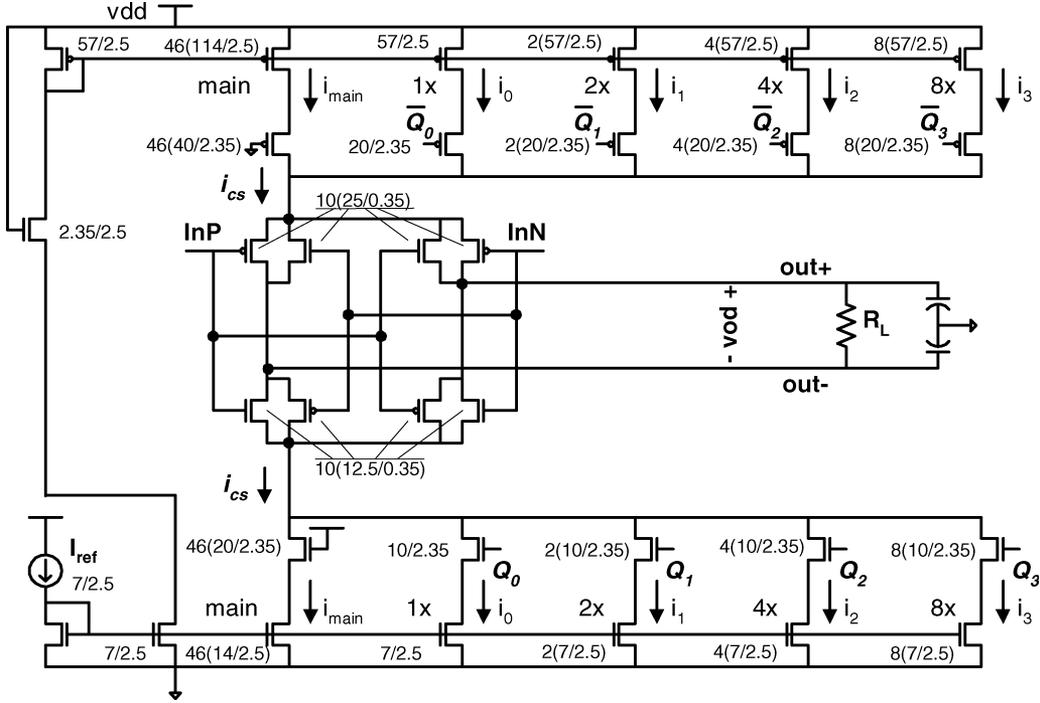


Fig. 1. Current-mode transmitter driver with binary-weighted current mirrors.

the driver differential output voltage is within a specified range around the desired value [24]. With the proposed method, high accuracy can be achieved without using expensive trimming methods or using high-voltage charge pump units. In addition, the proposed circuits can dynamically calibrate upon the collective errors from various sources due to process, power supply, and temperature variations. As a result, with autonomous calibration, a simpler current mirror structure and smaller transistors can be used because perfect mirror matching is no longer necessary; the demand on the reference current accuracy and load resistor accuracy is also reduced. This effectively improves the product yield and lowers down the cost. The design has been fabricated in a standard CMOS 0.35- μm process. Measurement results show that the differential output voltage can be calibrated to be within the $\pm 1\%$ predefined range plus the accuracy of a bandgap reference voltage, with the 16% reference current variation, 60% power supply variation, or 13% load resistance variation, respectively.

This paper is organized as follows. Section II describes the current mode driver with binary weighted current sources. Section III discusses the design of the proposed built-in self-measurement and self-calibration circuits. The measurement results and the conclusion are presented in Sections IV and V, respectively.

II. CURRENT-MODE DRIVER WITH BINARY-WEIGHTED CURRENT SOURCES

Fig. 1 shows the low-voltage current mode driver with binary-weighted current sources in this design. The transistor sizes are labeled in the figure. The current is mirrored from a current reference I_{ref} to five pairs of simple current sources/sinks. One of

them is the main source/sink. The other four are smaller current sources with relative size of 1 \times , 2 \times , 4 \times , and 8 \times among themselves. While the main mirror is always on, the other four can be turned on or off by the switches controlled by the digital binary code Q_0 , Q_1 , Q_2 , and Q_3 . The total current i_{cs} can be expressed by $i_{cs} = i_{\text{main}} + Q_0 i_0 + Q_1 i_1 + Q_2 i_2 + Q_3 i_3$, where i_{main} is the current of the main current source/sink, i_0 , i_1 , i_2 , and i_3 are the currents of the current sources/sinks with size of 1 \times , 2 \times , 4 \times , and 8 \times , respectively. The absolute value of the differential output voltage of the current-mode driver V_{od} is determined by $V_{\text{od}} = i_{cs} R_L$, where R_L is the external load impedance. The signal InP and InN are the complementary digital input signal of the driver; when InP is “1” and InN is “0,” V_{od} is positive; otherwise, V_{od} is negative.

The sizes of the main source, the small source fingers, and the number of adjustable bits should be selected based on the tunable range and minimum adjustable step according to the system requirements. In this design, the main source/sink pair is chosen as 92% of the total target output current, and the 1 \times current source is chosen as 1% of the total target output current in this case. A common on-chip bandgap reference and regulator can have about $\pm 1\%$ initial variation and about 50 ppm/ $^{\circ}\text{C}$ of temperature variation. With additional $\pm 1\%$ possible noise and fluctuation room, the total output variation will be about $\pm 4\%$ over the -40°C – $+160^{\circ}\text{C}$ temperature range. The serial communication standards normally specify $\pm 5\%$ accuracy. Without the proposed self-calibration circuits, the main error contributors are from transistor mismatch (about $\pm 1\%$), load accuracy (about $\pm 1\%$ initial and $\pm 1\%$ temperature variation), power supply (about $\pm 2\%$), reference (about $\pm 1\%$ initial and $\pm 1\%$ temperature variation), temporal noise, and fluctuation (about $\pm 1\%$). The total error is $\pm 8\%$. So, we choose four adjustable bits to cover the $\pm 8\%$ variation range.

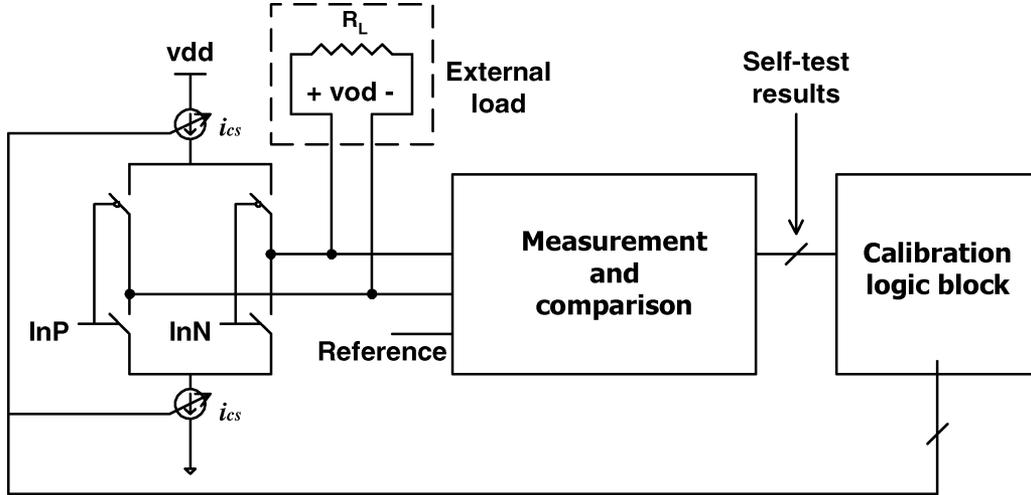


Fig. 2. Built-in self-measurement and self-calibration scheme.

A CMFB circuit [25], [26] can be added for complete design. A potential driver structure using a CMFB circuit is to control the gate voltage of the P-channel current sources with the CMFB voltage, while the N-channel current sources remain the same. Then, after each adjustment of Q_x , the CMFB circuit could function to adjust the gate voltage of the P-channel current sources. In this case, the self-measurement circuits should wait until the CMFB circuits settle before measuring the differential voltage. The speed of the CMFB circuit is typically fast enough so that the waiting time is potentially minimal. When both the P- and N-channel current sources are binary weighted, the variation of the common mode level will be smaller than the case when only one of the current sources is binary weighted.

The functional range of the mirror can be found by measuring the saturation range of the mirrors. The possible input range variation limits are: I_{ref} from 0 to ∞ ; R_{load} from 0 to ∞ ; V_{dd} from 0 to 4.0 V (limited by pad ESD circuit); and Q_x from 0000 to 1111. Simulations were carried out by adjusting each parameter individually while keeping other parameters at the ideal value. To ensure the saturation of the current mirror, the acceptable input ranges are I_{ref} from 5 to 120 μA , R_{load} from 0 to 400 Ω , and V_{dd} from 2.0 to 4.0 V, while the Q_x value does not affect the saturation status of the mirror.

III. BUILT-IN SELF-MEASUREMENT AND SELF-CALIBRATION CIRCUITS

Fig. 2 shows the system architecture of the built-in self-measurement and self-calibration scheme. The differential output of the driver is measured; the measured value is then compared with the reference voltages. The comparison result indicates whether V_{od} is within the desired range; furthermore, it also indicates whether the V_{od} value is above or below the reference range. This signal is used by the calibration logic block to tune the current of the driver so that the output reaches a desired value range.

In this design, it is chosen to perform calibration when the driver is not transmitting signals. The main reason is that, when the driver is transmitting high-frequency signals, it is difficult to measure the output accurately without interfering the normal operation of the driver and the sampling process will cause

spikes in the output wave shape. As a result, the design will be more complicated and high-cost. As will be shown later, since the self-calibration process takes less than 50 μs , it can be easily inserted into normal driver operation as a calibration phase. For example, assuming the self-calibration is carried out once every 10 s, this introduces only 0.005 $\%$ time overhead.

The schematic of the self-calibration circuit is shown in Fig. 3. The inputs of the self-calibration circuits $in+$ and $in-$ connect to the transmitter driver outputs $out+$ and $out-$, respectively, while the outputs of the calibration circuit Q_0 to Q_3 connect to the binary switches of the transmitter driver. The basic idea is to first measure the output voltages, then, by adjusting the binary switches to increase or decrease the current source/sink value to make the output within a specified range around the desired range. In this design, the range is defined by two external reference voltages, V_{ref-} to V_{ref+} . The open loop gain of the comparator used in this prototype chip is 84 dB.

The switch-capacitor-based self-calibration circuit operates in two nonoverlapping phases. In phase I, switches S_{1a} , S_{1b} , and S_{1c} are closed and the comparators work as a unity gain buffer; C_3 is connected to the output point of the comparator to increase the phase margin and ensure the stability. The bias voltage V_{bias} is to bias the input voltages of the comparator into the common mode range. At the end of phase I, the offsets of the comparators are stored in the capacitors C_1 and C_2 : $V_{C1} = V_5 = V_{bias} + V_{offset}$ and $V_{C2} = V_{bias} - V_{(in-)}$. In phase II, C_3 is disconnected and the comparators function at higher speed. Since V_{ref+} and $in+$ are connected to C_1 and C_2 , respectively, in phase II, the stabilized voltages at the end of phase II are $V_5 = V_{ref+} + V_{C1} = V_{ref+} + V_{bias} + V_{offset}$, meanwhile, $V_6 = V_{(in+)} + V_{C2} = V_{(in+)} + V_{bias} - V_{(in-)}$. When $V_{(in+)} - V_{(in-)} > V_{ref+}$, the output V_1 is high; otherwise, it is low. The second branch of the switch-capacitor comparator works in exactly the same way except that the differential output compares to V_{ref-} instead of V_{ref+} . The switch close time S_{1a} is slightly earlier than S_{1b} , while S_{1b} is slightly earlier than S_{1c} . This is to reduce the correlation of these switches and minimize the clock feed through effect. Simulation shows it achieves 0.5-mV precision even if there is an offset as large as 50 mV present. This is about 0.1% accuracy compared with the 500-mV V_{od} specified in this design.

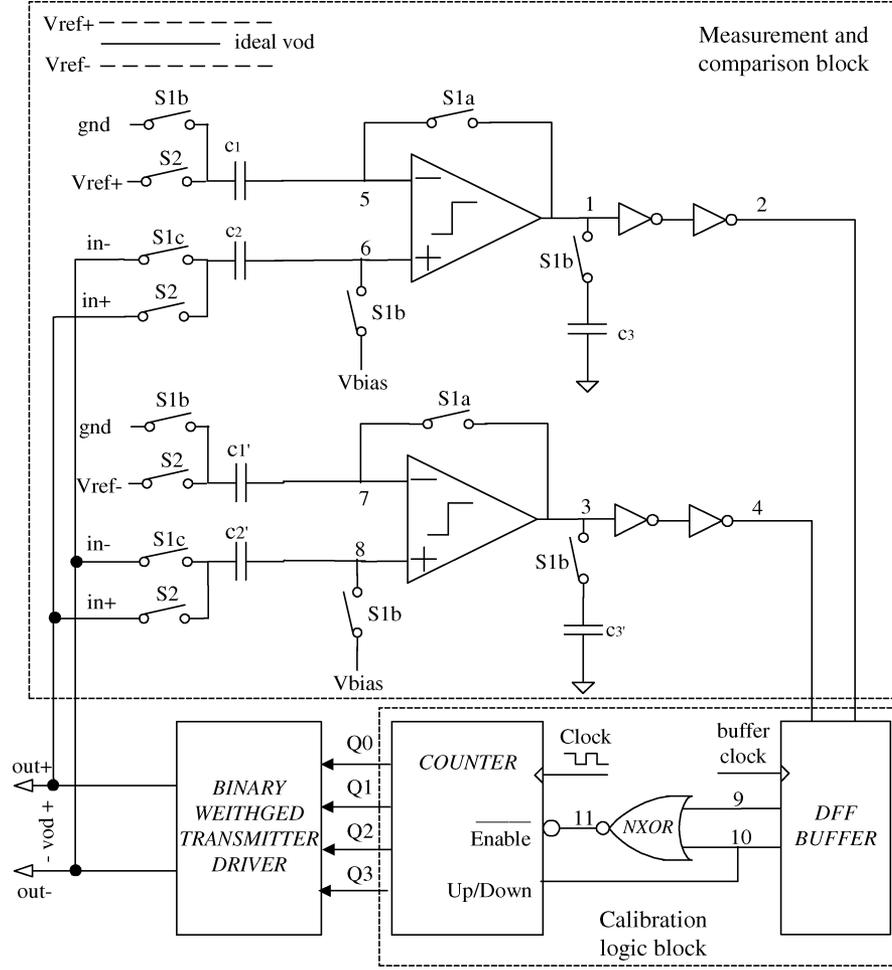


Fig. 3. On-chip self-calibration circuit.

 TABLE I
 COMPARISON RESULTS AND THE CORRESPONDING CALIBRATION ACTIONS
 FOR TWO REFERENCES

Condition	Vod vs. V_{ref+}	Vod vs. V_{ref-}	Calibration
1	Low	Low	Count up
2	High	High	Count down
3	Low	High	No action
4	High	Low	No action

As mentioned earlier, V_{ref+} , and V_{ref-} define the tolerant range around the desired differential voltage. This range is related to the size of the minimum adjustable ($1\times$) current source. The smaller the $1\times$ current source, the more accurate the current source is. The tunable range is limited by the number of the binary bits. In this design, the minimum current source is designed as 1% of the desired current and the range defined by V_{ref+} and V_{ref-} is designed to be slightly larger than 1% to ensure that the Vod can jump into this range. Smaller step size and more adjustable bits can further improve the calibration accuracy. The comparator outputs are connected to a NXOR gate to determine whether the measured output voltage is within the desired range. Then, a counter is used to count the digital control bits Q_x up or down according to the position of the output voltage relative to the reference voltages. The comparison results and the corresponding calibrations are listed in Table I.

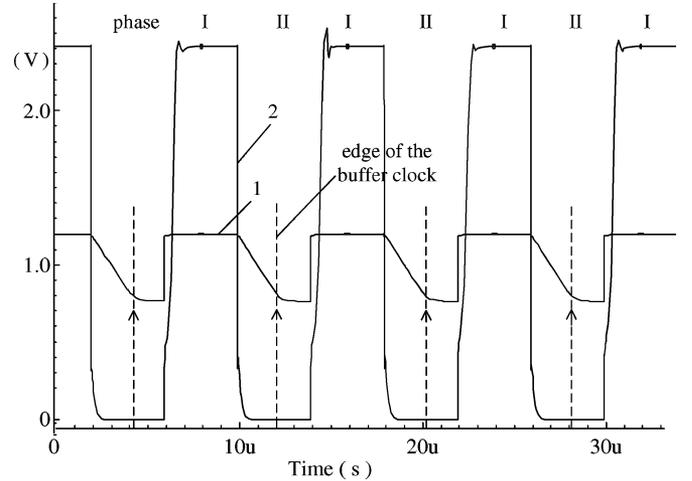

 Fig. 4. Comparator output when $V_{od} < V_{ref}$.

Fig. 4 shows a simulation waveform when $V_{(in+)} - V_{(in-)} < V_{ref}$ for points 1 and 2. In phase I, the V_1 becomes stable at $V_{bias} + V_{offset}$. In phase II, it either rises up or drops down according to the comparison result. Two serial connected inverters are used for two purposes: to speed up the output of the comparison, and to match the load of the two comparators. An additional clocked D-flip-flop buffer is used to pass the compar-

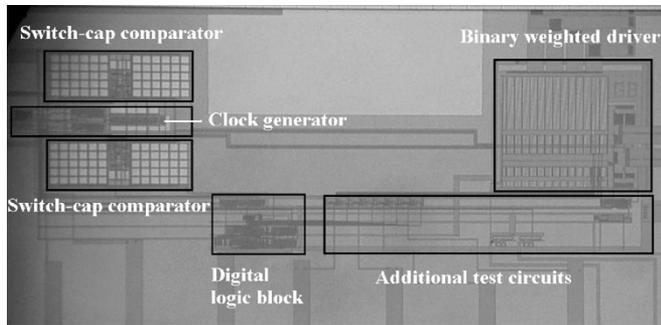


Fig. 5. Chip photograph.

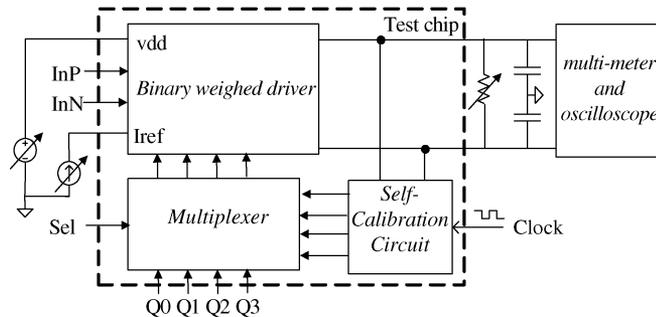


Fig. 6. Test setup.

ison results to the calibration logic block after the comparison results are stabilized at the middle of phase II. The counter is a synchronous binary counter with added clamping logic, so that it cannot jump from 1111 to 0000 when counting up or vice versa. The counting process stops after the output voltage reaches the desired range or when the counter reaches 1111 or 0000 even when the output voltage is not within the desired range.

Device matching is very important to achieve the desired accuracy. The most important points contributing to the calibration accuracy are points 5–8 in Fig. 3. Centroid matching layout was utilized for the large capacitors connected to these points. Also, it is desired to connect the measuring points between the driver output and the calibration circuit as closer as possible to the actual output bonding pads to avoid additional output voltage drop.

IV. TEST RESULTS

The design has been fabricated in TSMC 0.35- μm CMOS technology. The chip photograph is shown in Fig. 5. The die area of the driver with binary weighted current mirror is 92 400 μm^2 . The measurement and comparison circuits with the two-phase nonoverlapping clock generator circuits occupy 96 000 μm^2 die area; and the calibration logic block occupies 21 600 μm^2 of die area. Fig. 6 illustrates the test setup. The measured dc power consumption for the driver and the self-measurement and self-calibration circuits is totally 33.3 mW, including 31.8 mW consumed by the driver itself. The calibration time is maximally 50 μs for the counting up/down process of the 4-b current mirror control code. When the calibration is performed occasionally as proposed, the power consumption overhead is negligible.

Fig. 7 shows the typically measured output voltages levels out+ and out- and their common-mode voltage V_{com} . Since the supply voltage for the 0.35- μm process is 3.3 V, it is found

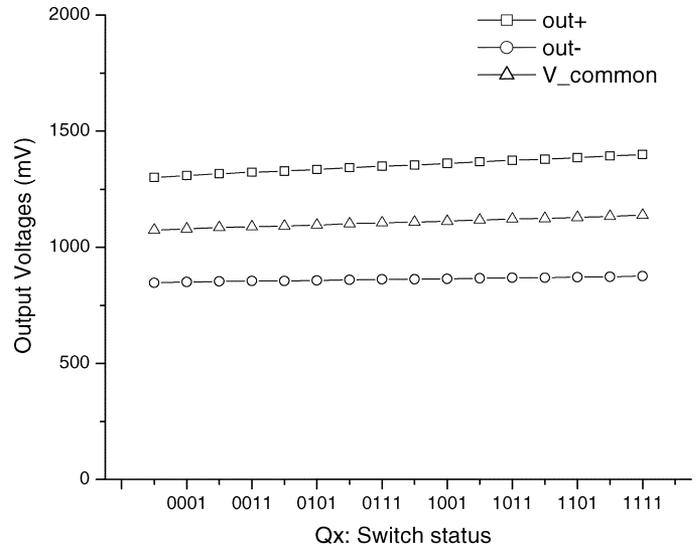


Fig. 7. Measured output and common-mode voltages for various switch statuses.

that the output common-mode level naturally settled around the 1.1–1.2-V range, based on the measurement results of about 40 randomly chosen chips from three fabrications. Fig. 8(a) presents the measured V_{od} values as a result of manually adjusting the binary control bits. Compared with the straight line, the linearity is good. To quantify the linearity, the absolute relative error between the measured V_{od} values and the straight line was calculated and presented in Fig. 8. It indicates that the mismatch of the binary weighted fingers only leads to maximum 0.11% relative errors. This guarantees the feasibility of the minimum 1% adjustable step.

The self-calibration circuit has been tested with the variations of current reference in the driver, the power supply voltage, the load resistance, and the process. A wide variation range, which exceeds the maximum tolerable range of the calibration circuit, has been used to test the robustness of the self-calibration scheme. Although a single factor variation in that large amount may not really happen, the total error in that range may actually occur when adding up all error contributor effects together in the worst case. Fig. 9 shows the measured output differential voltage with and without self-calibration when the current reference varies from 43 to 56 μA in 1- μA increments. The hollow dots are measured V_{od} without calibration, and the solid dots are measured V_{od} data points with self-calibration. The data points were collected from multiple chips, and they might overlap each other. In addition, each calibration can cause V_{od} to settle at one of the two possible values within the predefined ranges. Without calibration, the differential output voltage varies from -11% to $+8\%$ off the desired 500-mV value for -10% to $+6\%$ variations on input reference current of 50 μA . With self-calibration, the output voltage is within the $\pm 1\%$ range 500 mV for the same input reference current variation. Notice that, when the reference current is increased beyond 53 μA or decreased below 45 μA , the calibration circuit is no longer capable of calibrating the V_{od} within $\pm 1\%$ of the desired voltage. In this design, 4-b Q_x is used, which corresponds to an approximate maximum compensation range of $\pm 8\%$. More bits and/or larger calibration steps may be used if it is desired to compensate a wider

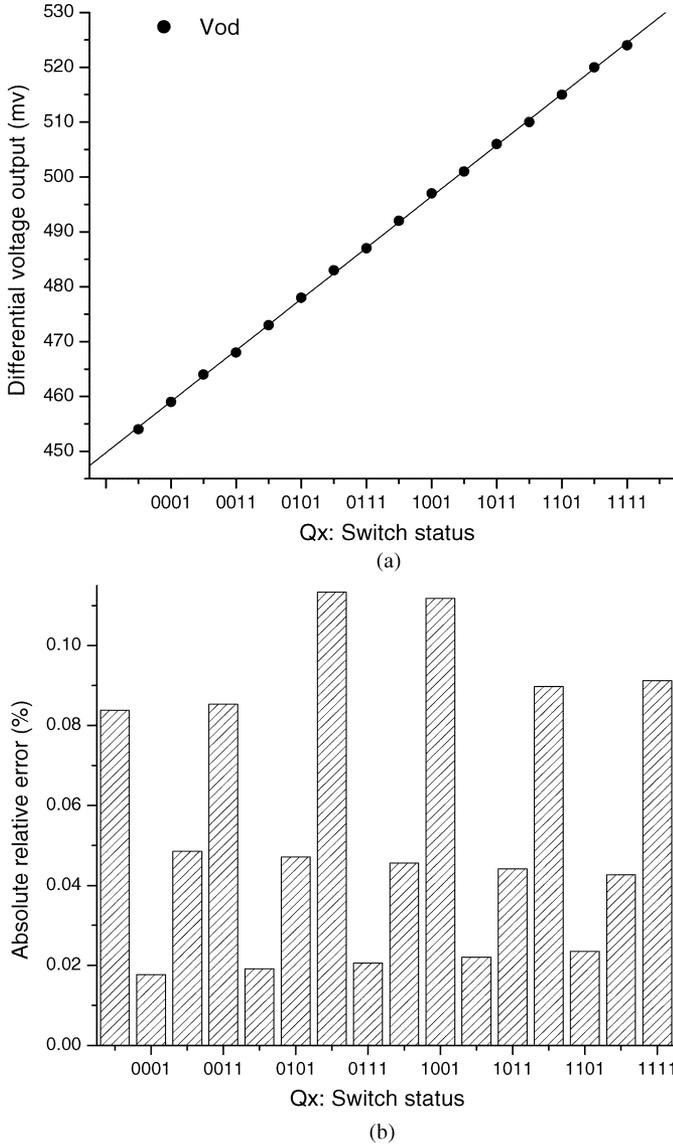


Fig. 8. (a) Measured differential output voltages (b) the absolute relative errors for different switch statuses.

parameter variation range. In the test, the power supply (3.3 V), the reference current, and the reference voltages, $V_{\text{ref}\pm}$, are provided off-chip. The external load is 100Ω , and the calibration clock is 300 kHz.

Figs. 10 and 11 present measured output voltage with and without calibration when varying the power supply voltage and when varying the external load resistance, respectively. With self-calibration, the output voltage is within the desired $\pm 1\%$ range for -39% to $+21\%$ variations on power supply voltage. Without calibration, the corresponding output voltage varies from -16% to $+5\%$. With self-calibration, the output voltage is within the desired $\pm 1\%$ range for -8% to $+5\%$ variations on the external load. Without calibration, the corresponding output voltage varies from -6% to $+10\%$.

Effects of process variation among ten test prototype chips are also characterized; a fixed power supply of 3.3 V, a current reference of $50 \mu\text{A}$, and load of 100Ω are used during this test. Measured data in Fig. 12 shows that there is about 2.5% systematic error and an additional $\pm 1.5\%$ random error due to process

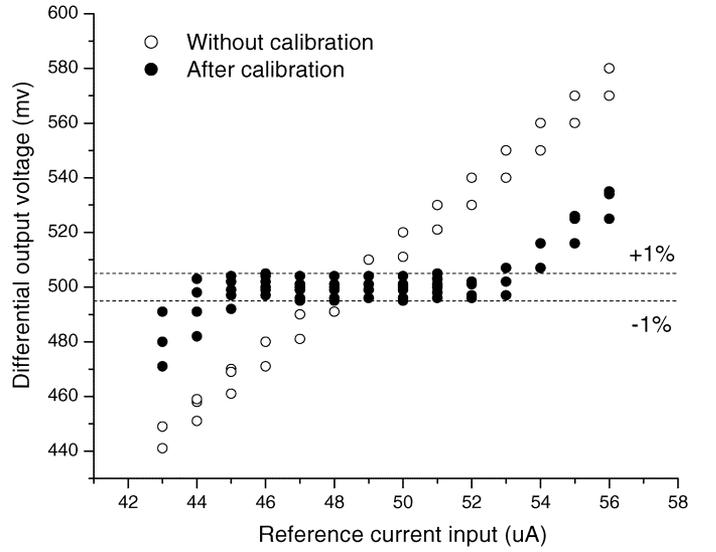


Fig. 9. Measured differential output voltage (V_{od}) with and without self-calibration over current reference variation.

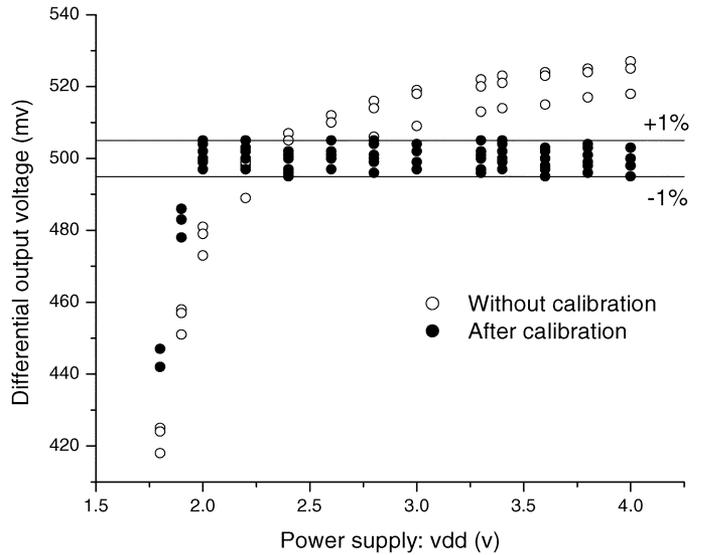


Fig. 10. Measured differential output voltage (V_{od}) with and without self-calibration over power supply variation.

variation. In this test, the power supply, the reference, and the load are all ideal and the temperature is fixed. After self-calibration, the residue errors of all chips are reduced to the desired $\pm 1\%$ range.

Since the power supply, the reference current, and the load are provided externally in the demo chip, testing of the temperature effect is carried out by heating the chip only. The result shows a very small, about 0.01% per $^{\circ}\text{C}$ output shift. That is too small to trigger the calibration since it is still within $\pm 1\%$ accuracy. In reality, the temperature may affect the output indirectly by varying the load, the references and the power supplies.

In this design, the reference voltages $V_{\text{ref}\pm}$ have been provided externally for the convenient characterization of the self-calibration circuits; this can be realized by an on-chip bandgap reference eventually. Two reference voltages, $V_{\text{ref}\pm}$ are used to obtain up/down operation, which is easy to be inserted as a fast calibration phase into normal transmitter operation. However,

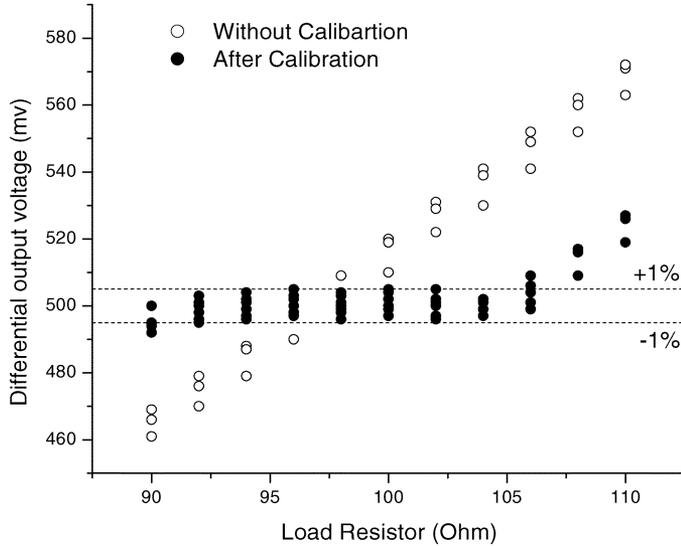


Fig. 11. Measured differential output voltage (V_{od}) with and without self-calibration over load resistance variation.

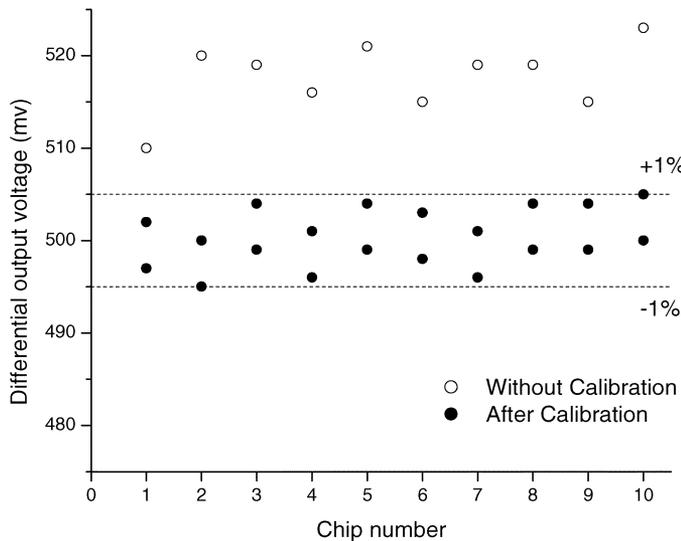


Fig. 12. Measured differential output voltage (V_{od}) with and without self-calibration over process variation.

TABLE II
COMPARISON RESULTS AND THE CORRESPONDING CALIBRATION ACTIONS FOR A SINGLE REFERENCE

Condition	V_{od} vs. V_{ref}	Action
1	Low	Count up
2	High	Count down

a single voltage reference is generally preferred over two references for design simplicity. In that case, one may use only one set of the comparator branches, and this reduces the die area. In the test chip, this has been done by connecting the V_{ref+} and V_{ref-} together as V_{ref} , and the calibration can be done according to Table II. While two references define a range that the output voltage can settle into; when only one reference is provided, the output will move up and down the desired value

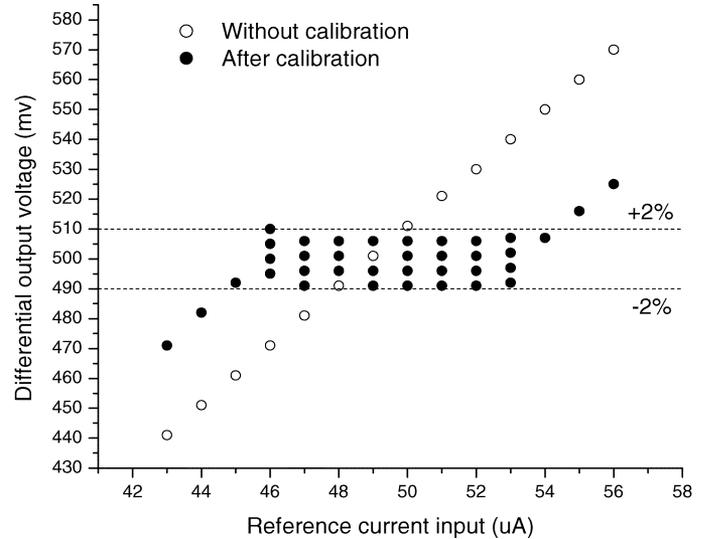


Fig. 13. Test results using a single V_{ref} .

and never settle. Since the proposed calibration scheme is performed when the driver is not transmitting signals, this is acceptable. After the calibration period ends and system goes back to the transmitting mode, the output will stay at one of the several consecutive values. Fig. 13 presents the test result in this condition: the output accuracy decreases to $\pm 2\%$. Adding up with the voltage reference error and temporal noise, it can still achieve $\pm 5\%$ over a 200°C operating temperature range. This can be very hard to obtain if there is no self-calibration presented, since the power supply, current reference, and load resistance can all vary and all the errors can be added up together. Especially for battery-powered or low-cost customer devices, the variations of power supply, load, and current reference are even larger and lead to additional errors.

As a brief summary, the tolerable variation range of the self-calibrated driver are I_{ref} from -10% to $+6\%$, V_{dd} from -39% to $+21\%$, and R_{load} from -8% to $+5\%$. Compared with the functional range provided in Section II, the I_{ref} and R_{load} tolerable ranges are much narrower than the functional range of the mirror. So, the saturation of the mirror is not the limiting fact here. However, the V_{DD} has the same range as the saturation of the mirror. This shows that the voltage supply is the limiting parameter; beyond the tolerable range of V_{DD} , the current mirrors are out of saturation.

V. CONCLUSION

This paper has presented on-chip self-measurement and self-calibration circuits to tune the binary weighted current mirror for low voltage differential driver. With the proposed method, high accuracy can be achieved without using expensive trimming methods or using high voltage charge pump units. In addition, the proposed circuits can dynamically calibrate upon the collective errors from various sources due to process, power supply, and temperature variations. As a result, it reduces the requirement on the current mirrors, the reference current, the supply voltage, and the load resistor while achieving high accuracy. This effectively improves the product yield and lowers down the cost. Measurement results show that the differential

output voltage can be self-calibrated to $\pm 1\%$ accuracy with 16% reference current variation, 60% power supply variation, 13% load variation, and multichip, multifabrication CMOS process variations, respectively.

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