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# Defects in Silicon Crystals and Their Impact on DRAM Device Characteristics

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Polished p-wafers from vacancy-rich silicon crystals are used as substrates for many device applications and, in particular, for memory devices. Octahedral vacancy aggregates, the so-called crystal originated pits, are found in these wafers with sizes of 150 nm and densities of $10^6$ $cm^{-3}$. To meet the design rule requirements of 0.13 μm and below, a reduction of defect size and density is required. The approaches to achieve silicon with nearly no intrinsic point defect aggregates are the growth of so-called perfect crystals, the growth of nitrogen-doped crystals with very fast cooling rates and subsequent high temperature wafer annealing, and epitaxy of wafers. In addition, new concepts like wafers with a thin refinement layer grown on a cost and bulk optimized substrate (so-called fLASH! wafers) will allow further cost reduction.
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Design rules of 0.13 μm and below require further improvement of the crystal originated grown-in defect level within the device active area. This corresponds to the region from the wafer surface to a depth of approximately 10 μm for deep trench capacitor dynamic random access memory (DRAM) technology. A defect-free depth of about 1 μm is sufficient for many other device technologies such as the stacked DRAM technology.[1] Defects do not deteriorate device performance if they are deeper in the bulk and do not interfere with the device active region. On the contrary, bulk microdefects (BMD) of about $10^9$ $cm^{-3}$ are usually required for internal gettering of metallic impurities[2] as well as for sufficient mechanical wafer stability during high temperature processing.

Today, crystal originated pits (COPs), which are octahedral void-like vacancy aggregates of typically 150 nm size[3,4] are the prevailing grown-in defects in Czochralski (CZ) grown silicon single crystals. However, as the design rule approaches the size of the grown-in defects, device yield deterioration is encountered due to, *e.g.*, gate oxide failure, high leakage current, lack of device reliability, and trench to trench shorts. Hence, bulk quality demands will change to so-called grown-in defect-free wafers.

Four different approaches are currently known to achieve silicon with nearly no intrinsic point defect aggregates.[5] The first is the growth of silicon crystals in a regime where Si interstitials and vacancies are incorporated in equal concentrations resulting in complete mutual annihilation of point defects (so-called perfect silicon).[6] The second approach is the growth of crystals with extremely small COPs by applying nitrogen doping and very fast pull rates and high cooling rates. Subsequent high temperature wafer annealing can easily dissolve the small COPs. A further alternative is the well-known epitaxial wafer, which is in use in device manufacturing since many years. A fourth approach is the so-called fLASH! wafer,[7] which is based on a thin refinement layer (fLASH! process) on a low-cost substrate with very small defects.

In particular, the changeover to 300 mm will make the epi wafer significantly more attractive as the relative price increase of an epi wafer as compared to a polished wafer becomes rather small. In this paper, we discuss grown-in defects in silicon wafers, their impact on DRAM device characteristics, and methods to improve the crystal quality.

## Grown-in Defects in Silicon Crystals

Grown-in defect formation in silicon crystals is dominated by the aggregation of vacancies and self-interstitials. Depending on the crystal pulling conditions, one of the two species prevails. This can be schematically explained by an axially cut crystal, which was grown with a pull rate decrease from top to bottom (Fig. 1). At the top of the crystal, the pull rate was high and only vacancy-type defects, the so-called D defects or COPs, appear. When reducing the pulling rate, the vacancy-rich region shrinks and interstitial-type defects are formed near the edges. These are networks of dislocation loops that can be revealed by etching as large pits (L-pits) of 20 μm size.[8] Wafers with L-pits are detrimental for devices, because of their large size. A high density of oxidation induced stacking faults (OSF) can be observed at the boundary between vacancy and interstitial regions after wet oxidation at 1100°C.

According to Voronkov's theory,[9,10] the boundary between vacancy and interstitial excess is found, where the ratio of the pull rate ($V$) and the temperature gradient ($G$) at the solidification interface

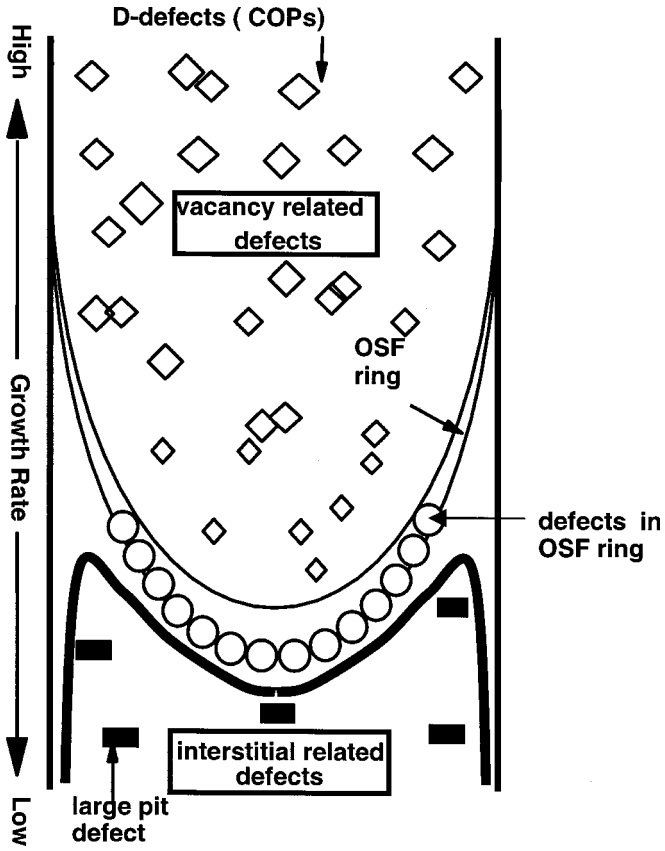


**Figure 1.** Grown-in defects in a silicon crystal, grown with a varying pulling rate.

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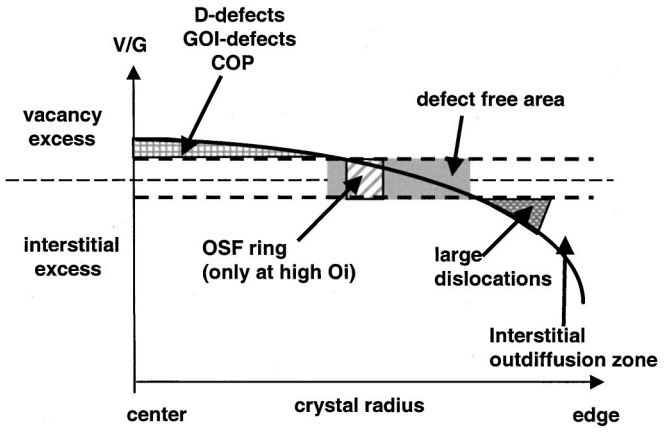


**Figure 2.** Radial variation of $V/G$ in CZ silicon crystals grown with a transition from vacancy-rich to interstitial-rich from center to rim.

$V/G$ is equal to a critical value, $C_{crit}$, of $1.4 \times 10^{-3}$ cm$^2$/K min[11] (Fig. 2). Crystals become fully interstitial-rich at low pull rates, where $C_{crit}$ is lower than $1.4 \times 10^{-3}$ cm$^2$/K min over the complete radius. In a relatively narrow window of approximately $\pm$ 10% of the critical $V/G$ value, neither vacancy nor interstitial reach the critical supersaturation for the nucleation of larger defects.

Today, prime polished wafers are predominantly made from vacancy-rich crystals with typical COP sizes of 150 nm and densities of $10^6$ cm$^{-3}$.[12] As shown later, it is feasible to optimize COP distributions for specific device applications by adjusting the crystal pulling process.

## Simulation of COPs

Defect engineering has become a combination of experimental and simulation work in recent years. Physical models have been developed to predict the densities and sizes of grown-in defects. Hence, simulation has become a viable tool for supporting the crystal pulling process development. Grown-in void formation in silicon crystals was simulated by combining three numerical models for the prediction of the thermal history, the point defect distribution and the agglomeration of vacancies. The models have been described in detail elsewhere;[13-15] therefore, we summarize in brief the important features only.

*Thermal simulation*.—Crystal temperatures were computed by using the finite element code FEMAG developed by Dupret *et al.*[13] Based on the assumption of an axially symmetric furnace geometry, the heat transfer between all furnace parts is taken into account. The code solves the transport equations for the heat conduction in the solid parts (*e.g.*, crystal, heater, and insulation) and for the diffuse radiation in the furnace enclosures. The convective heat transport in the melt is approximated by introducing an enhanced equivalent thermal conductivity, which has a convective and a conductive contribution. A comparison of simulated temperatures in the crystal with experimental data showed good agreement.[16]

*Point defect simulation*.—In previous numerical and experimental studies, we have observed that point defect dynamics and vacancy agglomeration can be decoupled from each other.[17] Since recombination of vacancies and self-interstitials occurs very rapidly near the solid/liquid interface, one of the point defect species becomes almost completely depleted at a temperature of 1200°C during cooling of the crystal. Hence, the concentration of the surviving species remains at a constant level during further cooling. At the onset of vacancy agglomeration in vacancy-rich crystals, the vacancy concentration has already stabilized and the self-interstitial concentration is reduced by orders of magnitude. This allows us to separately compute the thermal history of the crystal, the point defect dynamics, and the vacancy aggregation. A single set of thermophysical parameters is used for all simulations.[17]

On the basis of computed temperature distributions, simulations of vacancy and self-interstitial concentrations in the growing crystals were performed. Convection, diffusion, and recombination of the intrinsic point defects are considered before the onset of agglomeration. In the calculations, the vacancy and self-interstitial diffusivities and equilibrium concentrations have been taken from Sinno *et al.*[14] Equilibrium concentration of vacancies and self-interstitials at the solid/liquid interface, the crystal top and sidewall as boundary conditions.

*Simulation of void formation*.—We simulated the formation of grown-in voids with a vacancy cluster model[15] by using computed temperature and point defect distributions as input. Our approach assumes a zero dimensional case. This implies that we consider the crystal/void system as a closed system. Voids in the bulk of the crystal are not influenced by the boundary conditions at the domain boundaries from where vacancies could be supplied by diffusion. This assumption is justified, because clustering occurs at a relatively large distance from the solid/liquid interface and the vacancy concentration is influenced only in the vicinity of the lateral crystal surface (about 5 to 10 mm) by the boundary conditions.

Material points in the crystal are cooled down from melting to room temperature in time steps of 5 s. The time evolution of defect formation is directly linked to the axial cooling profile. Hence, an axial position in the crystal can be represented by the local thermal history. Voids are assumed to be of spherical shape and immobile in the lattice. Vacancy clusters of size $n$, can grow to size $(n + 1)$ by incorporating one vacancy or shrink to size $(n - 1)$ by emitting one vacancy. Agglomeration kinetics are modeled by deriving rate equations for the evolution of the void density. Discrete equations are developed for small clusters composed of less than 20 vacancies. Rate equations for larger voids are expanded into a single Fokker-Planck equation.

Growth and dissolution rates of vacancy clusters are functions of the Gibbs' free energy of the void/silicon crystal system. The Gibbs' free energy of a void in the silicon lattice can be expressed as the sum of volumetric and interfacial free energies. The interface energy density $\sigma$ is considered to be identical with the value for the {111} surface energy density of silicon, as the void planes are oriented in ⟨111⟩ direction. A surface energy density of 1.0 J/m$^2$ is used in the present simulations, which is in the range of published experimental data.[18]

*Results*.—Growth furnaces were designed for three different 200 mm lowly boron-doped p-crystals with slow (CZ1), medium (CZ2), and fast (CZ3) cooling rates. This was achieved by tuning the heat insulation efficiency of heat shields surrounding the growing crystal. The predicted crystal cooling curves and the pulling rate were used as input for the point defect simulation. All three crystals were grown in the vacancy-rich regime. Vacancy concentrations reduced from solidification temperature to 1200°C, where they reached a constant level of about $10^{14}$ cm$^{-3}$ (Fig. 3). Self-interstitials become depleted by recombination with vacancies.

By using the above described void simulator it was found that vacancies become supersaturated during cooling at 1100°C and start to nucleate octahedral voids. Nearly Gaussian-like void distributions are obtained with mean sizes of 160 nm for crystal CZ1, 125 nm for crystal CZ2, and 75 nm for crystal CZ3 (Fig. 4). Experimental data from COP and atomic force microscope measurements are very well in agreement with the simulation results. The impact of COPs on device performance is discussed in the next section.

## Impact of COPs on Yield and Reliability of ULSI Circuits

COP size did not seriously impact integrated circuit yield and reliability in the past. Active silicon device areas, which are defined by the design rules, were well above the average COP size. Moreover, the device integration density was sufficiently small compared

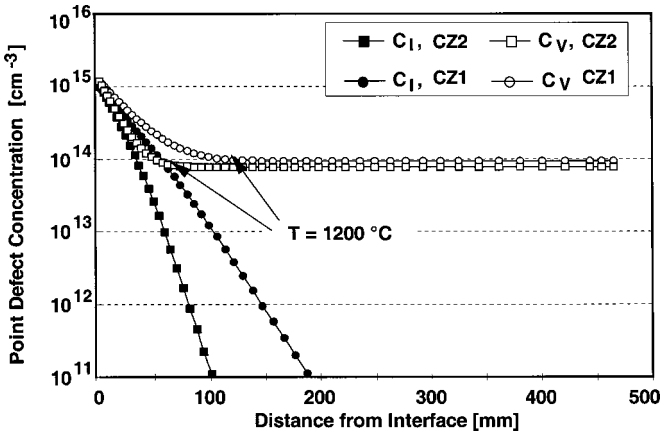


**Figure 3.** Vacancy ($C_V$) and self-interstitial ($C_I$) concentrations in growing CZ silicon crystals (CZ1 and CZ2) as a function of distance from the solidification interface.

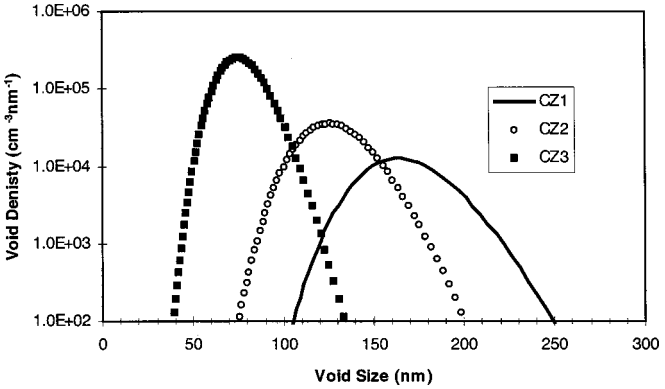


**Figure 4.** COP distributions in slowly (CZ1), medium (CZ2), and fast (CZ3) cooled 200 mm crystals.

to the COP density in the deep near-surface region of approximately 200 nm. The only exception has been the impact of COPs on the gate oxide integrity (GOI), in particular for oxide thicknesses above 10 nm.[19] Fortunately, thinner gate oxides (<5 nm) were found to be rather insensitive to COPs.[20] Hence, GOI degradation currently does not appear to be a major problem for smaller design rules, if the average COP size would remain constant.

The situation is changing now, because active device areas for actual design rules of 170 nm already correspond to typical COP sizes. They will become even smaller than the COP size in the near future, resulting in increased short fails, cross section throttle, or reliability degradation fail events of active devices per unit area. Increasing density, complexity, and chip area of advanced ultralarge scale integrated circuits enhance the absolute fail number per chip in parallel. Furthermore, yield and reliability detraction is mainly caused by the GOI degradation mechanism of the millions of MOS field effect transistors. DRAMs with deep trench cell structure, in contrast to stacked capacitor cell-based DRAMs, show additional COP impact mechanisms: a storage dielectric integrity (SDI) mechanism at the storage trench interface (SDI integrity, analogous to the GOI mechanism of planar metal oxide semiconductor transistors), short fails between neighbored deep storage trenches, and a vertical GOI (VGOI) mechanism of vertical transistors will arise, if they are introduced in future DRAMs.

Fortunately the impact of the SDI mechanism on yield and reliability of the recent deep trench cell based DRAM generations is rather low, because of the defect insensitivity of the nitride-oxide

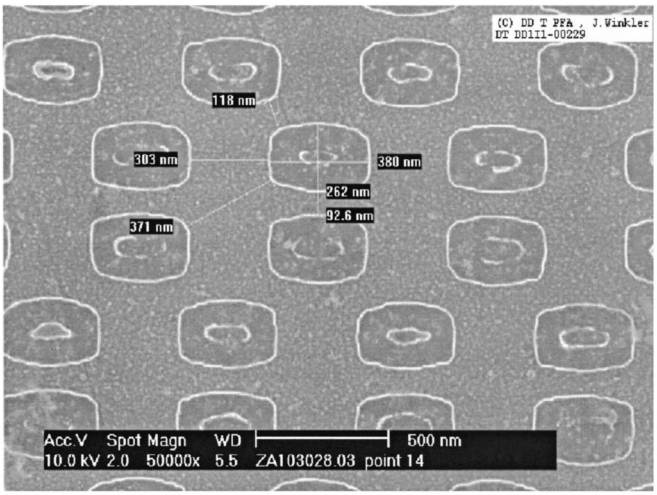


**Figure 5.** SEM of the asymmetric storage trench pattern of an actual trench cell-based DRAM product, where COP short fails mainly arise between the most adjacent deep trench pairs, having minimum distances down to 92 nm.

(NO) stack of about 4.5 nm oxide equivalent thickness, applied as the storage dielectric of the industrially fabricated trench cells so far. Storage dielectric films with a higher dielectric constant, which will be introduced into future trench cell-based DRAMs, have to stay at a comparable low SDI defect density.

A short between neighbored deep trenches arises, if a COP randomly is cut by at least two adjacent trenches during the trench reactive ion etch processing (Fig. 5). The cut COPs inner surface is coated with storage dielectric and node electrode films (the last is usually highly doped polysilicon), during the following steps of the deep trench processing (Fig. 6). The probability of such a short fail event strongly depends on the deep trench array geometry, *i.e.*, its

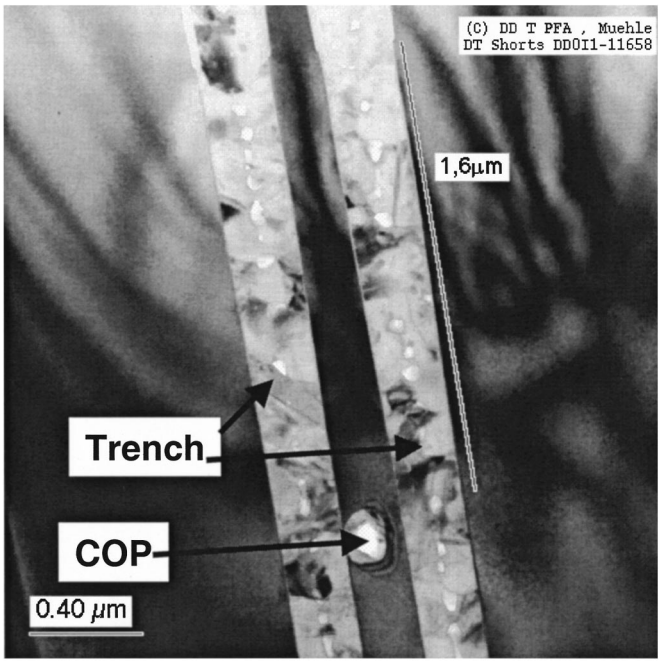


**Figure 6.** Scanning electron microscope (SEM) image of a COP short fail between adjacent deep trenches of an actual fabricated DRAM product, clearly showing the storage dielectric and poly electrode fill and the empty space in the COP center. Trenches are located above and below the photograph level.

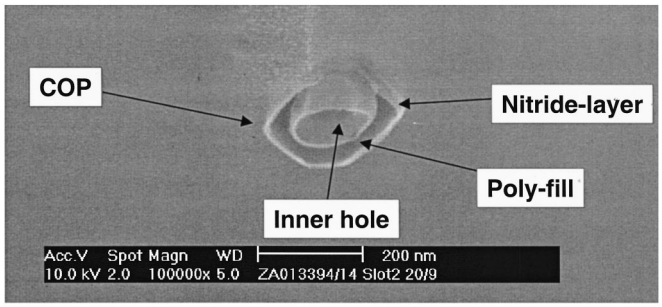


**Figure 7.** Transmission electron microscopy (TEM) image of a COP short between adjacent deep trenches of an actual fabricated DRAM product. The cut with the right trench is located outside the TEM sample cross section shown.

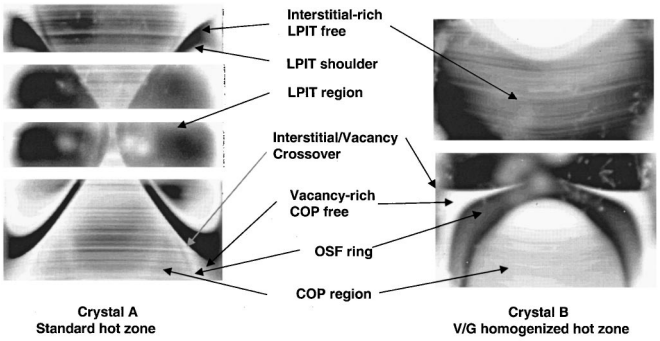


**Figure 8.** Defect distributions (after heat-treatment and etching) in crystals A and B grown with pull rate ramps in a standard and in a *G* homogenized hot zone, respectively.

layout pattern, defining the distances to the next neighbored trenches and their depth and steepness. Short fails mainly arise from the zones between each nearest neighbored deep trench pair (Fig. 7), due to the asymmetry of the deep trench pattern of actually fabricated trench cell-based DRAM products and the fact that the average COP size of the standard silicon substrate material does not exceed the minimum trench-trench distance too much. Analyses of this special COP short fail type on recent trench cell DRAM products with $\geqslant 7$ μm trench depth show an average short fail number of $<4$ per 64 M array block, which is small compared to other fail types. COP shorts as well as other fails are electrically eliminated by the redundancy repair technique.

Nevertheless, Si wafers with a near surface defect-free zone of up to 10 μm in depth will most likely be required for future logic (embedded DRAM) as well as for memory devices. COPs are also highly undesirable for particle monitoring wafers, used for tool and line monitoring, as they show up as localized light scattering (LLS) defects on the wafer surface and, therefore, obscure the detection of particles. Alternatives to vacancy-rich wafers are presented in the next section.

## Approaches to Improved Materials

Several approaches are known to achieve silicon with nearly no intrinsic point defect aggregates: (*i*) perfect silicon crystals, (*ii*) fast pulled and cooled, nitrogen-doped crystals with subsequent high temperature anneal, (*iii*) epitaxial wafers, and (*iv*) the so-called fLASH! wafers, which are discussed (briefly) in the following paragraphs.

*Perfect silicon crystals*.—In the so-called perfect crystal approach, crystals are grown without defects larger than approximately 10 nm. Neither vacancy nor interstitial type defects can be measured in the as-grown crystal. Only grown-in oxide precipitates of several nm can be delineated after additional thermal treatments. The growth of perfect silicon crystals occurs in a regime where Si interstitials and vacancies are incorporated in almost equal concentrations.[6,21] Both species quickly recombine close to the solidification interface, forming a nearly perfect crystal structure. Hence, neither vacancy nor interstitial concentrations can reach a supersaturation, which is sufficiently high to nucleate larger defects.

One approach to producing perfect crystals is the homogenization of $V/G$ which is illustrated in Fig. 8, where standard and $V/G$ homogenized crystals are compared with each other. Conditions for perfect silicon are achieved if the radial variation of $V/G$[22] is less than approximately $\pm 10\%$ of the critical $V/G$ value (Fig. 2), which is very demanding as $G$ usually decreases strongly from the center to the rim of the crystal.[23] Perfect crystals are grown if interstitials and vacancies are incorporated at almost equal concentrations at the solid/liquid interface. This leads to final concentrations of approximately $1 \times 10^{13}$ cm$^{-3}$ and less for both species after recombination has terminated. Hence, no L-pit and COP defects can form during further cooling.

Based on numerical simulation, a standard hot zone has been redesigned in order to increase the radial homogeneity of $G$ by optimizing a heat shield surrounding the growing crystal. Crystal A was grown in the standard hot zone with a pull rate of 1.0 mm/min. After a length of about 200 mm has been reached, the pull rate was linearly ramped down to 0.5 mm/min, and, subsequently, it was ramped up to 1.0 mm/min again. Up and down ramp occurred over a length of about 100 mm. Similar pull rate ramps were applied for the $G$ homogenized crystal B. However, the maximum and minimum pull rates were 0.6 and 0.3 mm/min, respectively. Both crystals were grown with a diam of 200 mm and boron doping levels of 10 Ω cm. Defect distributions were observed for axial cuts of the crystals after heat-treatment and etching (Fig. 8). It should be noted that the intensity of the colors in Fig. 8 is not only correlated with a particular defect region but also with the actual oxygen content of the crystal, *e.g.*, the OSF ring region looks bright for the top part and darker for the bottom part of crystal B.

Both crystals show vacancy-rich areas at high pull rates in the center part, where COPs are observed after SC1 cleaning. Next to the COP region is the OSF ring region, an area with excess vacancies but without COP defects, the vacancy/interstitial cross over, and an interstitial-rich region without L-pits. L-pit shoulders, and L-pit regions occur only in the standard crystal A at lower pull rates. A perfect silicon region without L-pits and COPs is found in the $G$ homogenized crystal B.

It is questionable whether perfect silicon crystals can become a mainstream product, as they face several drawbacks. Significantly lower pull rates and a very tight control of crystal growth parameters are required for growing perfect crystals, resulting in considerably lower throughputs and higher cost. Moreover, transient effects from shouldering unavoidably cause a material loss of 100 to 200 mm at the seed end part before the defect-free regime is reached. Additional yield excursions occur if the pull rate is not perfectly kept at the set point value within very small limits. Furthermore, the growth of perfect crystals is negatively affected by thermal drift of the hot zone, that unavoidably occurs due to gradual aging of graphite parts and graphite felt insulations. Growing of completely defect-free 300 mm crystals is an even more difficult undertaking as pulling speed and usable portion of the crystal further reduce. It can be assumed that the dislocation-free yield will decrease even more due to the extended process times, which increase the probability for creating first dislocations.

A further method to pull grown-in defect-free crystals is the *in situ* out-diffusion of interstitials.[24,25] In this case, crystals are pulled under interstitial-rich conditions and maintained at high temperatures for extended times. This method makes use of the very high migration speed of interstitials, which diffuse from the inner parts of the crystal to the rim, where they become surface lattice atoms.

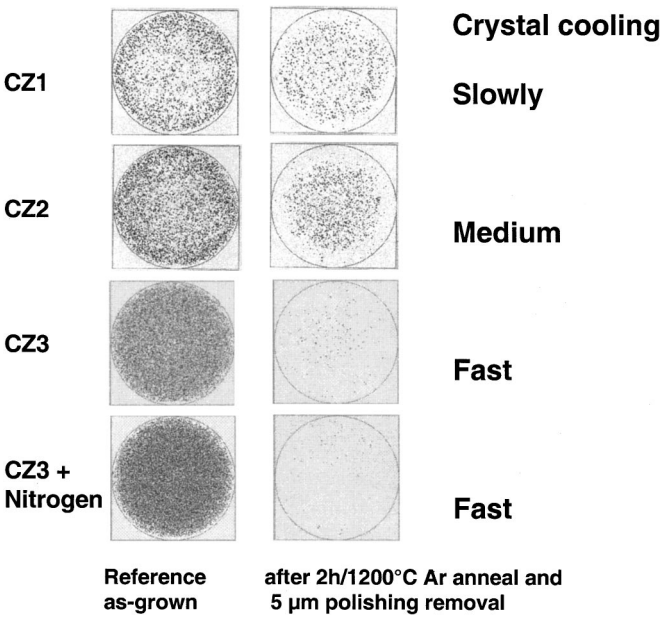


**Figure 9.** COPs on as-grown and annealed polished wafers from CZ1, CZ2, CZ3, and nitrogen-doped CZ3 crystals.

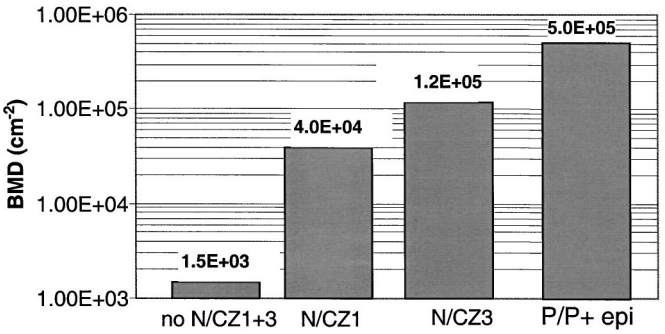


**Figure 10.** BMD densities after process simulation of wafers from non-nitrogen and nitrogen doped CZ1 and CZ3 crystals and of $p/p^+$ wafers.

However, extended cooling times of more than 30 h are required from melting point to 1050°C for 200 mm crystals. This results in very low pulling rates, long process times, and very complex furnace design. It is therefore very questionable whether this method can be applied at all for 300 mm crystals.

An additional drawback for grown-in defect-free crystals is the lack of internal gettering capability.[26] BMD nuclei cannot form during growth, as grown-in defect-free crystals are grown in the regime, where vacancies are not available for oxide precipitate growth. Hence, additional process steps such as pre-annealing are required.

In general, it cannot be expected that perfect crystals can become a mainstream product as the production cost and investment expenses for pulling facilities will be considerably higher as compared to the production of standard crystals.

*Annealing of COPs*.—Another approach to improving the bulk quality is the reduction of COP size from 150 to about 70 nm (see Fig. 4) and subsequent high temperature annealing. Wafers from crystals with small COPs become completely defect free in the surface and near surface regions after high temperature treatment at 1200°C in an argon or hydrogen atmosphere for typically 1-2 h.[27,28] However, starting materials have to be tuned for the annealing step as shown in the following examples. Wafers with large grown-in defects such as CZ1 or CZ2 material (Fig. 4) do not become completely defect free in a depth of 5 μm even after 2 h of annealing at 1200°C in an argon ambient, although the starting defect density of the substrate wafer has been low (Fig. 9). Fast cooled crystals (CZ3) with small defects become almost defect free after annealing in the surface and near surface regions. COP sizes are further reduced if the crystals are nitrogen doped.[29,30] These very small COPs of about 50 nm size completely disappear after 1200°C annealing (Fig. 9).

Nitrogen doping could become indispensable for the annealing of 300 mm crystals are more slowly grown and cooled than 200 mm crystals, because the heat losses from 300 mm crystals are smaller due the higher volume-to-surface ratio. Therefore, grown-in voids are unavoidably larger as compared with grown-in voids of smaller diameter wafers. Moreover, thermal stress in the crystal has to be kept at a level where breakage cannot occur. On the other hand, high temperature treatments of 300 mm wafers are rather risky with regard to the generation of slippage. Annealed wafers appear to be the more promising alternative as compared to perfect silicon. Although, the annealing step adds cost, the throughput and cost optimized crystal growth process overcompensates the disadvantages of the production of perfect crystals. Device manufacturers may even eliminate process steps, *e.g.*, denuded zone formation.

*Epitaxial wafer*.—As both of the above approaches show severe drawbacks especially for 300 mm wafers, most device manufacturers are favoring epitaxial wafers. Moreover, the production cost per square centimeter drops for epi layers from single wafer reactors with increasing wafer diameter, and, hence, is expected to reach a level for 300 mm wafers that is attractive for DRAM manufacturers as well. Epi wafers have built in several advantages for device manufacturing with respect to quality, because substrate wafer and epi layer can be independently optimized.

*Substrate*.—In case of highly boron-doped substrates, internal gettering capabilities are excellent, as BMD levels reach values of approximately $5 \times 10^5$ cm$^{-2}$ (Fig. 10). Also, latch up and electrostatic discharge problems are not encountered. For lowly boron-doped substrates, the grown-in void distributions and the BMD density can be tuned. In particular, fast pulled and fast cooled crystals show a very high density of small defects (see Fig. 4), which can be perfectly covered by the epi layer very easily.

With regard to the gettering capability of epi pp-wafers, it was found that sufficient BMDs are available, if the oxygen content of the substrate is well above $7 \times 10^{17}$ atom/cm$^3$. At lower oxygen concentrations, nitrogen doping is necessary to generate sufficient oxygen precipitation. However, in this case, the cooling rate of the growing crystal must be fast enough to keep the grown-in precipitate size below a critical value to avoid defects in the epi layer.

*Layer*.—Epi layer thickness is typically in the range of 3 to 5 μm for CMOS applications. In this case, the layer is sufficiently thick to cover all grown-in defects, and, hence, perfect and defect-free surface and subsurface layers can be achieved. The main drawback of this solution is the additional epitaxial process step, which significantly increases the wafer cost.

*The fLASH! concept*[7].—A new, cost optimized approach is the so-called fLASH! wafer, where only a thin layer of about 0.5 μm is deposited during a throughput optimized process. Standard wafers with large grown-in defects of 150 nm would not be suitable as substrates. COPs would not be fully covered by the layer and would appear as shallow postepitaxial surface pits which can be observed as localized light scatters (LLS $>$ 0.085 μm latex sphere equivalent) on the surface. Therefore, bulk optimized wafers from nitrogen-doped, fast pulled, and fast cooled crystals with a high density of small defects have to be used. As shown in Fig. 11, the gate oxide integrity (GOI) yield of fLASH! wafers is comparable with epi wafers and much better than GOI yields of polished wafers.

Moreover, fLASH! wafers from fast grown nitrogen-doped crystals exhibit sufficient gettering capabilities, as the BMD density is $1.2 \times 10^5$ cm$^{-2}$ after a 0.18 μm design rule process simulation

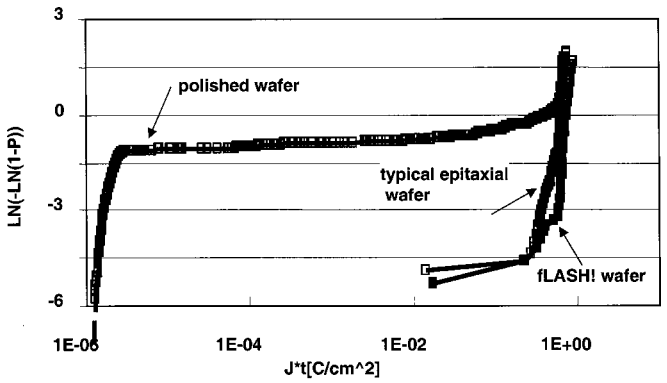


**Figure 11.** GOI performance of typical polished, epi wafers, and of fLASH! wafers.

(Fig. 10). In particular, they are superior to medium fast grown and non-nitrogen-doped substrates, and they reach almost the level of $pp^+$ epi wafers (*ca.* $5 \times 10^5$ $cm^{-2}$). The oxygen precipitate free zone after above process simulation is *ca.* 10 μm and, thus, large enough for nearly all device processes. However, the COP free zone is very small and, actually, extends over the refinement layer, only. The cycle time is too short for COP dissolution in the substrate. As a consequence, fLASH! wafers are not likely to be suitable for device technologies, which use deep trench capacitors.

## Conclusions

Octahedral voids, the so-called COPs of typical 150 nm size and $10^6$ $cm^{-3}$ density are becoming detrimental for devices of 0.13 μm and below design rules. The approaches to achieve silicon with nearly no intrinsic point defect aggregates are the growth of perfect crystals without grown-in defects, the growth of nitrogen-doped crystals with very fast pull rates/high cooling rates, and subsequent high temperature wafer annealing, and epitaxy of wafers. New concepts like the fast growth of thin layers (fLASH! process) on low-cost wafer substrates with very small defects will allow a further substantial cost reduction. In particular, epi and fLASH! wafers will become a very attractive alternative for many device applications on 300 mm wafers. They provide a defect-free surface and near surface region. Moreover, sufficiently high BMD densities in the bulk for internal gettering are formed if fast cooled, nitrogen-doped crystals are used for the substrate wafers.

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