A Neuromorphic VLSI Implementation of a Simplified Electrosensory System in a Weakly Electric Fish
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Motivation
The weakly electric *Mormyrid* fish senses its environment through active electrolocation for navigation and object detection. We present a modeling study of the sensory system of this fish, with the aim of gaining insight into the role of different neuronal populations as well as developing novel computational approaches for efficient, real-time near-range sensing devices.

Mormyrid – the Weakly Electric Fish
The *Mormyrid* senses its neighboring environment by generating electric field around itself through a tail organ. This field is generated in the form of short electrical pulses as a train of Electric Organ Discharge (EOD).

In the absence of field distortion, at ‘basal’ EOD, the electroreceptor afferents (first layer that feeds spikes to Electrosensory Lateral Line Lobe, ELL) emit 1 ~ 4 spikes.

The presence of an object affects the afferent spiking latencies as well as spikes/EOD.

Biological Basis of Electrosensory Lobe
The afferent fibres innervate the granular (Gr) layer (exc. and inh. cells). The exc. cells project to the large fusiform (Lf) cells. The local GABAergic interneurons, medium ganglions (Mg), inhibit the Lfs. The corollary discharge feedback (Electric Organ Corollary Discharge, EOCD) acts as gating and modulating input for Mg and Lf discharge [1].

Spiking Response in ELL Layers
Network response to varying basal EOD (DC) and LEOD amplitudes:

The visible jitter in spike time is due to the simulated mismatch among on-chip neurons.

CASE-I: For low DC and LEOD amplitude, Lfs fail to discharge.

CASE-II: Without Mg inhibition, Lfs evoke spikes at DC (basal EOD) also.

CASE-III: As Mg inhibition and EOCD feedback is reinstated, Lfs spike in the stronger LEOD region.

Conclusions and Future Work
We studied and modeled the ELL circuit of a weakly electric fish. The architecture reproduces biological observations by producing a temporal code for object proximity by means of a spiking neural network. An implementation on a multichip Address Event Representation (AER) [3] based system is currently being investigated.

References