Analyzing the Impact of Substrate Noise on Embedded Analog-to-Digital Converters

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Abstract - This paper presents the analysis and measurements of the impact of digital substrate noise on embedded Analog-to-Digital converters. The impact of substrate noise on analog design is explained, followed by a specific entire impact analysis of the impact on a regenerative comparator and an A/D converter. To confirm the analysis the substrate noise has also been measured on a test chip designed in a 0.35 μ m heavily-doped-substrate CMOS technology. From the measurements it was deduced that SNR and the effective number of bits are reduced by 20%.

Index terms – substrate noise, ADC, impact measurement, jitter.

I. Introduction

In the coming years the integration of full systems on chip (SoC) will increase, to reduce volume and cost. At the same time, the performances of analog design will increase, to be compatible with the performances required by new applications, e.g. new communication systems. But the amount of noise generated by the digital circuitry, and the sensitivity of the analog part to digital noise will increase as well. ADCs are the analog designs usually close to the digital noise sources. That is why this paper analyzes the impact of substrate noise on embedded ADCs. As the performance of high-speed ADCs typically using a parallelized topology is dependent of the performance of their comparator [1], we mainly concentrate on the comparator block and extend the analysis to the entire converter afterwards.

The paper is organized as follows. In the next section an overview of the noise coupling problem in analog design will be presented, followed by the substrate noise impact in the special case of comparator design. In section III the measurement setup will be presented, and in section IV measurements results will show the impact of the substrate noise on the comparator topology. In section V the impact of substrate noise on an entire ADC will be analyzed and applied to the measured results. Finally section VI will present some conclusions.

II. Overview of substrate noise impact in analog design

In this section an overview of the substrate noise problem in analog design will be presented. First, the impact of substrate noise in the MOS transistor model will be introduced. Secondly, the impact of substrate noise on regenerative comparator, a key building block for ADCs, will be analyzed.

A. Substrate noise in MOS transistor model

Substrate noise has an influence on the drain current, I_D , or on the transconductance, gm of a MOS transistor. This impact is described in the MOS transistor equations:

$$I_{D} = \frac{K_{p} \cdot W}{2 \cdot (1+\alpha) \cdot L} \cdot (V_{GS} - V_{T})^{2}$$
(1)

$$gm = \frac{K_p \cdot W}{(1 + 2 \cdot \alpha) \cdot L} \cdot (V_{GS} - V_T)$$
⁽²⁾

and
$$V_T \approx V_{T0} + \gamma \cdot \left(\sqrt{\phi + V_{SB}} - \sqrt{\phi}\right)$$
 (3)

The different process-dependent parameters are γ , the body-effect coefficient, ϕ , the surface inversion potential, α , the mobility reduction factor, and V_{T0} , the threshold voltage for $V_{SB} = 0V$.

 V_{SB} is the potential difference between the bulk connection and the source of transistor. This difference of potential is not directly the same potential as the substrate voltage, but can be considered as an "image" of this voltage introduced by the resistive substrate model. Usually, in presence of digital switching noise injected in the substrate, the substrate voltage is considered as a sum of sinusoidal signals at different frequencies, and with different amplitudes, over a large frequency range. In this case V_{SB} can be replaced by:

$$V_{SB} = \sum_{n=1}^{+\infty} A_n \cdot \sin(\overline{\omega}_n \cdot t)$$
⁽⁴⁾

In equation (1) and equation (2) V_{GS} - V_T can be replaced by the following expression:

$$V_{GS} - V_T = V_{GST0} - \Delta V_T \tag{5}$$

 V_{GST0} is equal to $(V_{GS} - V_{T0})$ and ΔV_T is equal to the part of V_T that depends on V_{SB} :

$$\Delta \mathbf{V}_{\mathrm{T}} = \gamma \cdot \left(\sqrt{\phi + V_{SB}} - \sqrt{\phi} \right) \tag{6}$$

From the previous equations two conclusions can be drawn on the MOS transistor sensitivity:

– The sensitivity to substrate noise is reduced for a transistor with a large V_{GST0} , as typically is the case for a current source for example. A transistor with small V_{GST0}

will be more sensitive to substrate noise, e.g. the input transistors for an opamp, which are usually designed for high gm, have typically low V_{GSTO} .

- A transistor with small V_{GST0} can be out of the saturation region for a large V_{SB} , since $V_{DSAT} = V_{GS} - V_T$ due to substrate impact.

B. Comparator and substrate noise

A typical regenerative comparator architecture is composed of two parts, a differential amplification stage, with a low gain A, followed by a latch [1], as shown in Figure 1. The latch is used to increase the switching speed from one output state to another.



The speed of a regenerative comparator is directly related to the regeneration time constant Tr [4], which is defined as: $Tr = \frac{Cgs_{3,4}}{gm_{3,4}}$, were $gm_{3,4}$ is the initial

transconductance of M_3 or M_4 , and Cgs the gate-source capacitance of each of these transistors. If we replace $gm_{3,4}$ by equation (2), we can see that Tr is inversely proportional to the source-bulk potential V_{SB} . But as it was explained above, the substrate noise voltage is not a fixed value but can be represented as a sum of sinusoidal signals, which make $gm_{3,4}$ time-dependent. Hence the variation of the Tr is not constant but depending of the time when you are measuring the output signal of the comparator.

This variation can be expressed as an output signal jitter, as shown in Figure 2.



If this jitter is gaussian distributed, the probability distribution of this jitter is equal to:

$$P(x) = \frac{1}{\sigma \cdot \sqrt{2 \cdot \pi}} e^{\left(\frac{-(x-\mu)^2}{2\sigma^2}\right)}$$
(7)

were σ is the standard deviation and μ de mean value of the distribution. The effect of this jitter becomes important in the design of high-speed ADCs, working with small period-to-jitter ratio.

III. Experimental setup

An experience was set up to provide measurements about the impact of the digital substrate noise on an analog design embedded in a large chip, and to measure the digital substrate noise on chip [5].

A test chip was designed and fabricated in $0.35 \,\mu\text{m}$ standard CMOS process on an epi-type substrate, with five metal and two poly layers (Figure 3). This test chip integrates a comparator array used to measure the substrate noise impact on analog cells.



Figure 3: Test chip micrograph.

The comparator schematic is shown in Figure 1. Figure 4 shows the implementation of the comparator array on the test chip. The input signals are common to all 15 comparators, and the output signal of each of them is connected to a digital multiplexing interface which is used to select which signal will be brought out, using six command signals C0 to C5.



Figure 4: Comparator array implementation.

The digital noise is generated using an on-chip digital IQ demodulator [6]. In our measurements the reference, logic REF (see Figure 3) will be used as noise source.

The presented test chip was used to measure the jitter of the comparator output due to the substrate noise. Since this output jitter is randomly varying around a mean value, it is measured using a statistical approach. In this case, the jitter is characterized by two parameters: the mean value, Tmean, and the standard deviation, $\sigma\Delta t$.

In order to measure these two parameters, a sampling oscilloscope was used. A noise sensor [7] was also integrated on the test chip to directly measure the substrate noise generated by the noise source and hence to provide a reference measurement for our analysis. In our measurements, the input of the digital logic was fixed, and the measurements were repeated for different digital clock frequencies.

IV. Measurement results

The output jitter of the comparator was measured for the presented test chip, with the comparator clock set to a period of 5 ns. An input signal with a frequency of 200 kHz was applied to the comparator input.

In order to see if the output signal of the comparator is affected by the substrate noise, a first measurement was done in the frequency domain. Figure 5 shows the spectrum of the output signal when the digital noise source is not injecting noise in the substrate (Figure 5a), and when the digital circuit is turned on, with a digital clock set to 41 MHz for this measurement (Figure 5b). We can clearly identify the extra spurs on the second plot, due to the influence of the digital substrate noise, mainly at the digital clock frequency and its harmonics.



Figure 5: Spectrum of the output signal a. with the REF noise source off, and b. with the noise source on (fclock = 41MHz).

A measurement of the standard deviation and of the mean value of the comparator output, without any digital activity, was performed first, to provide a reference value (Tmean0, sigma0) that includes all possible jitter that is present during our measurement and that is not due to substrate noise. This jitter depends on the clock source, input voltage source, sampling oscilloscope, etc.... Next, the mean and the standard deviation of the output signal jitter was measured, for N different digital frequencies. From these measurements we obtain a TmeanN and a sigmaN for each frequency.

In Figure 6 and Figure 7 the ratio between TmeanN and sigmaN, and the reference Tmean0 and sigma0 are plotted as a function of the digital clock frequency. The plot of the ratio between the measured value with digital activity and the reference value shows the amount of increase due to substrate noise. On the same figure in dashed line the substrate voltage is shown as measured with the noise sensor [6].



Figure 6: Plot of meanN/mean0, as a function of the digital frequency (left axis), and the substrate noise voltage value in mVrms (dashed line - right axis).



Figure 7 : Plot of sigmaN/sigma0, as a function of the digital frequency (left axis), and the substrate noise voltage value in mVrms (dashed line - right axis).

We can see on Figure 6 that the mean value is only affected by the substrate noise for high values of substrate noise voltage, but stays very close to Tmean0. We can see on Figure 7 that the standard deviation is increasing up to more than 5 times the value of sigma0 for the peak value of the substrate voltage. We can also observe that the average value of the sigma is increasing when the substrate noise voltage is increasing, i.e. the straight and the dashed lines more and less track each other in Figure 7.

V. Impact on embedded Analog to Digital Converters

In the previous sections we saw that the output of a comparator is affected by digital noise. In this section we will derive conclusions about the effect of the substrate noise on an embedded ADC, based on the knowledge from the measurements on the comparator.

One of the main problems in the design of high-speed ADCs is the clock jitter [1], [9]. It affects the ADC by changing the time when the input signal is sampled. The jitter on a comparator output that we measured above due to substrate noise is different in the sense that it does not modify the sampling time but affects the time characteristic of the comparator, the delay for example, and therefore the time characteristic of the ADC as well.

The impact of the clock jitter on the SNR of a sampling system was already discussed in the literature [10]. Wakimoto and al. in [11] derived formulas that describe the impact of timing jitter of a sampling system on the effective number of bits and the SNR of an ADC. If the input voltage is equal to $V_{in} = A \cdot \sin(2 \cdot \pi \cdot f_{in} \cdot t)$, then the root mean square value of the error due to the jitter and due to the quantization noise, respectively Err_{jrms} and Err_{qrms} , for an n-bit ADC are equal to:

$$Err_{jrms} = (\sqrt{8 \cdot \pi} \cdot f_{in} \cdot \sigma_T) \cdot S_{rms}$$
(8)

$$Err_{qrms} = \frac{S_{rms}}{2^n \cdot \sqrt{6/2}} \tag{9}$$

where $S_{rms} = A/\sqrt{2}$ is the rms value of the input amplitude and $\sigma_{\rm T}$ is the standard deviation of the jitter.

From these expressions the expression for the SNR, and the effective number of bits, ENOB or N_{eff} , derived:

$$SNR = 20 \cdot \log \left(\frac{S_{rms}}{\sqrt{Err_{jrms}^{2} + Err_{qrms}^{2}}} \right)$$
(10)

$$N_{eff} = n - \log_2 \left(\sqrt{1 + \left(\frac{Err_{jrms}}{Err_{qrms}}\right)^2} \right)$$
(11)

From our comparator measurements and using the formulas of Wakimoto and al., we extract the relative variation of the SNR and of the effective number of bits, $Delta_{SNR}$ and $Delta_{Neff}$, due to substrate noise, if the measured comparator would be used in a full n-bit ADC converter:

$$Delta_{SNR} = \frac{SNR_N}{SNR_0}$$
(12)

$$Delta_{Neff} = \frac{N_{effN}}{N_{eff0}}$$
(13)

For the 8-bit ADC presented in [3], for an input frequency of 1 MHz, and for a digital clock at 20 MHz, we calculate the variation on the SNR and the effective number of bits: as Delta_{SNR} = 0.8037 and Delta_{Neff} = 0.7932. We see that the SNR is dependent of the substrate noise and reduced by 20%, and the effective number of bits is reduced by

20% as well, due to the extra distortion introduced by the substrate noise induced jitter.

VI. Conclusions

In this paper the substrate noise impact on embedded comparators and analog-to-digital converters was discussed. The substrate noise impact at the output of a regenerative comparator was measured as an equivalent output signal jitter increase versus the jitter without any substrate noise. The substrate noise voltage induces a jitter at the output of the comparator that is up to more than 5 times larger than the normal output jitter. When a comparator is used in the design of an ADC, the jitter at the output of the comparator reduces the performance of the ADC. A reduction in 20% of the effective number of bits and of the SNR, was calculated.

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