

An Approach to Tackle Quantization Noise Folding in Double-Sampling $\Sigma\Delta$ Modulation A/D Converters

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Abstract— $\Sigma\Delta$ -modulation is a proven method to realize high- and very high-resolution analog-to-digital converters. A particularly efficient way to implement such a modulator uses double-sampling where the circuit operates during both clock phases of the master-clock. Hence, the sampling frequency is twice the master-clock frequency. Unfortunately, path mismatch between both sampling branches causes a part of the quantization noise to fold from the Nyquist frequency back in the signal band. Therefore, the performance is severely degraded. In this paper, we show that the problem is reduced but not eliminated by employing multibit quantization. Next, we present an indepth solution for the problem. The approach consists of modifying the quantization noise transfer function of the overall modulator to have one or several zeros at the Nyquist frequency. This way the effect of noise folding can nearly be eliminated. It is shown that this can be implemented by a simple modification of one of the integrators of the overall modulator circuit. Finally, several design examples of single-bit and multibit modulators are discussed.

Index Terms—Analog-to-digital conversion, double-sampling, spectral shaping.

I. INTRODUCTION

SIGMA-DELTA ($\Sigma\Delta$)-modulation is a proven technique to realize high- and very high-resolution analog-to-digital (A/D) converters. Where traditional implementations relied on a single-bit quantizer, today the matureness of dynamic element matching techniques allows the use of a multibit quantizer [1]–[7]. This way the modulator architecture can achieve an even higher performance. Therefore, in practice the overall accuracy of a $\Sigma\Delta$ -modulation A/D-conversion circuit is likely to be limited by circuit noise and not by quantization noise. Hence, it is of utmost importance to have an efficient circuit-level implementation. This could be achieved by the use of double-sampling techniques. Here the circuit operates during both clock phases of the master-clock. This way a sampling frequency that is twice the master-clock frequency is achieved [8]–[17]. A major disadvantage of a double-sampling $\Sigma\Delta$ -modulator is its sensitivity to path gain mismatch which causes quantization noise to fold from the Nyquist frequency back in the signal band. In the past, two solutions for this problem have been proposed. The first uses dynamic element

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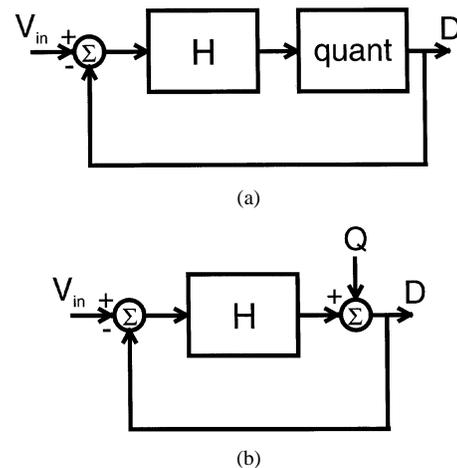


Fig. 1. (a) Conceptual diagram of a $\Sigma\Delta$ modulation A/D converter and (b) its linearized model.

matching techniques to shape the folded noise out of the signal band [13], [14]. The second approach uses a bilinear input integrator [15]–[17]. With both these approaches the feedback digital-to-analog converter requires a separate capacitor instead of sharing the input-sampling capacitor. This has the disadvantage that the feedback factor around the operational amplifier of the first integrator is reduced. Moreover, extra thermal noise is sampled on the additional capacitor.

In this paper we present a new approach that tackles the problem by modifying the quantization noise transfer function (NTF) of the overall modulator. It will be shown that this can be implemented by a simple modification of one of the integrators of the overall modulator circuit. In Section II, double-sampling $\Sigma\Delta$ modulators are briefly reviewed and the phenomenon of noise folding is explained. It is also shown how multibit modulation provides a partial solution for this problem. In Section III, we introduce our new method and explain how it can easily be implemented at the circuit level. Section IV discusses some design examples and finally the conclusions are presented in Section V.

II. NOISE FOLDING IN DOUBLE-SAMPLING $\Sigma\Delta$ MODULATORS

A. Double-Sampling $\Sigma\Delta$ Modulators

Fig. 1(a) shows a system level diagram of a $\Sigma\Delta$ modulation A/D converter. It consists of a loop with an analog filter H and a (single- or multibit) quantizer. The output D of the quantizer is fed back to the input of the filter. Fig. 1(b) shows the common “linearized” model of such a $\Sigma\Delta$ modulator where the operation

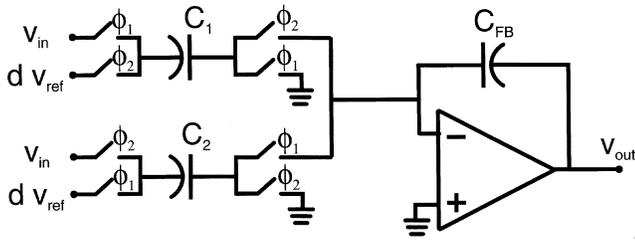


Fig. 2. Typical double-sampling input circuit of a $\Sigma\Delta$ modulation A/D converter.

of the quantizer is modeled by an additive error Q . This system can easily be analyzed in the Z -domain

$$D(z) = \underbrace{\frac{H(z)}{1+H(z)}}_{\text{STF}(z)} V_{\text{in}}(z) + \underbrace{\frac{1}{1+H(z)}}_{\text{NTF}(z)} Q(z). \quad (1)$$

The closed-loop transfer function of V_{in} to the output D is commonly called the signal transfer function STF whereas the transfer function of the quantization term Q is called the NTF. Normally the magnitude of the loop filter should be large (infinite) in the low-pass band of interest. Then (1) can be simplified

$$D(z) \approx V_{\text{in}}(z) + \text{NTF}(z)Q(z). \quad (2)$$

Fig. 2 shows a typical switched-capacitor implementation of the input circuit of a double-sampling $\Sigma\Delta$ modulation A/D converter [13]–[17]. It consists of an operational amplifier, a fixed feedback capacitor C_{FB} and two nominally matched switched input capacitors C_1 and C_2 . As is common the circuit operates on two nonoverlapping clock phases ϕ_1 and ϕ_2 . However, the output voltage v_{out} of the integrator is updated on both clock phases ϕ_1 and ϕ_2 because the two switched input capacitors operate in tandem. Hence, the sampling frequency equals twice the master clock frequency. Unfortunately the two input sampling capacitors C_1 and C_2 can be matched only with a limited accuracy. If we take this effect into account, the output voltage sequence $v_{\text{out}}(n)$ can be written as

$$v_{\text{out}}(n) = v_{\text{out}}(n-1) + \frac{C_{\text{av}}}{C_{\text{FB}}} (1 + (-1)^n \delta) \cdot (v_{\text{in}}(n-1) - d(n-1)) \quad (3)$$

where $C_{\text{av}} = (C_1 + C_2)/2$ and $\delta = (C_1 - C_2)/(C_1 + C_2)$. Here, lowercase letters are used when explicitly time domain sequence representations of signals are intended. For a Z -domain representation we will use uppercase letters. Without loss of generality the reference voltage v_{ref} is set equal to 1. Recalling that the sampling frequency is twice the master clock frequency it is noticed that the sequence $(-1)^n$ corresponds to a clock signal.

If δ equals 0 this circuit performs the normal integrator operation. In any real circuit, however, $\delta \neq 0$ and, hence, there is an undesired amplitude modulation effect. To study this effect we define the input referred equivalent voltage $v_{\text{eq}, \text{in}}$ as

$$v_{\text{eq}, \text{in}}(n) = \delta(d(n) - v_{\text{in}}(n))(-1)^n. \quad (4)$$

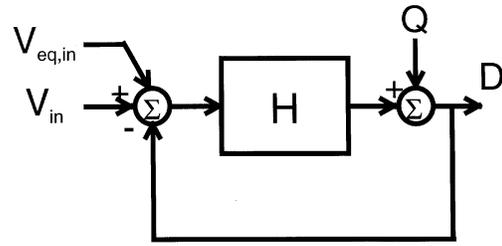


Fig. 3. System-level model of a double-sampling $\Sigma\Delta$ modulator.

Then the output voltage sequence of the input integrator of the modulator [(3)] can be rewritten as

$$v_{\text{out}}(n) = v_{\text{out}}(n-1) + \frac{C_{\text{av}}}{C_{\text{FB}}} \cdot (v_{\text{in}}(n-1) + v_{\text{eq}, \text{in}}(n-1) - d(n-1)). \quad (5)$$

This is the same expression as for an ideal integrator with an additional input signal $v_{\text{eq}, \text{in}}$. Hence, we can conclude that the effect of path mismatch can be modeled by adding the equivalent input referred voltage $v_{\text{eq}, \text{in}}$ (or $V_{\text{eq}, \text{in}}$ in the Z -domain) to the overall input of the modulator-model of Fig. 1. This is shown in Fig. 3.

The additional input ($V_{\text{eq}, \text{in}}$) on Fig. 3 will result in an extra error contribution in the output signal D of the overall modulator. We shall denote this extra error term the *folded noise* N_{Fold} . Then the output signal D can be written as

$$D(z) \approx V_{\text{in}}(z) + \text{NTF}(z)Q(z) + N_{\text{Fold}}(z). \quad (6)$$

Let us now focus on $V_{\text{eq}, \text{in}}$. From its definition in (4) it is clear that this signal contains an amplitude modulation with the clock signal $(-1)^n$. Due to the double sampling the clock frequency equals the Nyquist frequency f_N (half the sampling frequency). Such an amplitude modulation with the Nyquist frequency f_N corresponds to a frequency translation of f_N . In the Z -domain this corresponds to a substitution $z \rightarrow -z$. This can be formulated more strictly as

$$\begin{aligned} V_{\text{eq}, \text{in}}(z) &= \delta \sum_{n=0}^{\infty} (-1)^n z^{-n} (d(n) - v_{\text{in}}(n)) \\ &= \delta \sum_{n=0}^{\infty} (-z)^{-n} (d(n) - v_{\text{in}}(n)) \\ &= \delta(D(-z) - V_{\text{in}}(-z)). \end{aligned}$$

By inspection of Fig. 3, the folded noise can be written as

$$\begin{aligned} N_{\text{Fold}}(z) &\approx V_{\text{eq}, \text{in}}(z) \\ &= \delta(D(-z) - V_{\text{in}}(-z)) \end{aligned} \quad (7)$$

where $D(z)$ is given by (6). After substitution we get

$$N_{\text{Fold}}(z) \approx \delta(\text{NTF}(-z)Q(-z) + N_{\text{Fold}}(-z)). \quad (8)$$

This expression is exact apart from the approximation that the signal transfer function equals one in the band of interest. Now, the term $\delta N_{\text{Fold}}(-z)$ is of second order in δ . Because the path mismatch δ is small, this second-order contribution can be

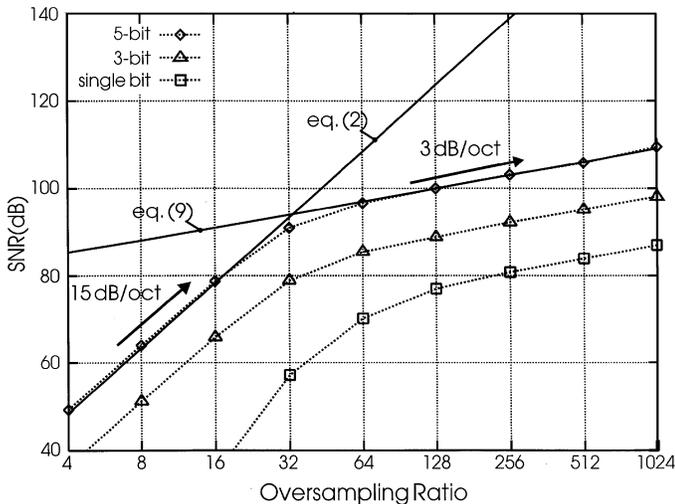


Fig. 4. Calculated and simulated SNR of double-sampling second-order $\Sigma\Delta$ modulators versus the oversampling ratio for various quantizer resolutions.

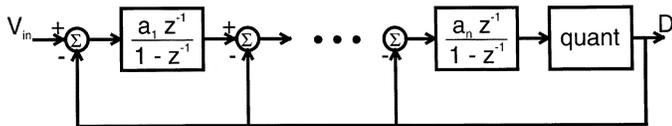


Fig. 5. System-level diagram of the architecture of a $\Sigma\Delta$ modulator.

neglected. Hence, we obtain the following expression for the folded noise:

$$N_{\text{Fold}}(z) \approx \delta Q(-z)NTF(-z). \quad (9)$$

Typically, the magnitude of the folded $NTF(-z)$ will not be small in the band of interest (where $z \approx 1$) and, hence, this error contribution can be the performance limiting factor. Equation (9) clearly indicates that the effect of noise folding in double-sampling can successfully be reduced by decreasing Q as well as by modifying the magnitude of $NTF(-z)$ in the signal band.

B. Multibit Quantization: A Partial Solution

The use of multibit quantization directly lowers the magnitude of the quantizer error Q which in turn decreases the amount of noise that can be folded into the baseband. In practice, the need for further measures may even be eliminated for medium-accuracy converters. To illustrate this, a computer simulation was performed for a second-order modulator with a $NTF = (1 - z^{-1})^2$. The case of a single bit, a 3-bit and a 5-bit quantizer were considered. In both multibit cases the operation of the feedback digital-to-analog converter was assumed to be ideal. In practice this is not the case but the effect of mismatch in the feedback DAC can be remediated through the use of a dynamic element matching technique [1]–[7]. The mismatch δ between both branches of the double-sampling circuit was taken 0.1%. The simulated signal-to-noise ratio (SNR) for both cases is shown on Fig. 4. For the 5-bit case the SNR for the shaped quantization noise alone [calculated from (2)] as well as for the folded noise alone [calculated from (9)] was added. From a comparison between the simulated and calculated plots it is clear that for small oversampling ratios up to 32, the performance remains

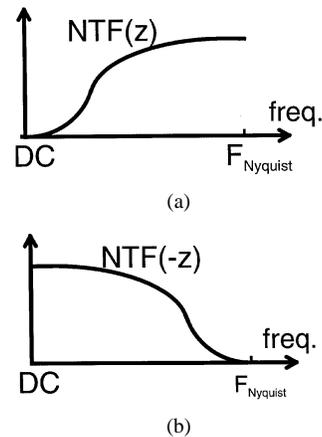


Fig. 6. (a) Normal and (b) folded NTF of a conventional $\Sigma\Delta$ modulator.

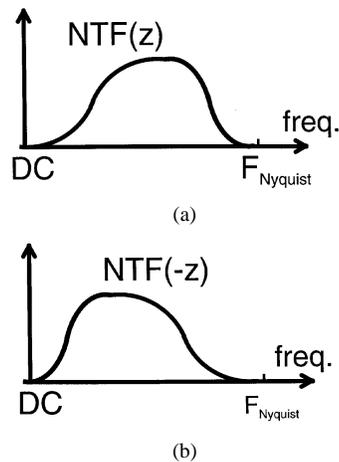


Fig. 7. (a) NTF and (b) folded NTF of a modified $\Sigma\Delta$ modulator.

nearly unaffected with the characteristic slope of 15 dB/octave of second-order noise-shaping. For higher oversampling ratios, the folded noise limits the performance.

It should be noted that the 5-bit modulator still allows 15-bit performance for an oversampling ratio of 32 without remediating the folded noise. The 3-bit modulator requires an oversampling ratio as high as 256 to obtain 15-bit performance. For the single-bit case this is even 2048.

III. MODIFYING THE QUANTIZATION NOISE TRANSFER FUNCTION

A. General Principle

The basic idea of our new approach to eliminate quantization noise folding is by modifying the loop-filter and, hence, the NTF. By extension also the folded noise can be modified. To explain the principle, the architecture of a typical implementation of a $\Sigma\Delta$ modulator is shown on Fig. 5. The magnitude of the resulting NTF is shown on Fig. 6(a): it exhibits several zeros at DC. Unfortunately the magnitude is large at the Nyquist-frequency. As indicated on Fig. 6(b) this will result in a large amount of quantization noise folded in the baseband.

Our new approach is to modify the NTF such that it has one or several zeros at the Nyquist frequency as well. This way the magnitude of the NTF will take the form of Fig. 7(a). As shown

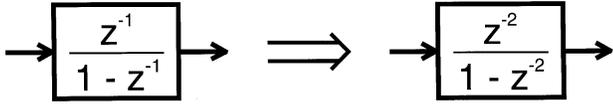


Fig. 8. A simple means to modify the NTF of a conventional $\Sigma\Delta$ modulator.

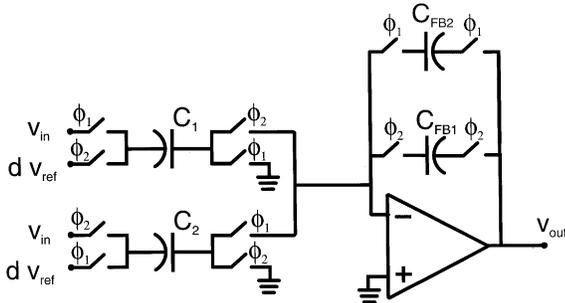


Fig. 9. Double-sampling circuit with a transfer function $\sim z^{-1}/(1-z^{-2})$.

on Fig. 7(b), the amount of noise folded toward DC will be reduced to a large extent.

Hence, the ideal NTF of a modified $\Sigma\Delta$ modulator will take the following form:

$$\text{NTF} = (1 - z^{-1})^n (1 + z^{-1})^m. \quad (10)$$

Here, n is the number of zeros at DC and corresponds to the order of the conventional $\Sigma\Delta$ modulator, m is the number of zeros at the Nyquist frequency. This equation also reveals the main drawback of this approach. Since $z \approx 1$ in the baseband, the factor $(1 + z^{-1})^m \approx 2^m$ in the baseband. This implies that the quantization-noise performance is reduced by 6 dB for each zero at the Nyquist frequency.

For this reason only as few zeros at the Nyquist frequency as possible should be added. Therefore, we can readily assume that $m < n$. Then the ideal modified NTF can be written as

$$\text{NTF} = (1 - z^{-1})^{(n-m)} (1 - z^{-2})^m. \quad (11)$$

It is important to note that this is the *ideal* form of the modified NTF. As will be illustrated in Section IV, an actual synthesis of a stable and manufacturable modulator is likely to exhibit nonzero poles in the modified NTF (and also in the STF).

B. An Efficient Circuit

A simple modification of the architecture of Fig. 5 that allows to obtain the desired zeros consists of replacing m integrators with a transfer function $z^{-1}/(1-z^{-1})$ by resonators with a transfer function $z^{-2}/(1-z^{-2})$. This is shown on Fig. 8.

An efficient double-sampling resonator circuit is shown on Fig. 9. It consists of an operational amplifier, two nominally matched feedback capacitors C_{FB1} and C_{FB2} and two nominally matched input capacitors C_1 and C_2 .

In practice the capacitor pairs C_{FB1} , C_{FB2} and C_1 , C_2 can only be matched with limited accuracy. Similarly as in Section II-A, the output voltage sequence $v_{\text{out}}(n)$ of this circuit can be written as

$$v_{\text{out}}(n) = v_{\text{out}}(n-2) + a_{\text{av}}(1 + \epsilon(-1)^n) \cdot (v_{\text{in}}(n-1) - d(n-1)). \quad (12)$$

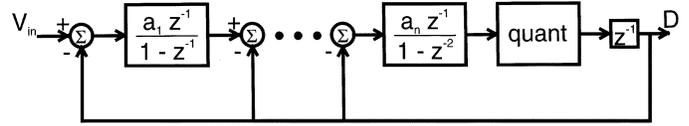


Fig. 10. Type I modified $\Sigma\Delta$ modulator architecture.

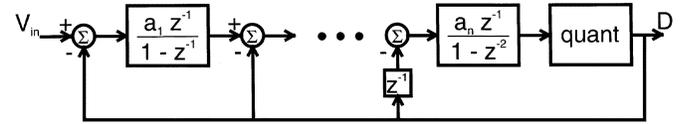


Fig. 11. Type II modified $\Sigma\Delta$ modulator architecture.

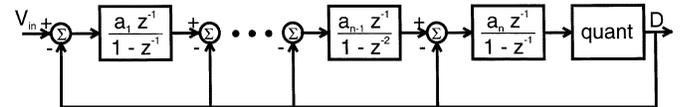


Fig. 12. Type III modified $\Sigma\Delta$ modulator architecture.

Here, we have introduced the average gain of the resonator a_{av} as $a_{\text{av}} = (a_{\text{odd}} + a_{\text{even}})/2$ where $a_{\text{odd}} = C_1/C_{FB1}$ and $a_{\text{even}} = C_2/C_{FB2}$. Further the path gain mismatch ϵ is defined as $\epsilon = (a_{\text{odd}} - a_{\text{even}})/(a_{\text{odd}} + a_{\text{even}})$.

For perfectly matched capacitors $\epsilon = 0$ and the transfer function of the circuit becomes $a_{\text{av}} z^{-1}/(1-z^{-2})$. Except for one delay in the signal path this performs the desired operation of Fig. 8.

For a nonzero ϵ the input is modulated again with the clock sequence $(-1)^n$. If this circuit is used in a double-sampling $\Sigma\Delta$ modulator, this effect can be referred to the input of the overall modulator, just as was done in Section II-A. Hence, it contributes to the global quantization noise folding from the Nyquist frequency toward the baseband, in exactly the same way as the path mismatch of the conventional integrator circuit of Fig. 2. Consequently, its effect is nearly eliminated by the modification of the NTF. This way it is concluded that this is a suitable circuit for use in a double-sampling modulator with a modified NTF.

C. One Zero at the Nyquist Frequency

In most applications the addition of only one zero at the Nyquist frequency should sufficiently reduce the effect of noise-folding. Many architectures can achieve this. Here some efficient implementations based on the circuits of Figs. 2 and 9 are discussed.

Fig. 10 shows an architecture which implements the transformation of Fig. 8 on the last integrator of the conventional architecture of Fig. 5. The other integrators remain unchanged. The additional delay in the last resonator, is performed on the digital output. This requires only one flip-flop (or a few flip-flops in the case of a multibit modulator). We shall denote this architecture a type I modified modulator.

Fig. 11 shows a type II modified modulator. This architecture cannot be obtained by a simple application of the transformation of Fig. 8. However, it can also be realized by the efficient circuits of Figs. 2 and 9. Again an additional delay in the digital signal path is needed. The need for this additional delay can be understood as follows: near the Nyquist-frequency we have

TABLE I
DETAILS OF THE EXAMPLE TYPE II MODULATORS

	a_i coefficients	NTF	STF
2@DC+1@Nyq	(2/5 1)	$\frac{(1-z^{-1})^2(1+z^{-1})}{1-z^{-1}+\frac{2}{5}z^{-2}}$	$\frac{\frac{2}{5}z^{-2}}{1-z^{-1}+\frac{2}{5}z^{-2}}$
4@DC+1@Nyq	(1/16 1/8 1/4 1)	$\frac{(1-z^{-1})^4(1+z^{-1})}{1-3z^{-1}+\frac{13}{4}z^{-2}-\frac{752}{512}z^{-3}+\frac{113}{512}z^{-4}}$	$\frac{\frac{1}{512}z^{-4}}{1-3z^{-1}+\frac{13}{4}z^{-2}-\frac{752}{512}z^{-3}+\frac{113}{512}z^{-4}}$

$z \approx -1$. Hence, removing the delay would generate a positive feedback path around the resonator. This could cause instability.

Finally, Fig. 12 shows a type III modified modulator. In contrast to the other types here the last but one integrator is modified. No additional delay in the digital signal path is needed because the number of delays in the main feedback path around the resonator is even.

In fact many more architectures that allow to obtain an NTF with zeros of the form of (11) can be conceived but the considered ones are among the simplest. This also raises two important additional considerations. First, it must be recognized that the structures of Figs. 10–12 pose restrictions on the NTFs that can be implemented. This is easily understood because the modulators are of order $n+1$ and there are only n coefficients. Hence, we are short of one degree of freedom, to implement arbitrary pole positions for the NTF (and also for the STF). This means that these architectures may lead to pole positions that have undesired properties such as e.g., peaking or excessive low-pass filtering of the STF. A complete study of these aspects goes beyond the scope of this paper but should be addressed in any design that incorporates these structures. Second, it should also be noted that the set of a_i coefficients should be different for each of the architectures of Figs. 5 and 10–12. The reason for this is that the pole positions depend both on these coefficients as well as on the position of the resonator.

IV. DESIGN EXAMPLES

We have performed several simulations to confirm the effectiveness of the proposed techniques. For all three architectures of the previous section, suitable coefficients could be found to obtain stable modulator performance. These coefficients were determined ad hoc¹ and it is not claimed that they are optimal.

Underneath, some examples are presented for the type II architecture (Fig. 11). Such a modulator exhibits n zeros in the baseband and 1 zero at the Nyquist frequency. Hence, its order is actually $(n+1)$ but the baseband behavior is similar to that of an n th order modulator. Also the circuit complexity is com-

¹These coefficients were determined by a trial and error procedure, not by a systematic design approach. The goal was just to illustrate the feasibility of the proposed circuits.

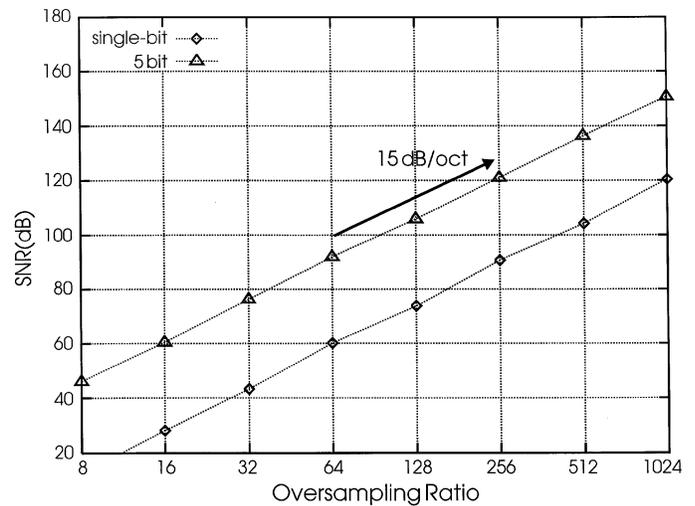


Fig. 13. Simulated SNR versus the oversampling ratio of double-sampling type II modulators of order 2@DC+1@Nyq.

parable to that of a conventional n th order modulator. We shall denote this as “a modulator of order n @DC+1@Nyq.”

A. Modulator of Order 2@DC+1@Nyq

First modulators with $n = 2$ were studied. Both the single-bit and multibit case were considered. For compactness the same coefficients were used for the single-bit and multibit cases here (see Table I). However, it was found that just as for conventional modulators more aggressive noise-shaping can be achieved by multibit modulation compared to the single-bit case.

Fig. 13 shows the simulated SNR versus oversampling ratio for a single-bit and a 5-bit modulator. In both cases the mismatch δ between both sampling branches was set to 0.1%. In the multibit case the feedback DAC was assumed to be ideal (just as for the simulation of Fig. 4). In practice a dynamic element matching technique is needed here [1]–[7]. The SNR was evaluated with a half-scale sine wave.

From Fig. 13 it is clear that the performance of these modified second-order modulators is not limited by folded noise. A comparison with Fig. 4 demonstrates the effectiveness of our new technique.

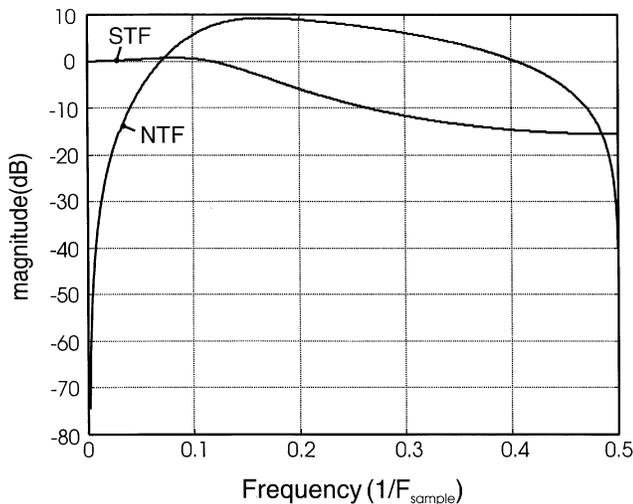


Fig. 14. Magnitude of the STF and NTF versus frequency for the example type II modulator of order 2@DC+1@Nyq.

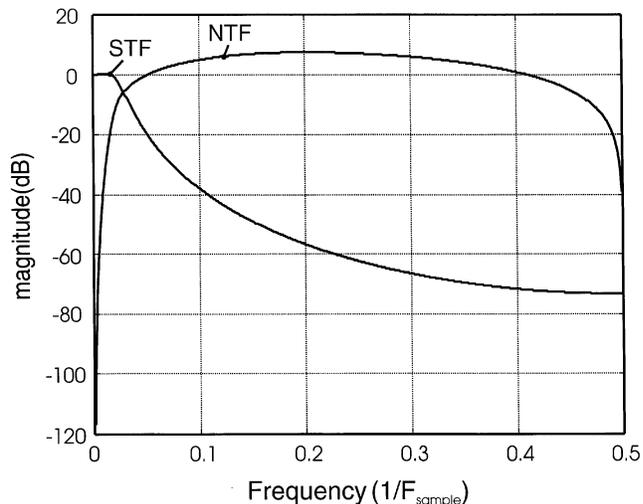


Fig. 16. Magnitude of the STF and NTF versus frequency for the example type II modulator of order 4@DC+1@Nyq.

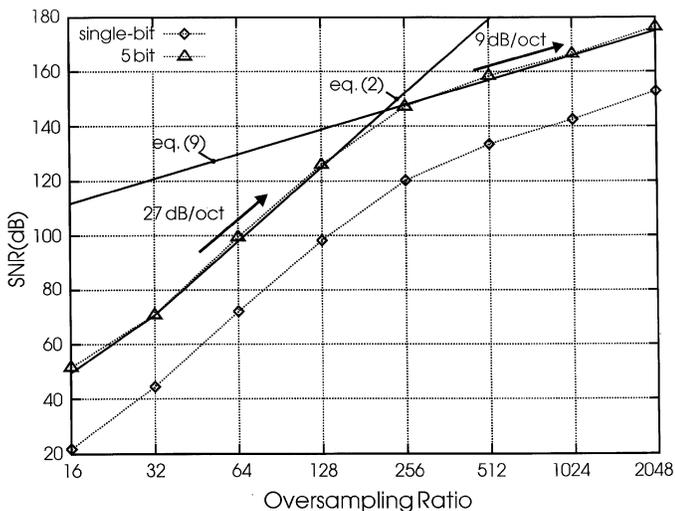


Fig. 15. Simulated SNR versus the oversampling ratio of the example double-sampling type II modulators of order 4@DC+1@Nyq.

The signal and noise transfer functions for this example are shown on Fig. 14 and the analytical expressions are listed in Table I. It is observed that the STF exhibits a low-pass filter effect and a small amount of peaking in the passband. In most applications the oversampling ratio will be higher than eight, and hence, these effects will be neglectable for this example.

B. Modulator of Order 4@DC+1@Nyq

Next high-order single-loop modulators with $n = 4$ were studied. The details of the considered structure are shown in Table I as well. Here also the same coefficients were used for the single-bit and multibit cases for compactness.

Fig. 15 shows the simulated SNR versus the oversampling ratio. Again the mismatch δ between the sampling branches was 0.1% and the multibit feedback DAC was assumed to be ideal. The SNR was evaluated with a half-scale sine wave.

For the 5-bit case also the theoretical SNR for the shaped quantization noise (2) and for the folded noise (9) fourth-order modulators is limited by folded quantization noise for very high

signal to noise ratios. This folded quantization noise is first-order shaped due to the zero at the Nyquist frequency in the NTF.

The plots of the signal and noise transfer functions for this example are shown on Fig. 16. From the figure it is clear that the STF exhibits a pronounced low-pass filter effect with a cutoff frequency around $f_N/20$. Therefore, this modulator is only usable for applications with a sufficiently high oversampling ratio.

C. Possible Extensions

It is clear that just as for the case of conventional modulators the approach can be refined by spreading the baseband zeros over the entire signal band. In fact the entire design of the loop filters could be improved. It is expected that the approach of [18] can be generalized toward the design of our modified modulators but a complete study of this is out of the scope of this paper.

It is also obvious that our approach can be applied to double-sampling multistage (MASH) modulators [19]–[21] as well. In this case only the first stage should be modified, because the effect of noise folding in a later stage is shaped anyway by the NTF of the preceding stages.

V. CONCLUSION

We have analyzed noise folding in double-sampling $\Sigma\Delta$ modulation A/D converters. We have shown that the problem is reduced but not eliminated by employing multibit quantization. Next we have introduced the concept of a modified NTF and shown that the effect of noise folding can almost completely be eliminated by adding zeros in the NTF at the Nyquist frequency. Several efficient circuits and architectures to implement this were discussed. Finally the approach was applied to the design of single-loop modulators of second and fourth order. Both single-bit and multibit modulators were considered and it was shown that the effect of noise-folding was nearly eliminated. We expect that this new method removes most practical problems for a wide application of double-sampling in $\Sigma\Delta$ modulation A/D converters.

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