

A 13.5-b 1.2-V Micropower Extended Counting A/D Converter

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Abstract—This work presents a study of the extended counting technique for a 1.2-V micropower voice-band A/D converter. This extended counting technique is a blend of $\Sigma\Delta$ modulation with its high resolution but relatively low speed and algorithmic conversion with its higher speed but lower accuracy. To achieve this, the converter successively operates first as a first-order $\Sigma\Delta$ modulator to convert the most significant bits, and then the same hardware is used as an algorithmic converter to convert the remaining least significant bits.

An experimental prototype was designed in 0.8- μm CMOS. With a 1.2-V power supply, it consumes 150 μW of power at a 16-kHz Nyquist sampling frequency. The measured peak $S/(N + \text{THD})$ was 80 dB and the dynamic range 82 dB. The converter core including the controller and all reconstruction logic occupies about $1.3 \times 1 \text{ mm}^2$ of chip area. This is considerably less than a complete $\Sigma\Delta$ modulation A/D converter where the digital decimation filter would occupy a significant amount of chip area.

Index Terms—Analog-to-digital, extended counting, low power, low voltage.

I. INTRODUCTION

THE WORK presented here deals with a study of the extended counting technique [1] for a low-voltage voice-band A/D converter targeted toward a medical application. This application requires at least 12-b linearity and noise performance. Moreover, single-battery operation is strongly desirable and the power consumption should be as low as possible. The total chip area should be small as well.

Traditionally, there are at least two possible candidate architectures for these specifications. The first is based on $\Sigma\Delta$ modulation [2]–[5]. Here a high resolution can be achieved at the expense of oversampling. This typically leads to an increased power consumption, although several design techniques can be used to cut the power drain. Moreover, these implementations require digital decimation filters that may occupy several square millimeters of silicon area.

The second candidate architecture is an algorithmic A/D converter [6]–[9]. Here, both the chip area and the power consumption can be very low. However, the linearity depends on component matching and therefore high resolution is difficult to achieve [6]. Recently, a circuit has been presented where through a combination of careful layout and process control up to 14-b component matching was demonstrated [10]. However,

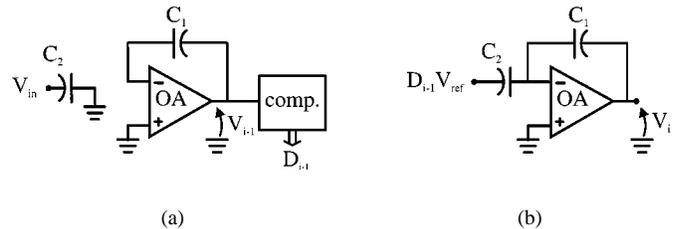


Fig. 1. Circuit configuration during both phases of a counting conversion step. (a) First phase. (b) Second phase.

such a high accuracy is very difficult to achieve in most standard CMOS processes. Alternatively, sophisticated circuit techniques can be used to enhance the linearity of such an algorithmic converter (e.g., [7]–[9]). This inevitably increases the complexity and therefore also the power consumption and the chip area.

In this work, we try to combine the advantages of $\Sigma\Delta$ modulation and algorithmic A/D conversion by employing the extended counting A/D conversion technique [1].

II. EXTENDED COUNTING

A. Principle

The extended counting technique is a compromise between $\Sigma\Delta$ modulation with its high accuracy but relatively low speed on the one hand and algorithmic A/D conversion with its higher speed but lower accuracy on the other hand [1]. For one A/D conversion, the converter passes through two modes. In the first mode, the system operates as a resettable first-order $\Sigma\Delta$ modulator to convert the most significant bits. This mode is called the “counting conversion.” Then in a second mode the same hardware is used to convert the least significant bits by an algorithmic A/D conversion technique. This mode is called the “extended conversion.” Both the counting as well as the extended conversion mode will take several clock cycles.

We shall first discuss the approach for a dc input voltage V_{in} . During the first part of a conversion, the system will be in the counting conversion mode. The circuit configuration during this mode is depicted in Fig. 1. In reality, the actual circuits are fully differential, but for the sake of simplicity the discussion is done here for a single-ended equivalent. It consists of a switched-capacitor integrator and a comparator. After an initial reset, the normal operation in each step consists of two phases. In the first phase of the i th step, the input voltage V_{in} is sampled on the input capacitor C_2 . Meanwhile, the output voltage V_{i-1} of the previous step is still available at the integrator’s output. Based on this voltage, a comparator decides the code D_{i-1} . The value of this code is +1 if the voltage V_{i-1} is positive and –1 if it

Manuscript received May 30, 2000; revised October 9, 2000.

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Publisher Item Identifier S 0018-9200(01)00924-6.

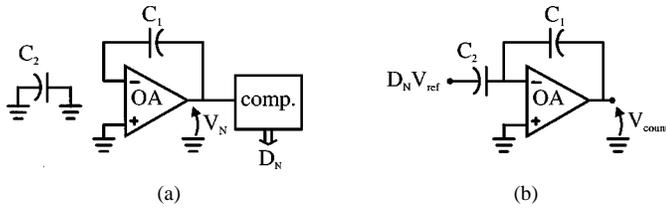


Fig. 2. Circuit configuration during the last counting conversion step. (a) First phase. (b) Second phase.

is negative. In the second phase, the top plate of the sampling capacitor C_2 is switched toward the opamp inverting node and the bottom plate is switched toward $\pm V_{\text{ref}}$ depending on the code D_{i-1} . Then the charge is transferred toward the feedback capacitor C_1 . Thus we obtain the output voltage V_i for the i th step:

$$V_i = V_{i-1} + \frac{C_2}{C_1} (V_{\text{in}} - D_{i-1} V_{\text{ref}}). \quad (1)$$

It is well known for this first-order $\Sigma\Delta$ modulator structure that the integrator output voltage V_i remains bounded. More precisely, we have

$$-\frac{2C_2}{C_1} V_{\text{ref}} \leq V_i \leq \frac{2C_2}{C_1} V_{\text{ref}}. \quad (2)$$

For notational convenience, we shall assume that V_{ref} equals 1. This can be done without loss of generality. Due to the initial reset, we have $V_0 = 0$ and $D_0 = 0$. Therefore, this recursion can be solved to write the voltage V_N after the last counting step as follows:

$$V_N = N \frac{C_2}{C_1} V_{\text{in}} - \frac{C_2}{C_1} \sum_{i=1}^{N-1} D_i. \quad (3)$$

Then one additional step is performed to obtain the output voltage V_{count} for the counting conversion (Fig. 2). This step operates as the previous N steps except that in the first phase, the capacitor C_2 is reset instead of charged to the input voltage V_{in} :

$$V_{\text{count}} = V_N - \frac{C_2}{C_1} D_N V_{\text{ref}}. \quad (4)$$

By combining this with (3) we can write V_{count} as:

$$V_{\text{count}} = N \frac{C_2}{C_1} V_{\text{in}} - \frac{C_2}{C_1} \sum_{i=1}^N D_i. \quad (5)$$

It can be shown that the voltage range of this final output voltage V_{count} is reduced by a factor of 2 compared to (2) [1]:

$$-\frac{C_2}{C_1} V_{\text{ref}} \leq V_{\text{count}} \leq \frac{C_2}{C_1} V_{\text{ref}}. \quad (6)$$

To reconstruct the input voltage V_{in} , (5) can be rewritten as

$$V_{\text{in}} = \frac{\sum_{i=1}^N D_i + \frac{C_1}{C_2} V_{\text{count}}}{N}. \quad (7)$$

After the counting steps, the system goes into the extended conversion mode where the voltage V_{count} is measured by a more efficient but less accurate algorithmic A/D conversion technique.

For the moment, we shall make abstraction of the extended conversion and assume that it results in a digital approximation $D_{\text{ext}}(V_{\text{count}})$ for the residue voltage V_{count} . Errors during the extended conversion are modeled by an additive error ε_{ext} . This error is an unknown function of the residue voltage V_{count} . Then we can write

$$D_{\text{ext}}(V_{\text{count}}) = V_{\text{count}} + \varepsilon_{\text{ext}}(V_{\text{count}}). \quad (8)$$

Together with (7) this allows us to obtain the digital output $D(V_{\text{in}})$. This should be a close approximation of the overall input voltage V_{in} :

$$D(V_{\text{in}}) = \frac{\sum_{i=1}^N D_i + \frac{C_1, \text{nom}}{C_2, \text{nom}} D_{\text{ext}}(V_{\text{count}})}{N}. \quad (9)$$

Since the actual value of the capacitance ratio C_1/C_2 is not exactly known it is approximated by its nominal value. This can be modeled by an additive error as well:

$$\frac{C_1, \text{nom}}{C_2, \text{nom}} = \frac{C_1}{C_2} + \varepsilon_{\text{ratio}}. \quad (10)$$

Then the digital output $D(V_{\text{in}})$ can be rewritten as

$$\begin{aligned} D(V_{\text{in}}) &= \frac{\sum_{i=1}^N D_i + \left(\frac{C_1}{C_2} + \varepsilon_{\text{ratio}} \right) (V_{\text{count}} + \varepsilon_{\text{ext}})}{N} \\ &= V_{\text{in}} + \underbrace{\frac{\varepsilon_{\text{ratio}} D_{\text{ext}}(V_N)}{N} + \frac{C_1}{C_2} \frac{\varepsilon_{\text{ext}}}{N}}_{\text{ADC error}} + O\left(\frac{\varepsilon^2}{N}\right). \end{aligned} \quad (11)$$

This equation indicates the main properties of the extended counting conversion technique. The first and most important property is that both errors $\varepsilon_{\text{ratio}}$ and ε_{ext} are divided by N , the number of counting steps. However, the error due to the extended conversion is multiplied by the capacitor ratio C_1/C_2 . Together with (2) this introduces a trade-off for this coefficient. To reduce the error contribution due to the extended conversion, the ratio C_1/C_2 should be large. To assure that the integrator output remains sufficiently small, this ratio should not be too large. For our prototype we want an input voltage range close to rail-to-rail. Since the integrator output voltage is bounded by the power rails, (2) implies that $C_1 \geq 2C_2$.

B. Extended Conversion

During the extended conversion, the system functions as an algorithmic A/D converter [6]. Here, every step takes only one phase. The circuit configuration during both odd and even phases is shown in Fig. 3. Here the capacitors C_2 , C_3 and C_4 are nominally equal. Both the comparator and the operational amplifier are the same as for the counting conversion.

To understand the basic operation, we shall first discuss the even phase. If i is an even number, then at the beginning of the

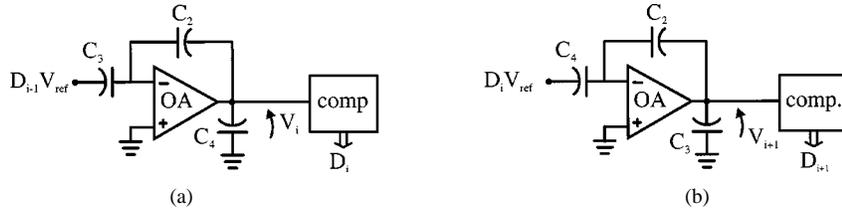


Fig. 3. Circuit configuration during an odd and an even step of the extended conversion. (a) Even phase. (b) Odd phase.

i th phase the capacitors C_2 and C_3 are charged with the output voltage V_{i-1} of the previous (odd) phase. The capacitor C_2 is in the feedback loop of the operational amplifier. The top plate of the capacitor C_3 is switched toward the inverting input node of the opamp and its bottom plate is switched to $+$ or $-V_{\text{ref}}$ depending on the previous value of the code D_{i-1} . This way we obtain the output voltage V_i :

$$V_i = \left(1 + \frac{C_3}{C_2}\right) V_{i-1} - D_{i-1} \frac{C_3}{C_2}. \quad (12)$$

Here again V_{ref} is set equal to 1. Because C_2 and C_3 are nominally equal, this simplifies to:

$$V_i \approx 2V_{i-1} - D_{i-1}. \quad (13)$$

This voltage is available over the capacitor C_4 that is connected to the opamp output, and over the feedback capacitor C_2 . At the end of this even phase the comparator is strobed to generate the code D_i .

For the operation during the succeeding odd phase the role of the capacitors C_3 and C_4 is interchanged Fig. 3. For the rest the operation is equivalent to the operation during the even phase. Therefore, (13) holds for odd phases as well. At the beginning of the extended conversion, the voltage V_{count} must be sampled on the capacitors C_2 and C_4 to initialize the algorithm. If the total of steps in this extended conversion equals M then this recursion formula can be solved for V_{count} :

$$V_{\text{count}} \approx \sum_{j=1}^M 2^{-j} D_{J+N}. \quad (14)$$

Therefore $D_{\text{ext}} = \sum_{j=1}^M 2^{-j} D_{J+N}$ can indeed be considered as a suitable digital approximation of V_{count} .

It is well known that the accuracy of this algorithmic conversion is limited by mismatch of the nominally equal capacitors C_2 – C_4 [6]–[9]. This was modeled by the additive error term ε_{ext} in (8). Although the accuracy for the overall A/D converter is bootstrapped by the number of steps in the counting conversion, good capacitor matching is still important, because this allows us to obtain the same accuracy with a smaller number of counting steps.

C. Three-Level Quantizer

In the discussion of both the counting as well as the extended conversion, both the comparator and the operational amplifier were assumed to be ideal. However, any practical realization of these circuits inevitably suffer from an offset voltage. The counting conversion is based on a first-order $\Sigma\Delta$ modulator which is known to be tolerant toward offset effects. However,

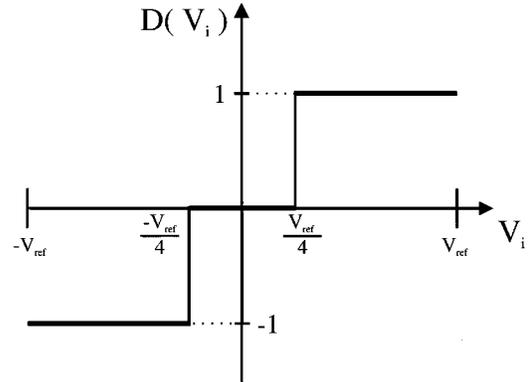


Fig. 4. Input–output characteristic of the three-level comparator bank.

the extended conversion is an algorithmic conversion. Here comparator and operational amplifier offset cause nonlinearity. In addition, operational amplifier offset results in an overall input-referred offset [8]. While this input-referred offset can be tolerated in most applications, the nonlinearity error cannot. The simplest way to solve this problem is to use two comparators instead of just one [6], [8]. For maximum tolerance toward offset, the comparator thresholds should be $-V_{\text{ref}}/4$ and $+V_{\text{ref}}/4$. Then the code D_i can take the values -1 , 0 , and 1 (Fig. 4). This implies that in the circuit of Fig. 3, the input capacitor C_3 or C_4 must be switched toward $D_i V_{\text{ref}}$, i.e., 0 or $\pm V_{\text{ref}}$. In a fully differential circuit implementation, this function is readily available [5], [8], [11], [12].

To reduce the power consumption and the chip area, the same comparators must be used both in the counting and extended conversion. With this three-level comparator-bank the output voltage of the integrator during the counting conversion is reduced and the bounds of (2) are relaxed. This can be exploited in two possible ways. The first way is to decrease the coefficient C_1/C_2 to enhance the linearity performance. The second strategy is to keep the same value of C_1/C_2 . This way the requirements for the operational amplifier's output voltage range are reduced. In this low-voltage design, the second approach is followed and C_1 is set nominally to $2C_2$.

D. Architectural Choices

In the target process for our design, capacitors can be matched up to 10- or 11-b accuracy. However, the application requires better than 12-b linearity. Therefore, the counting conversion should relax the accuracy requirements on the extended conversion with at least a factor 4. Since $C_1 = 2C_2$ it can be concluded from (11) that the number of counting steps N should be at least eight to obtain 12- to 13-b linearity.

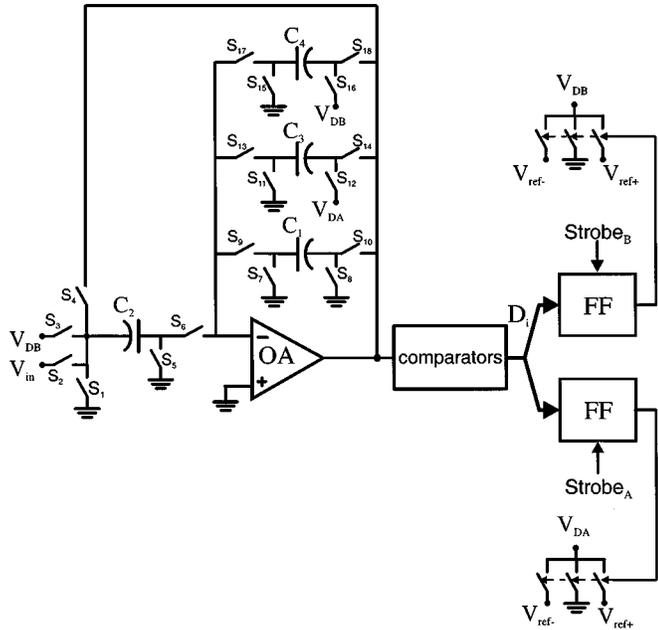


Fig. 5. Single-ended schematic of the overall A/D converter.

To improve this by one more bit, the approach is refined as follows [13]. First it is observed that the input voltage range of the algorithmic conversion is $[-V_{\text{ref}}, +V_{\text{ref}}]$. However, with our choice of $C_1 = 2C_2$ it is concluded from (6) that the voltage range of V_{count} would occupy only half this range. Since we employ a three-level instead of a two-level quantizer, the actual voltage range is even less. Therefore, the voltage V_{count} can be amplified by a factor C_1/C_2 to initialize the algorithmic conversion. Following a similar reasoning as in Section II-B it can be shown that the digital output $D(V_{\text{in}})$ now equals

$$D(V_{\text{in}}) = V_{\text{in}} + \frac{\varepsilon_{\text{ext}}}{N}. \quad (15)$$

In our case, where nominally $C_1 = 2C_2$, the nonlinearity error term is reduced by a factor 2 compared to (11). This is confirmed by behavioral simulations.

Based on these considerations, the number of counting steps N was chosen equal to 8. This takes $8 + 1 = 9$ clock cycles. Then the number of extended steps M was set equal to 12, which takes six clock cycles. The amplification with the factor C_1/C_2 to initialize the extended conversion also takes one clock cycle. One complete A/D conversion then takes a total of 16 clock cycles. This gives the analog part of the circuit a complexity comparable to a first-order $\Sigma\Delta$ modulator that operates at an oversampling ratio of 16. Behavioral simulations confirm that with these choices of N and M even under worst-case matching conditions better than 13-b linearity can be obtained.

A single-ended schematic of the overall A/D converter is shown in Fig. 5. A timing diagram of all the switch drive signals is shown in Fig. 6.

E. Non-DC Input

When the input signal is not constant, (5) is no longer valid. Instead it should be replaced by

$$V_{\text{count}} = \frac{C_2}{C_1} \sum_{i=0}^{N-1} \left(V_{\text{in}} \left(t_0 + i \frac{T}{N_{\text{tot}}} \right) - D_i V_{\text{ref}} \right). \quad (16)$$

Here t_0 is the nominal sampling instance and N_{tot} is the total amount of clock cycles that is required for one complete extended counting A/D conversion. Together with (9) this gives for the overall digital output D

$$D = \frac{\sum_{i=0}^{N-1} V_{\text{in}} \left(t_0 + i \frac{T}{N_{\text{tot}}} \right)}{N}. \quad (17)$$

Here, the error contributions ε_{ext} and $\varepsilon_{\text{ratio}}$ are neglected. This nonuniform sampling gives an additional constant-delay filter effect. For our prototype, the number of clock cycles N during the counting conversion equals 8 and the total amount of clock cycles N_{tot} is 16. The magnitude of the corresponding A/D converter frequency response is shown in Fig. 7. It is clear from the plot that this filter effect is quite modest in the Nyquist band. If needed, it can easily be corrected by a simple digital filter.

III. CMOS IMPLEMENTATION AT 1.2 V

A. Controller Logic

The system described in the previous section requires a digital controller to generate the appropriate switch signals. It is implemented as a synchronous automata that operates at twice the clock frequency of the switched-capacitor circuits. All this logic is implemented with standard cells of a 5- to 3.3-V library that are used far beyond their specification at 1.2 V. It turns out that the speed of these cells is reduced significantly, but for this voice-band application this is not a problem.

B. Switches

A well-known problem for low-voltage switched-capacitor circuits is the conductance of the switch. This is due to the fact that the gate overdrive voltage inevitably is very low in a low-voltage circuit.

One method to solve this problem is to generate a higher voltage on the chip to drive the gates of the switch transistors [5], [14]–[18]. This technique provides a simple means to use all conventional switched-capacitor techniques at a reduced supply voltage. A drawback of this approach may be the reduced reliability. This is greatly reduced but not completely solved by using bootstrapping techniques [16]–[18].

Another approach is the use of switched-opamp techniques [3], [4], [19]–[22]. Here the signals are not switched themselves. Instead the entire opamp that drives the signal node is switched off. This can be achieved by a simple nMOS switch in series with the negative supply rail or a pMOS switch in series with the positive supply. Therefore no higher voltages are needed on the chip and no reliability problem occurs. However, to achieve a reasonable input-voltage range, a switched input buffer is needed [20]. Next to this, the switched opamp technique imposes several other restrictions. Therefore, here it is chosen to generate a higher on-chip voltage with an integrated charge pump [15]. Since the prototype circuit is designed in a 5-V capable CMOS process, reliability is not a problem here.

First, the conductance of a single nMOS switch with a $2-V_{\text{dd}}$ gate drive voltage was investigated. It turned out that under worst-case process conditions ($V_{Tn, \text{max}} = 850$ mV) even this

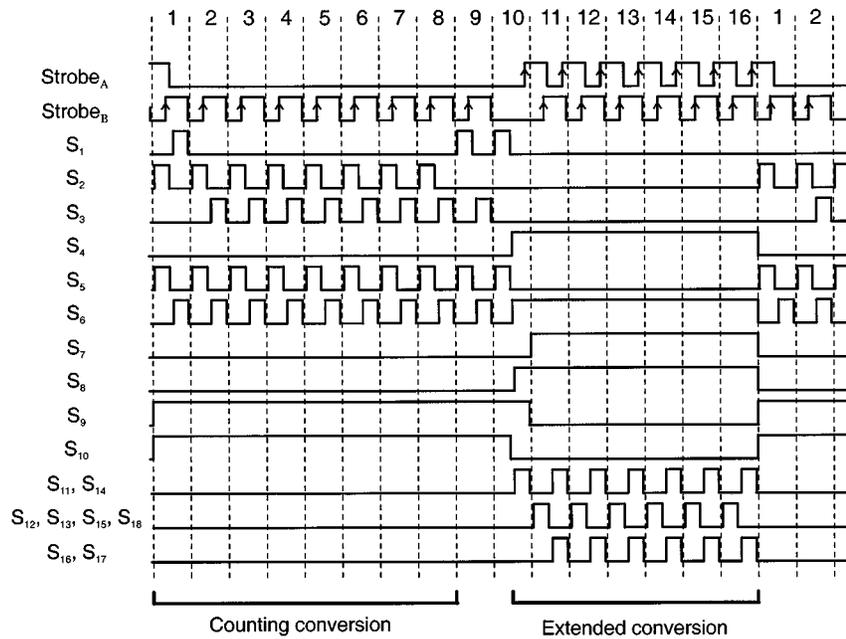


Fig. 6. Timing diagram for the extended counting A/D converter.

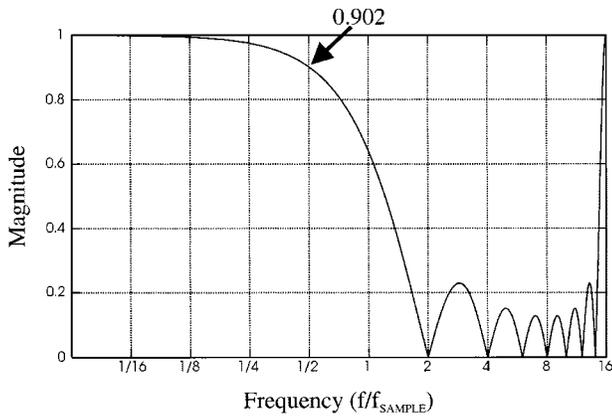


Fig. 7. Frequency response of the designed A/D converter.

gate drive voltage was not high enough to assure adequate conductance over the entire signal range. Therefore, a $\times 3$ charge pump was chosen.

Instead of using one charge pump for each switch as in some previously reported low-voltage designs [14], we used one large charge pump to generate the $3\text{-}V_{dd}$ voltage on the chip. A switch selection signal (1.2-V logic) is then applied to a level shifter circuit to generate the “stronger” selection signal (at about 3.6 V) to drive the gate of the nMOS switch transistor [15]. This level shifter is powered by the charge pump (see Fig. 8).

C. Operational Amplifier

The operational amplifier schematic is shown in Fig. 9. It is a rather conventional two-stage design with a modified Miller compensation [24]. The second stage is a common-source stage. This is needed to maximize the output swing. The first stage is a folded cascode to achieve a high dc-gain. Both the input differential-pair transistors and the common-source output transistors are biased in weak inversion.

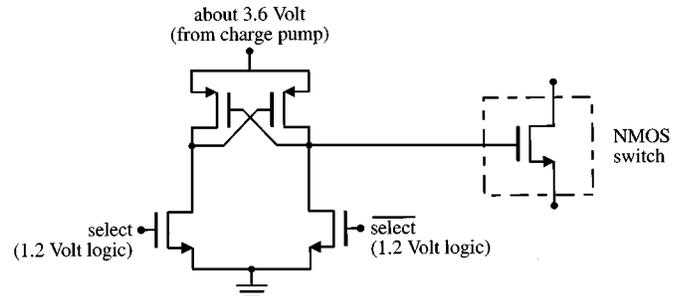


Fig. 8. Switch driver circuit.

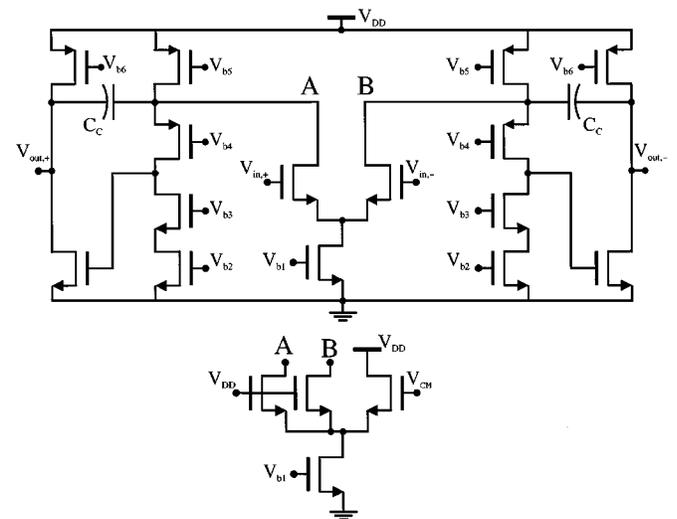


Fig. 9. Operational amplifier schematic.

Unlike several previously reported low-voltage designs where a pMOS input stage is employed [3], [4], [21], an nMOS input stage is used here. If a pMOS input stage is used, the opamp input common-mode voltage must be close to the

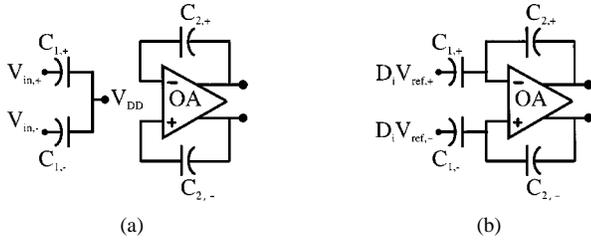


Fig. 10. Fully differential equivalent of the circuit of Fig. 1 with a proper opamp input common-mode voltage. (a) First phase. (b) Second phase.

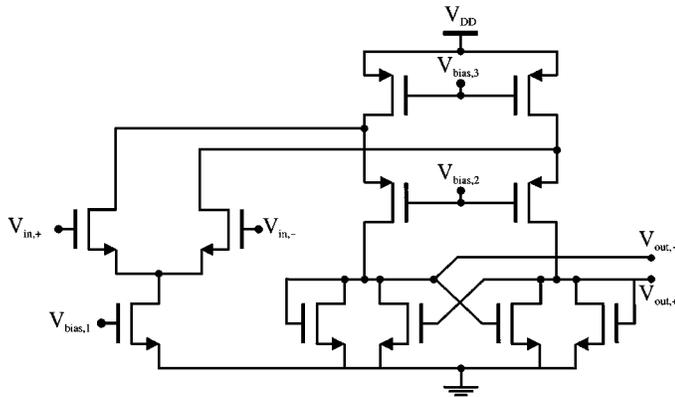


Fig. 11. Comparator pre-amplifier schematic.

negative rail in a low-voltage circuit. This means that voltage spikes during transients could cause the opamp input nodes to go beneath the negative rail. The p-type substrate is connected to this negative rail. In combination with the drains of the nMOS switches that are connected to the opamp input nodes, the substrate forms a pn-junction diode that would be forward biased [21]. Both during the counting and extended conversion, large voltage spikes can occur. Therefore, the pMOS input stage is avoided and an nMOS input stage is used instead. The input common-mode voltage is set equal to the positive supply rail. The configurations of Figs. 1–3 can easily be adapted to achieve this. Fig. 10 shows the modification for the fully differential equivalent of Fig. 1. The only difference is that during the sampling phase, the top plates of the capacitors $C_{1,+}$ and $C_{1,-}$ are switched to the positive supply rail instead of to the signal common-mode voltage. The modification for the configurations of Figs. 2 and 3 is similar.

The common-mode feedback is injected on the nodes *A* and *B* by an additional differential pair. The common-mode voltage is sensed by a switched-capacitor voltage divider.

D. Comparator

The comparator consists of a pre-amplifier followed by a latch. The pre-amplifier schematic is shown in Fig. 11. It is a differential pair with a folded cascode loaded with cross-coupled nMOS mirrors. This circuit combines a large differential voltage gain with a stabilization of the output common-mode voltage [22], [23]. Again, an nMOS input stage is used. Proper operation of this input stage is achieved by capacitively coupling the input common-mode voltage and the threshold voltage [6]. As shown in Fig. 12, this can be done in two phases. In the first phase, the comparator input common-mode voltage and the

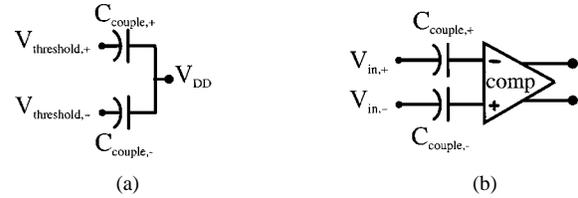


Fig. 12. Reset and comparison phase of the capacitively coupled comparator. (a) Reset phase. (b) Comparison phase.

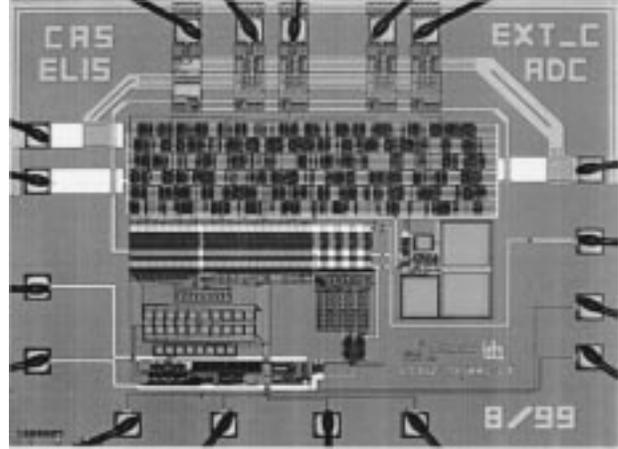


Fig. 13. Chip microscope photograph.

comparator threshold voltage are sampled on the coupling capacitor. The comparator threshold voltage is generated by a capacitive voltage divider. Fig. 12 shows only the Thévenin equivalent of this. In a second phase, the differential input voltage is applied.

IV. EXPERIMENTAL RESULTS

The above-described techniques were implemented in an experimental prototype. A standard $0.8\text{-}\mu\text{m}$ CMOS process with typically $V_{T,N} = 0.75\text{ V}$ and $V_{T,P} = 0.75\text{ V}$ was used. A microscope photograph of the chip is shown in Fig. 13. The large rectangular structure at the upper side of the core is the controller logic. Underneath the logic is a row with the level-shifters and switches. Also, the large capacitors of the integrated charge pump are visible in the middle right. The opamp and the capacitors are located in the bottom left. The comparators are in the center. It is clear that no attempt was done to optimize the layout at this stage. The reason for this is that the circuit is already smaller than the minimum “Europractice” chip size for this process. The core area including all logic is only about $1.3 \times 1\text{ mm}^2$. For comparison purpose, in a comparable process ($1\text{-}\mu\text{m}$ CMOS) the decimation filter that is required additionally to obtain a complete $\Sigma\Delta$ modulation A/D converter occupies 2.4 mm^2 [25].

The measurements reported here were performed with a 1.2 V supply voltage at a 16-kHz Nyquist sampling rate. This corresponds with an analog clock frequency of 256 kHz . The differential reference voltage was set equal to the power supplies, which corresponds to a rail-to-rail input signal range ($\pm 1.2\text{-V}$ differential). Dynamic measurements were done by applying a sinusoidal signal at the input of the converter. Fig. 14 shows a typical 1024-pt fast Fourier transform (FFT) result for

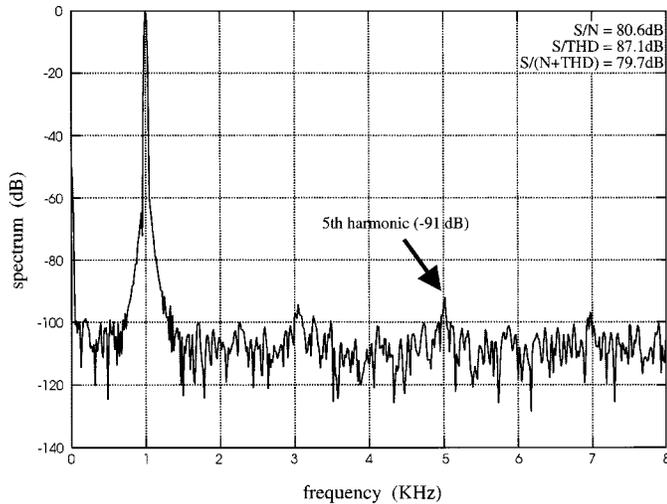


Fig. 14. Measured ADC output spectrum (1024-pt FFT).

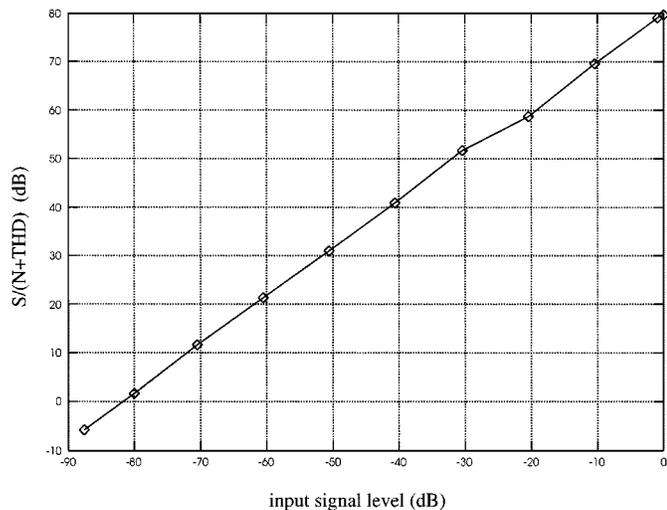


Fig. 15. Measured $S/(N + THD)$ ratio versus input amplitude.

a -0.1 -dB input signal of about 1 kHz. The $S/(N + THD)$ ratio here is 79.7 dB. The largest harmonic is the fifth (-91 dB). No even harmonic distortion is observable. This confirms that the three-level operation of the $\Sigma\Delta$ modulator during the counting conversion occurs with a very high accuracy. The $S/(THD)$ ratio is 87.1 dB (harmonics 2 to 14). The corresponding signal-to-noise (S/N) ratio is 80.6 dB. Fig. 15 shows the $S/(N + THD)$ ratio vs the input level. The dynamic range is 82 dB which is better than 13-b performance. This agrees well with qualitative kT/C noise calculations for the unit capacitance value of 3 pF. The use of these relatively large capacitors also gives a large tolerance toward charge injection of the switches which had minimum size. More detailed circuit-level noise simulations where also the noise of the opamps was taken into account, predicted a dynamic range of about 83 dB, which is very close to the measured value.

The power consumption of the analog blocks is $100 \mu\text{W}$. About $60 \mu\text{W}$ is consumed by the operational amplifier, $20 \mu\text{W}$ by the comparators and $20 \mu\text{W}$ by bias circuitry. All these circuits were designed very conservatively. A less conservative de-

TABLE I
MEASURED PERFORMANCE

Technology	$0.8 \mu\text{m}$ CMOS (2M2P)
Supply Voltage	1.2 V
Clock Frequency	256 KHz
Sample-frequency	16 KHz
Power consumption	$150 \mu\text{W}$
Peak $S/(N+THD)$	80 dB
Dynamic range	82 dB
Input range	rail to rail
Core area	$1.3 \times 1 \text{ mm}^2$

sign would result in an even lower power consumption. The digital circuits, including the charge pump and the level-shifter consume $50 \mu\text{W}$ at a sample rate of 16 kHz. This unexpected large power drain, turns out to be due to short currents in the level shifters for the switches (Fig. 8). These are driven by undersized buffers. By an appropriate redesign also this could further be reduced. The measured performance is summarized in Table I.

V. CONCLUSION

This paper has investigated the extended counting technique [1] for a low-voltage micropower voice-band A/D converter. It is shown that this technique is capable of realizing a high resolution that is competitive with $\Sigma\Delta$ modulation. The analog part of the design presented here is comparable to a first-order $\Sigma\Delta$ modulator working at an oversampling ratio of 16. In addition, the digital control and reconstruction logic is considerably less complex than the decimation filter that is required for a $\Sigma\Delta$ modulator.

The experimental results prove state-of-the-art performance with excellent linearity. At a 1.2-V power supply and a 16-kHz Nyquist sampling rate, the design features a peak $S/(N + THD)$ of 80 dB, a dynamic range of 82 dB, and a power consumption of $150 \mu\text{W}$.

ACKNOWLEDGMENT

The authors wish to thank Dr. L. V. Immerseel of the University of Antwerpen for introducing them to the problem area.

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