Efficiency Optimization of a Step-Down Switched Capacitor Converter for Subthreshold Applications

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***Abstract*— In this brief, an efficient voltage scalable switched capacitor converter (SCC) for 1.1 V battery-powered digital system is presented. The SCC employs a binary resolution technique to preserve high efficiency at load voltages down to sub-200 mV while keeping the efficiency high. The proposed converter can be configured into four topologies to support subthreshold output levels of 0.18–0.6 V. The converter is designed in a standard lowpower 40-nm CMOS TSMC process. Simulation results show that the efficiency of the SCC can be improved by 10%–11% in the vicinity of $V_{DD} = 200$ mV as compared to one using a conventional approach. An optimization strategy for designing multi-topology SCC is presented to improve the effectiveness of the circuit and to preserve efficiency over large load voltages.**

***Index Terms*— Dc–dc power converter, design optimization, low-power electronics, subthreshold design, switched capacitor circuits.**

I. Introduction

The growing quest for power-saving techniques in digital systems has raised the need for an integrated dc–dc converter which is compatible with subthreshold operation levels [1]. To minimize power dissipation in ultra low power systems, the dc–dc converter needs to supply variable subthreshold load voltages [2]. Switched capacitor converters (SCCs) have become very attractive for battery-operated systems because they can minimize the number of off-chip components and have the flexibility in sizing switches and capacitors. The challenge associated with the realization of an efficient low-voltage and ultralow-power SCC has led to several recent developments [3]–[5]. These studies have shown that the efficiency of multiple-conversion-ratio SCCs can be effectively maintained over wider input voltage range than a single topology converter. It is shown that a combination of two standard divide-by-2 SCC cells can support two additional topologies, which provide two-third and one-third conversion ratios [6]. This circuit and its variants have been systematically designed in numerous studies, utilizing one or more of its possible conversion ratios. The use of a reconfigurable array of capacitors to support a large range of load voltages of 0.3–1.1 V from a 1.2-V battery is presented in [7]. They suggest an SCC consisting of 13 charge-transfer switches and an additional topology switches to realize five conversion ratios $G = \{1/3, 1/2, 2/3, 3/4, 1\}$. An adaptive-body-bias SCC for powering light loads with output voltages of 0.3–0.4 V from a 1–1.2-V input source has been demonstrated in [8], while supporting a $G = 1/2$ conversion ratio.

Because of the unavoidable loss mechanism, it is clear that the main challenge in SCC design is the optimization of the converter parameters while meeting various constraints on efficiency, silicon area, and output voltage V_{DD}. If, for instance, a traditional design approach is adopted, such as sizing the switches of the SCC to the same $R_{ds(on)}$ or, alternatively, adjusting it to allow operation in the complete charge-transfer mode, one might end up with a nonoptimal design. For example, an earlier brief [9] that implemented SCC with $G = 2/3$ conversion ratio also confirms this point.

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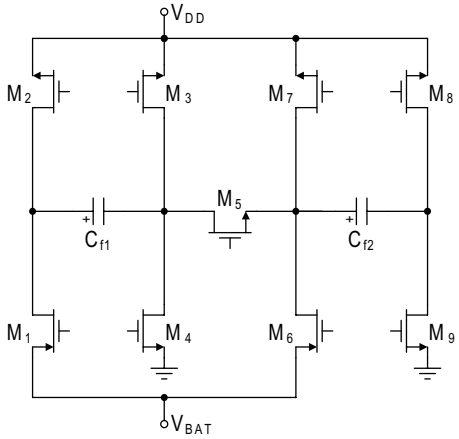

Fig. 1. Conventional 9 switch SCC with three conversion ratios $G = \{1/3, 1/2, 2/3\}$.

Motivated by the above concerns, this brief presents a novel optimization procedure of a 40-nm 1.1-V CMOS voltage-scalable SCC which is suitable for mobile subthreshold applications supporting output levels of 0.18–0.6 V. The core of the proposed circuit is a classical SCC shown in Fig. 1. This circuit is composed of nine switches and two flying capacitors to support three conversion ratios (this topology denoted henceforth as conventional SCC).

Since the proposed SCC is supposed to work over four different topologies, it is hard to define a single optimized operating point that can constitute an optimization criterion for all topologies. Therefore, this brief outlines an optimization methodology of a multiobjective optimization approach. Furthermore, the proposed optimization technique takes into account nontrivial design parameters.

II. Proposed Switched Capacitor Converter

It is well established that any SCC can be modeled with an equivalent no-load voltage source connected in a series with an equivalent resistor R_{eq}. The maximum theoretical efficiency of the SCC for a given conversion ratio G can be expressed by

$$\eta_{max} = \frac{V_{DD}}{G \cdot V_{BAT}} = \frac{R_L}{R_L + R_{eq}} \tag{1}$$

where V_{DD} and V_{BAT} are the loaded output and input battery voltages, respectively and R_L is the load resistance. A more accurate representation of (1) will be with all loss contributors

$$\eta = \frac{P_L}{P_L/\eta_{max} + P_{BP} + P_{Drive} + P_{Leak} + P_{Control}} \tag{2}$$

where P_L, P_{BP}, P_{Drive}, P_{Leak}, and $P_{Control}$ are, respectively, the output power, the bottom-plate parasitic-capacitor-related losses, the gate drive loss, the power consumption due to leakage current, and the power lost in the control circuitry.

In practice, employing the circuit of Fig. 1 and using the smallest possible ratio of $G = 1/3$, it follows from (1) that for $V_{DD} = 0.2$ V, the obtainable efficiency is limited to 54%. It would appear that a conversion ratio of $G = 1/4$ can be realized by cascading two divide-by 2 SCCs in order to increase the efficiency up to 73%. However, this requires an additional number of power switches that need to be considered.

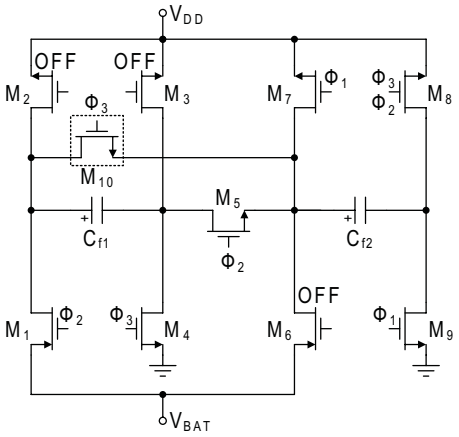

Fig. 2. Proposed 10 switch SCC with four conversion ratios $G = \{1/4, 1/3, 1/2, 2/3\}$. With gain setting of $G = 1/4$, the switches M_2, M_3, M_6 are in off state, while the remaining switches are clocked by a 3 phase timing template $\{\Phi_1, \Phi_2, \text{and } \Phi_3\}$.

Since the aim of the brief is to provide sizing methodology for the power-stage components, it is assumed that the power consumption due to control circuits is negligible. In practice, the losses of the control can be estimated by the following expression [7]:

$$P_{\text{Control}} = N_G C_{\text{avg}} V_{\text{BAT}}^2 f_{\text{sw}} + I_{\text{Leak}} V_{\text{BAT}} + I_{\text{DD}} V_{\text{BAT}} \quad (3)$$

where, N_G is the number of gates, C_{avg} is the average capacitance switched in the control circuitry every cycle, I_{Leak} is the total leakage current consumed by the control circuit, and I_{DD} represents the current consumption due to the analog blocks and the static bias current inside the digital modules. It has been reported that the control losses can be kept less than 15 μW at a switching frequency of 30 MHz and load power of 4.93 mW [10].

A. Approach

The configuration of the proposed power stage converter is depicted in Fig. 2. This circuit consists of a conventional SCC (Fig. 1) and an additional switch M_{10}. The SCC is designed to implement four different conversion ratios, excluding the trivial case $G = 1$. The reader is referred to [4] and [6] for a detailed analysis of the ordinary conversion ratios and their corresponding topologies. When the circuit is supposed to operate with $G = 1/4$, essentially it consists of three subcircuits extended over three nonoverlapping time sessions $\{\Phi_1, \Phi_2, \Phi_3\}$. Readers are referred to [5] for more in-depth treatment of the three-phase clock generation circuits. Following the theory in [3], the subcircuits of the SCC can be represented by an equivalent system of linear equations. Designating the voltages across C_{f1} and C_{f2} by V_{C1} and V_{C2}, the system of linear equations is composed as follows:

$$\begin{pmatrix} 1 & 0 & -1 \\ 1 & 1 & 1 \\ 1 & -1 & 1 \end{pmatrix} \cdot \begin{pmatrix} V_{DD} \\ V_{C1} \\ V_{C2} \end{pmatrix} = \begin{pmatrix} 0 \\ V_{BAT} \\ 0 \end{pmatrix}. \quad (4)$$

The solution of (4) is $V_{\text{DD}} = (1/4)V_{\text{BAT}}$, $V_{\text{C1}} = (1/2)V_{\text{BAT}}$, and $V_{\text{C2}} = (1/4)V_{\text{BAT}}$.

B. Architecture

The block diagram architecture of the considered SCC is shown in Fig. 3. Apart from the SCC circuit, all control blocks were implemented with the Verilog-A language. The SCC block contains the flying capacitors (C_{f1}, C_{f2}) and the power switches, as shown in Fig. 2. The gain selection block activates one of the four topologies, depending on the proximity of its target voltage to the load voltage being delivered and its ability to provide the load power demand. The converter uses the hysteretic mode control to maintain the feedback voltage V_{DD} within the hysteretic band of $\pm\Delta V$, where ΔV is set to 10 mV. In this way, the converter remains idle until the output voltage falls below $V_{\text{REF}} - \Delta V$. At this point, the output of the comparator V_{comp} switches to a high state and thereby enables the SCC to transfer charge packets to the load.

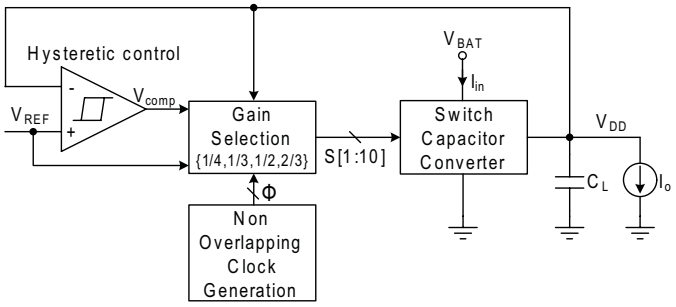

Fig. 3. Block diagram of the Hysteretic mode control regulated SCC.

TABLE I
1ST OPTIMIZATION OF SCC PARAMETERS

Optimized Parameter	Optimization Range (MIN:STEPS:MAX)	Final Value
W_{OPT}	1 μm:30:400 μm	268.6 μm
$m_{\text{f1}} = m_{\text{f2}}$	1:30:400	328.8
k	0.0001:30:0.1	2.043 m

The parameter W_{OPT} represents the width of the switches when all share the same optimized value. The parameters $m_{\text{f1}} = m_{\text{f2}}$ define the number of 1.14 pF @ 1.1 V nMOS capacitors connected in parallel to implement the flying capacitors $C_{\text{f1}} = C_{\text{f2}}$. The parameter k is a design variable of the rise/fall/dead times as explained in Section III.

III. OPTIMIZATION

The proposed circuit was tested and characterized in a standard low-power 40-nm TSMC CMOS process. To avoid a short channel effect, the channel length was set three times larger than the minimum technology L_{min} namely, $L = 120$ nm. The widths of the switches and additional parameters were adjusted by a global optimization procedure using a parallel simulated annealing algorithm. Depending on the end application and technology (e.g., CMOS, SOI), practical low-voltage loads of integrated SCC designs range between 100 nW [8] and several milliwatts [10]. The proposed SCC was designed to deliver a typical load current of $I_{\text{o}} = 1$ mA with high efficiency over 0.18 V $\leq V_{\text{DD}} \leq$ 0.6 V. A global optimization was performed by evaluating the average efficiency and unregulated output V_{DD} over a range of switches' widths and flying capacitors $C_{\text{f1}} = C_{\text{f2}}$, until the system specifications were satisfied. Here we note that the fall/rise and dead times of the gating signals are accessible within the Verilog-A controller. So, during the optimization these parameters were set for simplicity to be proportional to f_{sw} as, $t_f = t_r = k/f_{\text{sw}}$, and $t_{\text{dt}} = 2k/f_{\text{sw}}$, where k was fed to the optimization as a designable parameter. The parameter k was included in order to emphasize the correlation that exists between the gating signal waveform and the inherent losses of the converter.

The optimization procedure was conducted using the following assumptions and conditions.

1) All losses are considered except the losses of the control circuit. As matter of fact, the larger the output power, the more it is justified to assume that the control circuitry losses are negligible compared with major loss factors [5].

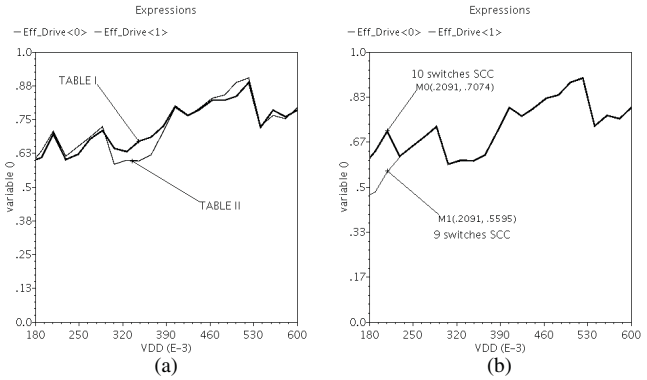

Fig. 4. SCC efficiency versus load voltage V_{DD} over 0.18 V $\leq V_{DD} \leq$ 0.6 V for $I_o = 1$ mA. (a) Comparison between 1st (I) and 2nd (II) optimizations. (b) Comparison between 9 switches SCC (conventional circuit without M_{10}) and 10 switches SCC (proposed circuit) using the results of the 2nd optimization.

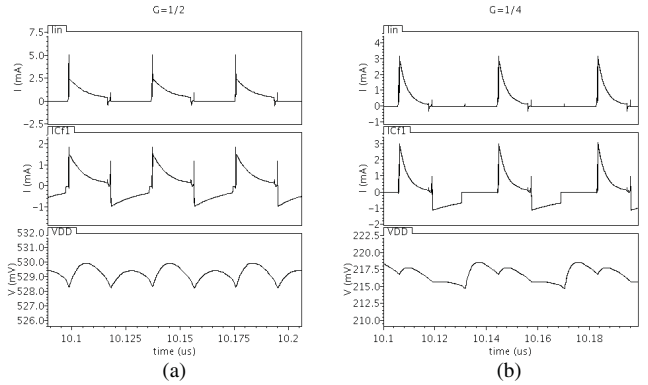

Fig. 5. Open loop key waveforms of the SCC at $I_o = 1$ mA. Traces from top to bottom i_{in}, i_{Cf1}, V_{DD} for (a) $G = 1/2$ and (b) $G = 1/4$.

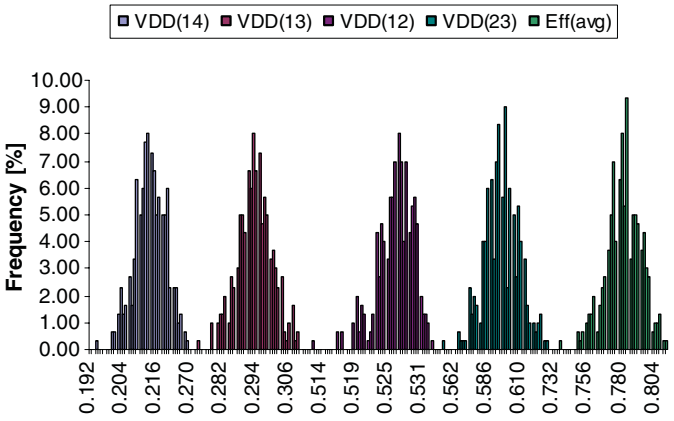

Fig. 6. Monte Carlo statistical distributions in a 3000 point simulation at $I_o = 1$ mA. From left to right: $V_{DD(14)}$, $V_{DD(13)}$, $V_{DD(12)}$, $V_{DD(23)}$, η_{avg} with $\{\mu_{14} = 0.213,\ \sigma_{14} = 5.68$ mV$\}$, $\{\mu_{13} = 0.293,\ \sigma_{13} = 6.27$ mV$\}$, $\{\mu_{12} = 0.526,\ \sigma_{12} = 3.32$ mV$\}$, $\{\mu_{23} = 0.593,\ \sigma_{23} = 12.52$ mV$\}$, $\{\mu_{\eta} = 0.778$, and $\sigma_{\eta} = 12.75$ m$\}$.

2) The switching frequency f_{sw} was set for simplicity to a fixed value of $f_{sw} = 26$ MHz. Although the switching frequency can also be included as optimization variable, it will increase the optimization time considerably. To scale down the size of the flying capacitors and switches, one should strive to select an initial f_{sw} as high as possible while keeping the losses of the control circuitry $P_{Control}$ (3) a reasonable fraction of the total output power P_L.
3) The SCC was implemented with low-V_t MOS transistors of the process library.
4) The output capacitor (Fig. 3) was set to $C_L = 3.2$ nF to fulfill a requirement of $\Delta_{ripple} = 12$ mV maximum output ripple by the relation $C_L = I_o/(\Delta_{ripple} f_{sw})$ [9]. Note that the hysteretic band $\pm\Delta V = \pm 10$ mV is the regulated output ripple, while the Δ_{ripple} is the unregulated output ripple when the output of the comparator V_{comp} is maintained in high state (Fig. 3). The situation $V_{comp} = 1$ occurs when the SCC reaches the maximum output voltage V_{DD} of a given topology.

Each designable parameter was constrained to take values from a limited range. The performance function of the circuit is the average efficiency of the four topologies defined as

$$\eta_{avg} = \frac{\eta_{14} + \eta_{13} + \eta_{12} + \eta_{23}}{4} \tag{5}$$

where η_{14}, η_{13}, η_{12}, and η_{23} are the efficiencies of topologies $G = \{1/4, 1/3, 1/2, 2/3\}$, respectively. The efficiencies were evaluated at a maximum current of $I_o = 1$ mA and with the corresponding unregulated output voltages (open-loop control). Unregulated output voltage is the obtainable steady-state output voltage of a topology, while the output of the comparator V_{comp} (Fig. 3) is maintained in a high state. The average efficiency η_{avg} and the four efficiencies at the respective unregulated maximum output voltages were constrained to satisfy the following:

$$75\% \leq \eta_{avg} \leq 85\% \tag{6}$$

and simultaneously

$$\begin{aligned} V_{DD(14)} &\geq 0.2V; \quad \eta_{14} \geq 60\% \\ V_{DD(13)} &\geq 0.3V; \quad \eta_{13} \geq 60\% \\ V_{DD(12)} &\geq 0.5V; \quad \eta_{12} \geq 60\% \\ V_{DD(23)} &\geq 0.6V; \quad \eta_{23} \geq 60\% \end{aligned} \tag{7}$$

while letting the optimizer engine to choose values such that the SCCs comply with constraints (6) and (7). The optimization procedure is summarized as follows:

Optimized Variables: 1) Proportionality factor k of the gating signals; 2) the widths of the switches W_i where $i = 1, 2, \ldots, 10$; and 3) the flying capacitors C_{f1}, C_{f2}.

Design Constraints: Equations (6) and (7).

Objective Function: Minimize the size of the switches and flying capacitors.

Using above constraints, two optimization sets were conducted in order to validate the method. In the first optimization, all widths of the power switches forced to the same size W_{opt} while the capacitors were imposed to $C_{f1} = C_{f2}$. It should be noted that this condition does not necessarily reflects the same $R_{ds(on)}$ of the switches. In the second optimization, the switches of the power stage were sized individually, while the parameter k was set to the same value as obtained in the first run in order to preserve same drive condition. The objective of the two optimizations sets was to evaluate the functionality of the SCC in terms of efficiency and size when two different strategies are used.

Table I summarizes the design variables involved in the first optimization procedure, the corresponding optimization ranges of legal values, and the final optimum values. The parameter STEPS defines number of unequally spaced values between MIN and MAX limits. The results of the second optimization over the same constraints ranges are $W_1 = W_6 = 264.6$ μm; $W_4 = W_9 = 115.8$ μm, $W_2 = 142.4$ μm; $W_3 = 325.3$ μm; $W_5 = 215.2$ μm; $W_7 = 144.4$ μm; $W_8 = 175.5$ μm; $W_{10} = 33.52$ μm;

TABLE II
COMPARISON WITH RECENTLY PUBLISHED STEP-DOWN SC DC-DC CONVERTERS

	This Brief	[6]	[7]	[8]	[10]	[11]
Technology	40 nm CMOS	32 nm SOI	65 nm CMOS	130 nm CMOS	45 nm CMOS	65 nm CMOS
Gain ratios	1/4, 1/3, 1/2, 2/3	1/3, 1/2, 2/3	1/3, 1/2, 2/3, 3/4, 1	1/2	2/3	1/2
No. of power switches	10	9	13	5	7	5
Flying capacitor C_f	2×371 pF (Integrated)	NA	Total 600 pF (Integrated)	2×200 pF (Integrated)	Total 534 pF (Integrated)	2×4.7 nF (off chip)
Output capacitor C_L	3.2 nF (off chip)	0	NA	2 nF (off chip)	700 pF (Integrated)	47 nF (off chip)
Active area	0.074 mm^2	0.378 mm^2	0.12 mm^2	0.13 mm^2	0.16 mm^2	0.074 mm^2 (switches only)
Components sizing method	Global optimization (simulation based)	Optimization at nominal point	Adjustable switches widths	NA	Adjustable switches widths	NA
No. of clock phases	2, 3	2 (32 interleaved SCC)	2	2	2 (2 interleaved SCC)	2
Max. switching frequency	26 MHz	~600 MHz	15 MHz	20 MHz	30 MHz	15 MHz
Output regulation method	Hysteretic	PFM	PFM	Hysteretic + body bias control	Hysteretic capacitance modulation + PFM	Hysteretic + ripple control
Input voltage	1.1 V	2 V	1.2 V	1 V–1.2 V	1.8 V	1 V
Output voltage	0.18 V–0.6 V	0.5 V–1.2 V	0.3 V–1.1 V	0.4 V	0.8 V–1 V	0.2 V–0.47 V
Max. output current	1 mA	NA	NA	NA	8 mA	10 mA
Max. output power	0.6 mW	200 mW	0.5 mW	0.125 mW	7.2 mW	4.7 mW
Peak efficiency	90.35% @ {$V_{DD} = 0.53$ V, $I_o = 1$ mA}	81% @ {$V_{DD} = 0.88$ V, $P_o = 0.16$ W}	77% @ {$V_{DD} = 0.5$ V, $P_o = 50$ μW}	74% @ {$V_{DD} = 0.4$ V, $P_o = 100$ μW}	69% @ {$V_{DD} = 0.987$ V, $I_o = 5$ mA}	87% @ {$V_{DD} = 0.47$ V, $I_o = 1$ mA}
Ideal efficiency η_{max} calculated by (1)	96.4% @ {$V_{DD} = 0.53$ V, $G = 1/2$}	88% @ {$V_{DD} = 0.88$ V, $G = 1/2$}	83.3% @ {$V_{DD} = 0.5$ V, $G = 1/2$}	80% @ {$V_{DD} = 0.4$ V, $G = 1/2$}	82.25% @ {$V_{DD} = 0.987$ V, $G = 2/3$}	94% @ {$V_{DD} = 0.47$ V, $G = 1/2$}

$m_{f1} = m_{f2} = 325.3$. The parameter W_i corresponds to the width of the switch M_i where $I = 1, 2, \ldots, 10$.

IV. SIMULATION RESULTS

The SCC was implemented and simulated using the Cadence Spectre simulator. No level shifters were used, and hence the input voltage V_{BAT} has been used as a rail for the gate drive of all transistors, causing a gate voltage swing between ground and V_{BAT}.

Fig. 4(a) depicts the efficiency plot of the two approaches while delivering a load current of 1 mA using the optimized parameters obtained in the first and second optimization. Since the two designs are subject to the same constraints, the efficiency curves are fairly coincident. However, by comparing the results, it is evident that when the components are sized individually (second optimization) the total occupied area of the switches is 0.65 times that of first. Therefore, henceforth we shall focus only on the design of second optimization. Fig. 4(b) emphasizes that the proposed SCC dramatically improves the efficiency at low output voltages. Specifically, the SCC efficiency is improved by 15% in the vicinity of $V_{DD} = 200$ mV as compared to the one using a conventional nine-switch topology [4], [6] while maintaining the same efficiency over the rest of the range. The SCC achieves a peak efficiency of 90.35% at $V_{DD} = 0.53$ V with 1 mA load current.

Fig. 5 shows the open-loop key waveforms of the SCC at two operating points. As is evident from the figure, the parameters of the SCC are optimized to brief in the incomplete transfer mode. It can be noticed that, using $G = 1/2$ topology, the operation is governed by two clock phases, while with $G = 1/4$ topology one clock period is divided into three time sessions.

Post-layout Monte Carlo analysis was also performed to further validate the robustness of the proposed converter. Fig. 6 plots the distribution of the obtained unregulated maximum output voltage of each topology and the average efficiency η_{avg} (6) in a 3000-point simulation at $I_o = 1$ mA. This simulation takes into account both local and global process variations. As can be seen, the proposed converter is very robust, achieving very slight deviations in all examined parameters.

Table II shows performance comparison of some previously reported SC converters. The total active area that is consumed by the switches, the flying capacitors, and the expected control circuitry is 0.074 mm^2. It should be highlighted that the active area is dominated by the flying capacitors by about 240 times the area of the switches. Therefore, assuming that the other parameters are kept constant, the total active area will not change significantly if more power switches are added (for additional voltage gains) or by enlargement of the power switches to support a higher output load

TABLE III
UNREGULATED EFFICENCY AND LOSS FACTORS CONTRIBUTION

	$G = 1/4$	$G = 1/3$	$G = 1/2$	$G = 2/3$
P_{drive}	17.84 μW	19.56 μW	23.2 μW	22.6 μW
P_{cond}	54.89 μW	65.56 μW	19.8 μW	124.4 μW
$P_{\text{Leak}} + P_{\text{BP}}$	9.58 μW	11.78 μW	13.6 μW	10.8 μW
V_{DD}	0.2201 V	0.3011 V	0.5302 V	0.6089 V
P_{Control} (extracted)	20 μW	10 μW	10 μW	10 μW
η (including P_{Control})	68.26%	73.79%	88.84%	78.39%
η (excluding P_{Control})	72.78%	75.65%	90.35%	79.41%
η_{max} using (1)	80.04%	82.12%	96.4%	83.03%

Unregulated efficiency and loss factors contribution at I_{o} =1 mA for each conversion ratio. The simulation conducted with the optimized values of the 2nd optimization.

power. Although a direct and fair comparison with other competing systems is difficult because of the different target output power levels, the number of conversion ratios, the input and output voltages, the flying capacitor technology, and the switching frequency, it may be worth comparing our system with the system reported in [7]. Both systems adopt a high number of conversion ratios with the same output power, but the number of switches and the resulting active area is higher in [7] compared to the proposed design. The systems achieve approximately similar deviation between peak efficiency relative to the ideal efficiency. However, because of the employment of the three-phase clocking operation, it is expected that the efficiency of the proposed system would decrease rapidly at low output power levels. The core of this brief is based on the SCC presented in [6]. Therefore, it is also worth outlining the differences between the designs. The design in [6] was implemented in SOI technology working at higher voltage levels (step down from 2 V to 0.5–1.2 V). It is well known that the advantages of SOI technology allow operating the SCC at higher switching speeds and, hence, brief satisfactorily within the power constraints of the intended low-voltage applications. A very noticeable and important aspect is the approach of sizing the SCC components. Le *et al.* [6] used an equation-based optimization procedure evaluated at single nominal point. Kwong *et al.* [7] and Ramadass *et al.* [10] used the adjustable switch width sizing method to maintain the complete charge-transfer mode. The other systems, [8], [11] did not address this issue. In contrast, this brief suggests simulation-based sizing methodology evaluated over all possible configurations while meeting predefined design constraints.

Table III shows the loss mechanism distribution due to each loss factor at different configurations while delivering output current of $I_{\text{o}} = 1$ mA. It is evident that the dominant loss portion is the conduction losses P_{cond}. In order to improve the total efficiency, the power consumption of the control losses has been extracted from previous brief [10]. They reported control losses of about 15 μW at the switching frequency of 30 MHz. We use an overhead of 20 μW to represent the control losses when the circuit is configured to $G = 1/4$, and 10 μW to represent the control losses of the remaining configurable gains. According to Table III, we obtain a deviation of about 5% at $G = 1/4$ between the efficiency with and without including the control losses, while the other configurations exhibit 1%–2% difference. These results imply an improvement of 10%–11% in sub-200 mV load voltages of the proposed SCC.

V. CONCLUSION

Four different conversion ratios were employed by the addition of a single power switch to the conventional topology instead of cascading two SCC circuits in order to implement the $G = 1/4$ voltage gain. The proposed SCC achieved an efficiency improvement of 10%–11% in the vicinity of $V_{\text{DD}} = 200$ mV as compared to the conventional topology (Fig. 1) and a peak efficiency of about 88.84% at $V_{\text{DD}} = 0.53$ V (Table III). It is well known that increasing the number of configurable voltage gains is always preferable for maintaining the efficiency high to a design with fewer configurable voltage gains. However, the penalty of such approach is the necessity of more complicated control schemes and slightly reduced efficiency unless the output power is boosted [5]. The main contribution of this brief lies not only in maximizing the peak efficiency at one particular output voltage but also in establishing an organized methodology for sizing and optimizing the power-stage SCC. The proposed optimization procedure was employed to realize four conversion ratios using two approaches, and it was shown that the second approach consumes less area occupied by the switches. With a little effort, the proposed approach can be expanded to consider additional performance constraints such as output voltage ripple [12], control circuit losses, and harmonic content of the charging current.

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