Reconfigurable Hardware Structures for Spreading and Scrambling Operations

Sug H. Jeong, Myung H. Sunwoo, and Seong K. Oh

Abstract— This paper proposes reconfigurable hardware structures for spreading and scrambling of multi-mode CDMA systems. The proposed reconfigurable structures supporting IS-95, cdma2000 and WCDMA, include a pseudo noise code generator, a channelization code generator and a control circuit for signal flow control. The proposed reconfigurable structures provide an efficient hardware usage for multi-mode CDMA systems. The synthesis results show the area reduction about 24.7% compared with the original code generators. The proposed structures can provide efficient reconfigurability and high speed operations for future SDR systems.

Index Terms— CDMA, Reconfigurable, Spreading, Scrambling, SDR

I. INTRODUCTION

The recent growth of CDMA communication services has resulted in a number of competing and incompatible air interface standards. Due to various standards and backward compatibility, international roaming has not been realized. Hence, products that support dual or even more modes have been emerged. However, these are typically a combination of existing single mode products [1]. This approach is costly, inflexible, and unable to adapt to future communication standards.

In order to overcome these problems, the concept of

the software defined radio (SDR) has been promoted [2]. SDR is a flexible communication system that supports multi-mode and multi-band through software update and hardware reconfiguration. To implement SDR, many flexible hardware structures have been proposed. For example, a general transmitter/receiver structure of mobile cellular systems [3], a programmable modulator / demodulator [4] and a reconfigurable correlator/FIR filter [5] have been proposed.

Fig. 1 shows a conceptual SDR platform. It is composed of reconfigurable processors, DSP, and microprocessor. Functions requiring high speed operations, such as the scrambling code generation, channelization code generation and the spreading operation are performed in the reconfigurable hardware [6]. Hence, a flexible and efficient hardware architecture is necessary.

Fig. 2 shows the generalized structure for the spreading and modulation of CDMA systems. First, the data sequence is multiplied with a set of orthogonal
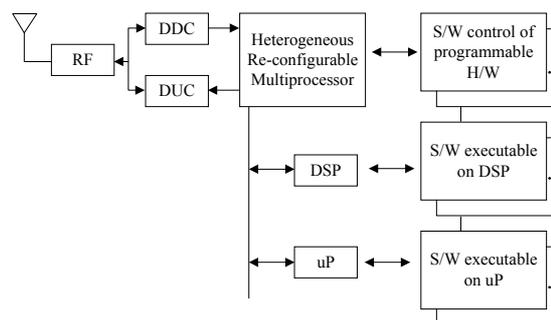

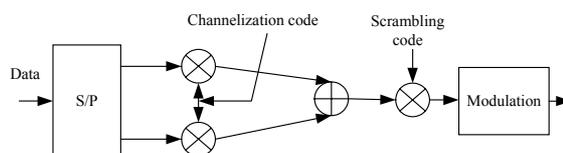**Fig. 1.** Conceptual SDR platform.

Fig. 2. Generalized CDMA spreading and modulation.

channelization codes for separating different users. The In-phase and Quadrature-phase parts are joined, and then scrambled with scrambling codes.

However, many differences exist in CDMA systems. Each CDMA system uses different channelization codes and scrambling codes. In IS-95, only the 64-chip Walsh codes are used for channelization and I/Q channel PN codes are used for scrambling. CDMA2000 uses the same scrambling codes, however it uses variable length Walsh codes. WCDMA uses OVSF codes for channelization and Gold codes for scrambling. In addition, CDMA2000 and WCDMA use complex scrambling, etc. By using flexible code generator, common spreading and modulation structures for CDMA systems can be used.

This paper proposes common spreading and scrambling structures for multi-mode CDMA systems. The common structures can be used in SDR and they can perform spreading and scrambling processes of IS-95 [7], cdma2000 [8] and WCDMA [9].

The paper is organized as follows. Section II describes the proposed common structures. Section III and IV contains implementation results and concluding remarks, respectively.

II. THE PROPOSED COMMON STRUCTURES FOR SPREADING AND SCRAMBLING

This section describes the proposed common

(a)

(b)

(c)
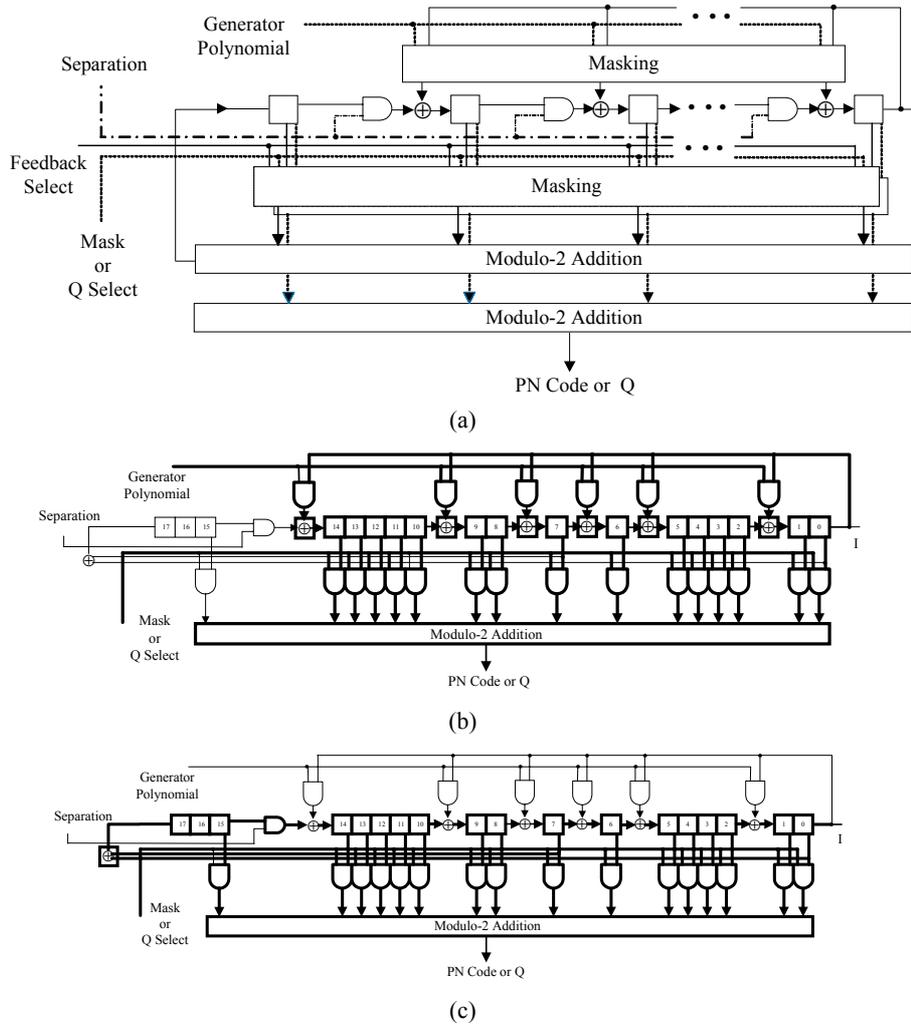
Fig. 3. (a) The proposed PN code generator. (b) Configuration for the IS-95 and cdma2000 modes. (c) Configuration for the WCDMA mode.

structures of CDMA systems for spreading and scrambling. A common pseudo noise code generator, a common Walsh and an OVSF code generator, and an overall common spreading and scrambling structure are presented.

A. The Common Pseudo Noise Code Generator

The PN code can be generated using a feedback shift register. The feedback shift register is divided into two categories [10]. In the Galois configuration, with each clock cycle the output of the last register is introduced into each of the tapped registers simultaneously, where it is added (modulo 2) to the contents of the preceding register. In the Fibonacci configuration, with each clock cycle selected register values are added (modulo 2) and the resulting bit is fed back into the first register. IS-95 and cdma2000 use the first configuration and WCDMA uses the second configuration. In addition, the length of the shift register and the number of output codes are different. Fig. 3(a) shows the proposed PN code generator that supports the differences mentioned above. Details of the proposed PN code generator are described as follows.

First, the circuits to update register values are reconfigured. For the Galois configuration, AND gates and the Generator Polynomial signal are used as shown in Fig. 3(a). The XOR gates are selected according to the generator polynomial. If the Generator Polynomial signal is '0', then the connected XOR gate has '0' as its one input. Thus, the XOR gate passes another input signal directly. Hence, the XOR gates selected by the generator polynomial are operating as a modulo 2 adder. For the Fibonacci configuration, different masking and modulo 2 addition circuits are added. The Feedback Select signal selects register values, which are used to update the most significant register. The selected values are added (modulo 2) and are fed into the most significant register.

Second, the Mask or Q Select signal is used to mask or select the output sequence. The desired register values can be selected by inserting '1' to the AND gates because the modulo 2 addition counts only the number of 1s.

Finally, the AND gates to separate registers are included between registers. The shift registers are separated at the desired positions by inserting '0' into the

Separation signal. Thus, we can obtain variable length shift registers according to standards.

Fig. 3(b) and 3(c) show configuration examples, which operate as the I channel pilot PN code generator of IS-95 and a part of the downlink scrambling code generator of WCDMA, respectively. The thick lines represent the parts used in each mode. Using this structure, the partial I and Q scrambling codes and the I channel pilot PN code can be obtained. Fig. 3(c) shows only one shift register.

Fig. 4(a) shows the complete code generator configuration. One shift register is reconfigurable as the I channel pilot PN code generator and one shift register of the downlink scrambling code generator. Another shift register is reconfigurable as the Q channel pilot PN code generator and another shift register of the downlink scrambling code generator. 36 registers are required to implement the complete generator and 18 registers are used for each shift register. Each shift register has the separation circuit at the 15th register for IS-95 and cdma2000. In the WCDMA mode, the shift register output I and Q signals are modulo 2 added, and then they become complete I and Q scrambling codes of WCDMA. In IS-95 and cdma2000, each Q signal of two shift registers is the I and Q channel pilot PN code, respectively. Similarly, the proposed PN code generator as shown in Fig. 4(b) is reconfigurable as the long code

(a)

(b)
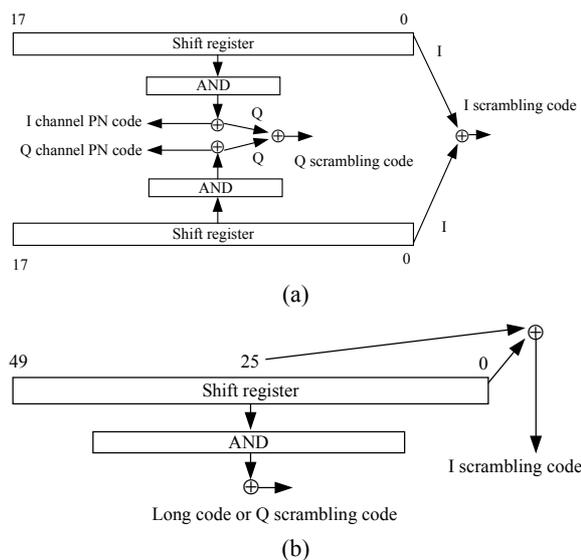
Fig. 4. (a) I/Q channel PN code generator + downlink scrambling code generator. (b) Long code generator + uplink scrambling code generator.

generator and the uplink scrambling code generator.

The proposed PN code generator is recongfigurable by using parameters, such as the Generator Polynomial, Feedback Select, Mask or Q Select, and Separation signals as shown in Fig. 3(a), and it can generate any PN code.

B. The Common Walsh and OVSF Code Generator

Fig. 5 shows the OVSF code tree. The OVSF code has a variable length according to data rates. In this figure, SF (Spreading Factor) represents the code length. The OVSF codes are generated recursively as depicted in Fig. 5. Starting with the sequence, $C_{1, 0}$, the sequences $C_{2M, 2k}$ and $C_{2M, 2k+1}$ of the length 2M are derived from the sequence $C_{M, k}$ of the length M by appending $C_{M, k}$ (upper branch) and by appending $-C_{M, k}$ (lower branch). Lower branch codes contain the upper code, and thus, the longest code has all upper codes having the same root. Consequently, we can obtain the desired OVSF codes from the longest OVSF code.

Fig. 6 shows the proposed Walsh and OVSF code generator. To produce variable length codes, the shifter and counter are used. The shifter shifts the input code number left $N - \log_2 SF$ times. Then, the shifted code number designates the longest code (length = 2^N). The longest code has the desired code as a root. Thus, the generated longest OVSF code contains the desired code. The counter is reset when the counter value is the same as SF, and thus, the desired length code is generated. For example, if $N = 3$, $SF = 2$, and the input code number is 1, then the shifted code number becomes 4. Thus, the generated code is $C_{8, 4}$. However, the counter is reset in every 2 (SF = 2) clocks, and then the output is the desired code $C_{2, 1}$. The range of the code is from 1 to 2^N.

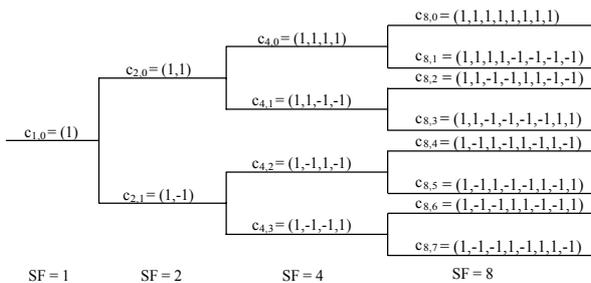The bit reverse block is used for the Walsh code generation. The Walsh code number is the bit reversed form of the OVSF code number. The proposed structure generates Walsh and OVSF codes having variable lengths.

C. The overall common structure for spreading and scrambling

Fig. 7(a) shows the overall common structure for spreading and scrambling of CDMA systems. The proposed code generators shown in Fig. 4 and Fig. 6 are used, and MUXs for signal flow control are added. This structure supports IS-95, cdma2000 and WCDMA.

The common signal flow includes data mapping, serial to parallel conversion, spreading, scrambling, pulse shaping and quadrature modulation. First, the input data is converted to real values (+1, -1) in the data mapper block. Then, the data is spread with the Walsh or OVSF code after serial to parallel conversion. Scrambling, pulse shaping and quadrature modulation are performed. To provide flexibility, the proposed structure uses programmable filters and NCO.

In Fig. 7(a), MUXs and multiple signal paths are used to select data according to each standard. For IS-95 and cdma2000, the long code is generated and is multiplied with the data. In the IS-95 uplink, the data is replaced by the Walsh code. WCDMA and cdma2000 use complex scrambling.

Fig. 7(b) shows the proposed PN code generator. Using the structure, every code used in CDMA systems can be generated. It consists of the I/Q channel pilot PN code and the downlink scrambling code generator, the long code and the uplink scrambling code generator, 2:1 decimator, multipliers, and MUXs. In the downlink of IS-95, cdma2000 and WCDMA, the I/Q channel pilot PN code and the downlink scrambling code generator are used. However, in the uplink of cdma2000 and WCDMA,
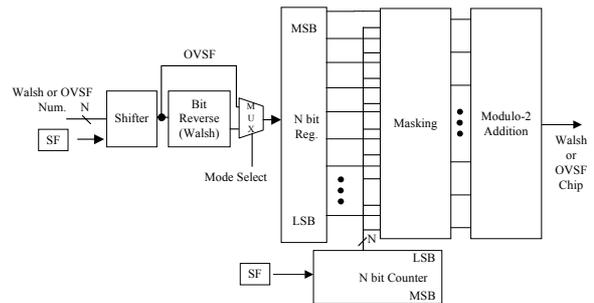

Fig. 5. OVSF code tree.

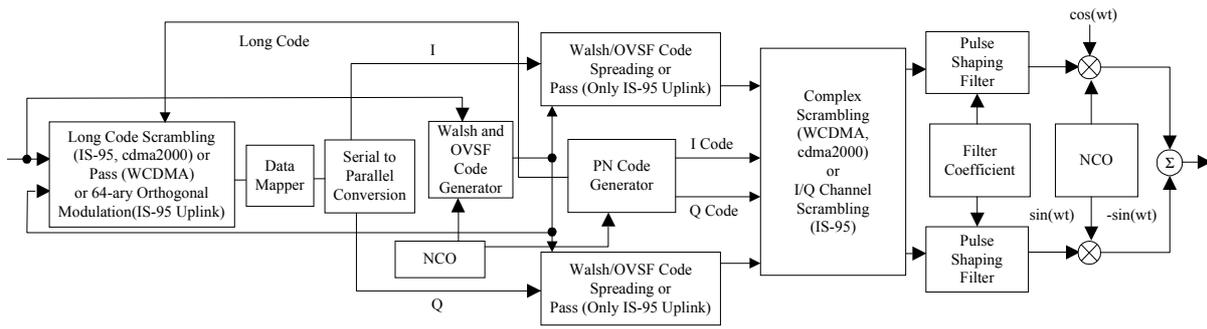**Fig. 6.** The proposed Walsh and OVSF code generator.

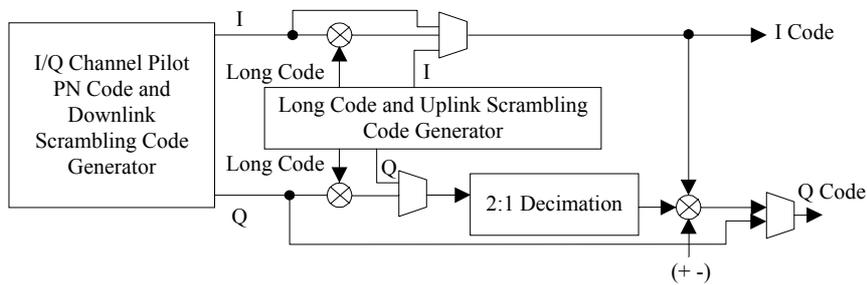**Fig. 7.** (a) The overall spreading and scrambling structure.

Fig. 7. (b) The PN code generator.

2:1 decimation and scrambling with the fixed repeating function (+1, -1) are performed.

The proposed structures provide the common architecture for IS-95, cdma2000 and WCDMA by reconfigurable code generators.

III. IMPLEMENTATION RESULTS

The proposed code generators have been simulated in VHDL, and synthesized using the Faraday 0.25μm standard cell library. The results are shown in Table I.

As shown in Fig. 4, the proposed code generators in the fourth column of Table I are reconfigurable as the code generators in the first column of Table I. The area of the whole code generators in the fourth column of Table 1 is reduced by about 24.7% compared with the original code generators listed in the first column of Table I. In addition, using the overall common structure for spreading and scrambling can reduce more area.

IV. CONCLUSIONS

In this paper, reconfigurable hardware structures of spreading and scrambling for multi-mode CDMA systems are proposed. The PN code generator, the Walsh and OVSF code generator and the control circuits for signal flow control are proposed. The proposed common structures support IS-95, cdma2000 and WCDMA. These common structures have smaller area compared to the combination of each structure. Thus, an efficient hardware usage can be obtained. In addition, the proposed spreading and scrambling hardware structures can be used in the SDR to satisfy high speed operations which cannot be performed by software.

Table I. Synthesis results

Generator	Gates	Generator	Gates
I channel PN code	173	The proposed generator Fig. 4(a)	437
Q channel PN code	178		
DL scrambling code	269		
UL scrambling code	332	The proposed generator Fig. 4(b)	609
Long code	503		
Walsh code	173	The proposed generator Fig. 6	349
OVSF code	224		

ACKNOWLEDGEMENTS

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