

Monitoring Power Dissipation for Fault Detection

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Abstract

In this paper, we suggest that the dynamic power dissipation of a circuit can be used to detect faults in it. The change in dissipation caused by a fault can be maximized by applying specific test vectors. For example circuits, we show that the power dissipation can be used to detect faults which do not affect static power dissipation. We also discuss how faults may be detected with a frequency domain analysis. In many cases, the Fourier spectra of the power supply currents in the good and faulty circuits will be very different. Power monitoring is also verified experimentally, for an example circuit.

1 Introduction

Monitoring the current drawn from the power supply is one method to test a CMOS circuit [2–4]. In this paper, we demonstrate that monitoring the dynamic power dissipation of a device can also aid in fault detection. A fault which affects functionality also changes the energy consumption on input transitions. The inputs can be applied so as to maximize the difference in energy consumption between the good and faulty circuits on each transition. The difference in power dissipation can be raised by increasing the input frequency. Target faults considered include stuck-at and stuck-open faults in static CMOS circuits. The Fourier spectra of the power supply currents in the good and faulty circuits are also different. This difference in the frequency domain decomposition can also be used to detect the presence of a fault.

2 Preliminaries

In a CMOS circuit, power is dissipated when the inputs are static, and when they change. With static inputs leakage currents in devices cause power dissipation. There are two components to power dissipation caused by input changes: (1) short-circuit and (2) capacitor charge currents. Several signals change in response to an input transition. When a gate's output rises: (1) there is a power to ground path which causes a temporary short circuit current; (2) the capacitive load C at its output will have to be charged to V_{DD} . The charge supplied is CV_{DD} . At a transition frequency f , the power dissipation is CV^2f . The average current drawn from the power supply is CVf .

Relevant Previous Work: Several CMOS test techniques based on monitoring the power supply current

are known. The most common are I_{DDQ} test schemes. The transient response of the circuit to pulses on power supply rails is another test technique [5]. I_{DDt} test techniques [3, 4] measure the dynamic response to an input transition. In [3] the shape of transient response is used as a guide to fault detection. The technique discussed in [4] monitors the charge injected into each gate, or a collection of gates, in a circuit on various input transitions. DSP techniques have also been applied to fault detection [7]. Techniques to minimize the power dissipation of a circuit when testing it, to ensure it does not exceed specifications, are presented in [8]. A detailed comparison with previous work is discussed later.

3 Fault Detection

When the inputs to a circuit are changed with frequency f , the power supply current is a pulse sequence. The start of each pulse is coincidental with input transitions. The width of the pulse is determined by the longest path along which input changes are propagated. The magnitude of the pulse is determined by the maximum number of signals changing simultaneously. The area under the pulse determines the total energy consumption. Consider a fault f on a gate g in a circuit C . In addition to the circuit functionality, the fault f also alters the signal transitions resulting from a transition in the inputs. Therefore, the short circuit current drain and the number of capacitors charged and discharged in the good and faulty circuits will differ. That is, a fault alters the energy consumed by a circuit in responding to an input transition. Consequently, for a sequence of vectors, the total energy consumed, as well as the instantaneous power dissipation, are altered by a fault. The input vectors and the specific fault determine the impact on the energy consumption.

Targeted Detection Given a target fault, inputs may be applied such that the difference in energy consumption between the good and faulty circuits is maximized. As an example consider a stuck at fault f . A pair of vectors V_1 and V_2 is chosen as follows. V_1 is set such that f is excited and one or more paths from the fault site that are sensitive to the fault are created. V_2 is chosen such that the signals at the fault site and along the sensitized path assume their value in the faulty circuit. When V_1 and V_2 are alter-

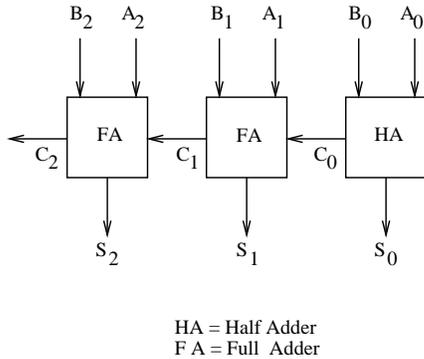


Figure 1: Three-bit adder

nated at frequency f , in the good circuit, the signal values at the site of the fault and along the sensitized path will oscillate. In the faulty circuit none of the wires at the fault site and along the sensitized path will change state. Maximizing the sensitized path will maximize the difference in energy consumption. Assume that, on both transitions a total capacitance of C_G (C_F) is charged in the good(faulty) circuit. The energy consumed on each transition in the good(faulty) circuit is $C_G V_{DD}^2$ ($C_F V_{DD}^2$). The difference in power dissipation between the good and faulty circuits is $(C_G - C_F) V_{DD}^2 f$. The difference in energy consumption depends on the target fault and input vectors. The difference in power dissipation depends on the input vector frequency. The power dissipation difference is detected by monitoring the power supply current.

Fourier Spectrum An analysis of the supply current in the frequency domain can also aid in fault detection [10]. A fault will alter the relative strengths of the various components in the Fourier spectrum of the current. The width of the current pulse is determined by the length of longest path of wires and gates sensitive to the changing input signals. The maximum value of the pulse is determined by the maximum number of gates changing state simultaneously. The length of the longest path sensitive to the input change may be changed by a fault. The maximum number of gates changing states simultaneously may not be altered by the same fraction. Thus, a fault will change the width of a pulse relative to its maximum value. This alters the relative strengths of the various components in the Fourier spectrum. If the width of a pulse is decreased while maintaining its magnitude, the high frequency components in the spectrum are strengthened. If the width is increased while maintaining its magnitude, low frequency components are strengthened. Rather than absolute values, relative strengths may be used to detect faults.

4 Test Technique Application

Consider the adder designed to add 3-bit numbers in Figure 1. The inputs are two 3-bit vectors A and B . The gate level realization for a one-bit full adder is shown in Figure 2. A half adder can be derived from

the full adder. Refer to the vectors formed by the sum and carry outputs as S and C . Let the B inputs to the adder be constant at $B_7 = b_2 b_1 b_0 = 111$. Consider two vectors $A_0 = a_2 a_1 a_0 = 000$ and $A_1 = a_2 a_1 a_0 = 001$, alternated at the A inputs with frequency f . In the good circuit, the sum and carry vectors for input A_1 are $C_1 = 111$ and $S_1 = 000$, and for the input A_0 they are $C_0 = 000$ and $S_0 = 111$. We consider the effects of various faults. All circuits discussed below were simulated using Spice with the parameters for a 2μ 5V process. A 30pF capacitor was added to the power supply pin to suppress ripples, and a 30Ω resistor and 30nH inductor were added to simulate lead resistance and inductance.

Stuck-at Faults Consider a stuck-at 0 ($sa0$) fault on the carry output of the half adder. For the input A_1 the sum and carry vectors are $C_1 = 000$ and $S_1 = 110$. For the input A_0 the sum and carry vectors are $C_0 = 000$ and $S_0 = 111$. In the faulty circuit, the number of signals which change state when A_0 and A_1 are alternated is far less than in the good circuit. Consequently, the energy consumed from the power supply is lower in the faulty circuit than in the good circuit. The difference will depend on device characteristics, such as gate and routing capacitances. The power supply current waveforms in the good and faulty circuits, when the inputs are applied at 10MHz, are compared in Figure 3. The larger waveform shows the supply current in the good circuit. Both the shape of and the area under the waveforms differ markedly. At 10MHz, the average power dissipation in the good and faulty circuits are approximately $240\mu W$ and $75\mu W$. The difference in the average currents is $33\mu A$. Capacitances to account for on-chip routing, and the output loads were not incorporated into the Spice file. (Leakage currents, used in I_{DDQ} test, for the 3-bit adder are less than $10 nA$.) The difference in average current is proportional to the input frequency.

Fourier Transform The fault also alters the “shape” of the Fourier spectrum of the faulty circuit. Figures 4 and 5 show the Fourier spectra of the power supply currents in the good and faulty circuits respectively. With respect to the good circuit, in the faulty circuit the relative reduction in the width of the power supply pulse is greater than the reduction in its maximum value. In the good circuit, the low frequency components are strong relative to the high frequency components. In the faulty circuit, the low frequency components are relatively weaker. For example, in the good circuit, the ratio of the 10MHz component to the 100MHz component is approximately 3. In the faulty circuit, this ratio is approximately 1.2.

Stuck-open Faults We demonstrate that a transistor level fault which alters functionality, and not static dissipation, may also be detected by monitoring the power dissipation. We consider a fault in the logic used to compute the carry out signal of the half adder in Figure 1. The half adder is obtained by deleting redundant gates from the full adder of Figure 2. That is, gates $N5$, $N6$, $N7$, and $N9$ are removed, and

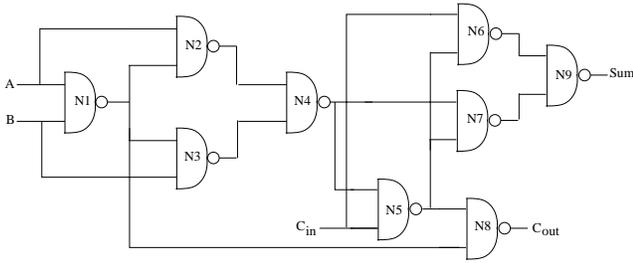


Figure 2: Gate-level description of one-bit adder

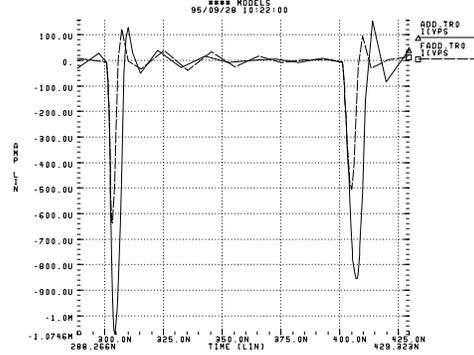


Figure 3: Monitoring power dissipation to detect a stuck fault

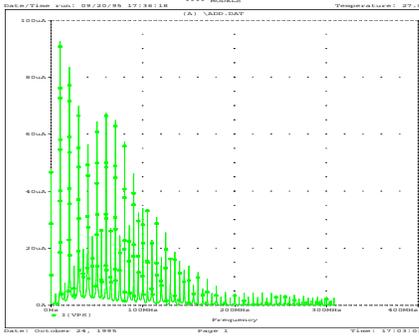


Figure 4: Fourier spectrum in the fault-free adder

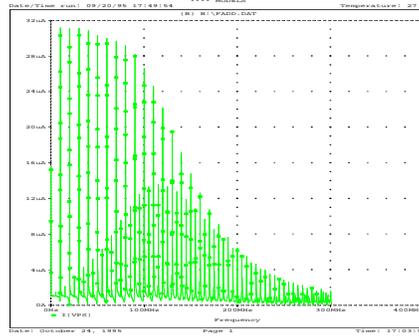


Figure 5: Fourier spectrum in the faulty adder

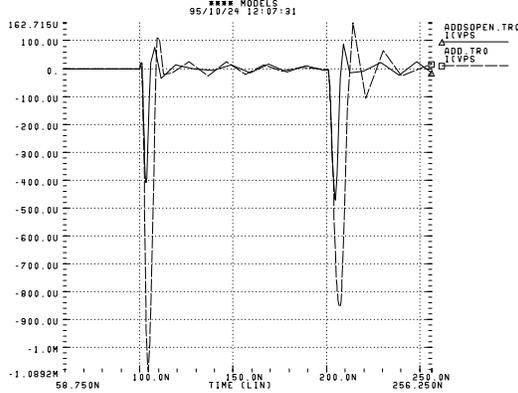


Figure 6: Detecting a stuck-open fault

$N8$ replaced by an inverter I . Consider a stuck-open fault in the pMOS transistor p_I in I . Consider the set of patterns used above. For the vectors A_0 and A_1 , the signals c_0 and c_1 are 0 and 1. When p_I is stuck-open, the signal c_0 remains at 0 even when A_1 is applied after A_0 . Hence, the capacitive load on the signal c_0 is not charged. For both inputs A_0 and A_1 , the carry out vector in the faulty circuit is $C = 000$. The sum vectors for the two inputs in the faulty circuit are $S_0 = 111$ and $S_1 = 110$. The power dissipated by the good circuit is more than that dissipated by the faulty circuit. Figure 6 compares the supply currents in the good and faulty circuits.

Dynamic Circuits Power dissipation monitoring may also be applied to dynamic circuits. We consider DCVS circuits [6], and a stuck-on fault. Consider the AND gate in Figure 7. Assume that it is used to compute the carry out in the half adder of Figure 1. When $PC = 0$, both preoutput nodes pc_0 and pc_1 are precharged to 1. When PC is high, and if the circuit functions normally, only one of the two circuit outputs is raised. In the 3-bit adder, there are two carry vectors C and \bar{C} , and two sum vectors S and \bar{S} . Again, we consider the same set of input vectors B_7 and A_0 . The carry vectors for the good circuit are $C_0 = 000$ and $\bar{C}_0 = 111$. The sum vectors are $S_0 = 111$ and $\bar{S}_0 = 000$. Next, consider a stuck-on fault in transistor $T4$. In the faulty circuit, for an input of A_0 both the c_0 and \bar{c}_0 inputs are raised to 1. This alters other carry signals in the adder as well. For the inputs A_0 and A_1 , the carry vectors for the faulty circuit are $C_0 = 111$ and $\bar{C}_0 = 111$. The sum vectors are $S_0 = 111$ and $\bar{S}_0 = 011$. Whenever a gate output is raised to 1, the corresponding preoutput node has to be recharged. In the good circuit, only the \bar{C} and \bar{S} nodes are raised to 1. In the faulty circuit, all but one of the sum and carry vector nodes are raised to 1. More nodes will have to be recharged during the precharge phase in the faulty circuit. Hence, the faulty circuit will consume more energy from the power supply.

Redundant Faults Circuits may contain faults which are redundant, or untestable, at the logic level.

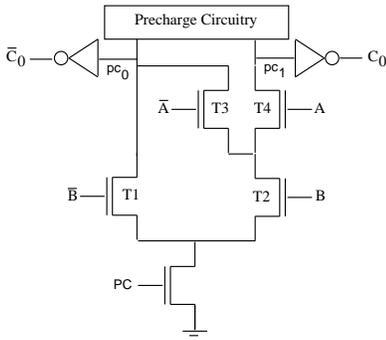


Figure 7: DCVS AND gate

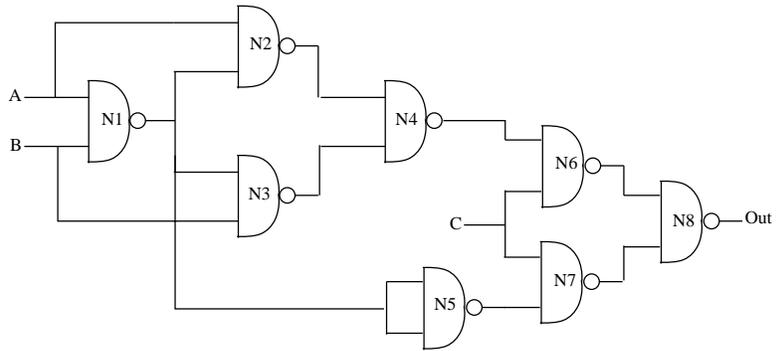


Figure 8: Example circuit with redundant fault

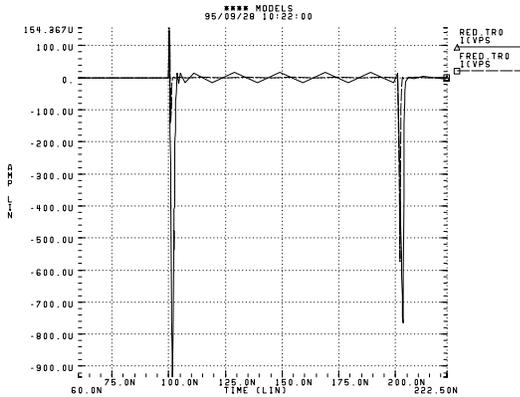


Figure 9: Detecting a redundant fault

These faults may affect the functionality of a gate and internal signal values. With power monitoring, if a fault affects a sufficient number of internal signal transitions, it may be possible to detect it, even if it is redundant. Consider the circuit shown in Figure 8. Consider the *sal* fault on the output of gate *N1*. This fault is logically redundant. Consider two input vectors $V_1 = abc = 011$ and $V_2 = abc = 111$. When these vectors are alternated at the inputs, in the good and faulty circuits, the number of signals which change state are 10 and 2 respectively. Consequently, the faulty circuit dissipates less power. Figure 9 compares the power supply currents when the input vectors are alternated at a frequency of 10MHz. There is a substantial difference between the power dissipation in the good and faulty circuits. While this fault is detectable, the detection of all redundant faults cannot be guaranteed. For example, gate *N5* is an inverter. A stuck-at 1 fault on one of the inputs to gate *N5* can probably not be detected by this technique. This fault cannot be propagated to the outputs of *N5*. Hence, vector pairs for which the signal transitions in the good and faulty circuits are substantially different cannot be generated.

5 Experimental Results

A prototype of the circuit in Figure 8 was constructed from discrete components and breadboarded. The time varying input was supplied by a signal generator. The stuck-at 1 fault was emulated by connecting

all the signals on the fanout of the faulty node to the power supply. The power supply current was magnified with a 100Ω resistor. The voltage across the resistor follows the supply current. Figure 10 compares the power dissipation in the good and faulty circuits for an input frequency of $1.5MHz$. Such a low frequency is enough to cause an appreciable difference since the capacitances on a breadboard are very large. The voltages measured were in the millivolt range, and required no special measurement techniques.

Fourier Spectra The oscilloscope could also compute the Fourier spectra of captured signals. The fault reduces the length of the longest path sensitive to the change in the input. However, the peak of the power supply pulse is not reduced by the same fraction. The low-frequency components can be expected to be stronger in the good circuit. In fact, one may observe a substantial difference between the spectra of the supply currents for the good and faulty circuits. As expected, not only does the magnitude at various frequencies change, the relative magnitudes of the components also change. Figure 11 shows the spectra of the good and faulty circuits. Since the spectra were not displayed simultaneously, they are not to the same scale. The spectrum for the faulty circuit, the upper one, is not significant on the same scale. Also, readers may note that the scale is in dB not μA . Even with such a compression, the difference between the shapes of the spectra is clear. Next, we discuss the advantages and limitations of this approach.

6 Discussion

This approach has both potential advantages as well as several significant limitations.

Advantages: We compare power monitoring with those based on monitoring the supply current. We target faults which do not affect static dissipation. (We are currently investigating the effectiveness of propagation with stuck-on and bridging faults.) I_{DDQ} test techniques may need built-in sensors to improve fault detection capability. The dynamic currents used here are normally larger than static currents. The effect of a fault is significant even only a small fraction of circuit gates are affected by it. Consider a circuit with 100,000 minimum-sized transistors, fabricated with a

Fault-free circuit

Faulty circuit

Figure 10: Measuring power dissipation to detect a redundant fault

Good circuit spectrum is the lower one

Figure 11: Fourier spectra for fault detection

2 μ 5V process. With a per transistor leakage current of 10^{-12} A [11], circuit leakage currents are 0.1μ A. The gate capacitance is approximately $0.75fF/\mu^2$. At an input frequency of 10MHz. To produce a power supply current difference of 50μ A, less than 70, or less than 0.2% of all signals, need be affected by the fault.

The charge injected into a gate on a transition can be used to detect faults [4]. The actual charge injected on a test is compared to the expected value, using built-in sensors. The expected charge injection has to be preset. This can restrict fault coverage, especially when one sensor monitors many gates. Also, no effort is made to propagate faults to other gates. There is a great reliance on simulation to estimate the charge injected accurately. With power dissipation, the effect of a fault can be magnified, and observed more easily, using several techniques. This reduces reliance on simulation accuracy. With off-chip test, the expected dissipation does not have to be preset, and a frequency domain analysis of the response may detect faults. The use of DSP techniques for fault detection has been suggested [7]. However, rather than absolute values, we suggest that relative values of components in the Fourier spectrum be used as a guide to fault detection.

Limitations: Power monitoring suffers from significant limitations. To maximize the power difference caused by it, a fault can be targeted by test vectors. However, to produce a measurable difference in power dissipation, each test vector pair will have to be applied multiple times at full speed. This, need for multiple application of each test pair will increase test time.

The fault coverage is determined by the minimum observable deviation in the supply current. This depends on the accuracies with which the expected current can be computed, and the actual current measured. The former depends on the accuracy and difficulty in estimating on-chip capacitive loads, and computing currents. The larger the difference caused by a fault, the less the reliance on tolerances. The coverage will be determined by the larger of the tolerances.

For a fault to be detected, the number of capacitors switched in the good and faulty circuits have to differ. The closer a fault is to the circuit outputs, the more difficult this is to achieve. One potential solution may be to develop a DFT technique to increase the capacitance at specific internal nodes in the test mode.

7 Conclusion

The dynamic power dissipation of a CMOS circuit can be used to detect faults in it. When a fault alters a circuit's functionality, it alters the way internal signals respond to input transitions. Consequently, the energy consumption and power dissipation of a circuit are altered by a fault. Both logic-level and transistor level faults in CMOS circuits, which do not change static dissipation, alter dynamic power dissipation. In many cases, a fault also alters the shape of the Fourier spectrum of the power supply current. This permits detection in the frequency domain. Power supply monitoring was shown to detect faults which

are redundant at the logic level. For a typical process, relative to I_{DDQ} and charge monitoring tests, the fault induced errors in the currents to be measured are large. The limitations of this technique include an increase in test time and the need for compute-intensive simulation.

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