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Protection of Instrument Control Computers against Soft and Hard Errors and Cosmic Ray Effects

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Summary

Off-the shelf commercial microprocessors, if properly selected and used, provide cost-effective, low weight and low power engineering solutions for space applications. Non-interruptable and 100 % error free operation is not a mandatory requirement for scientific instrument control. Thus, hardware overhead in terms of weight, power consumption and component cost may be significantly reduced. This paper deals with parts selection for radiative space environment, and selection of low-overhead redundancy concepts. Special attention is paid to cosmic ray induced single envent upsets in digital logic, because onboard protection methods are not always efficient. Functional requirements for onboard software are considered, especially for conditions where temporary errors, caused by single event upsets, are to be excepted. Design solutions for two space control computers are reviewed: Promics-3 control computer for the soviet Interball mission, and ERNE control computer for the future SOHO mission of ESA.

1. Introduction

Reliability of spaceborn computer systems, as well as other digital systems, is strongly affected by two factors: statistical, random fault mechanism of microelectronic components, and effects of cosmic radiation. This is especially serious, because in the reliability model of a typical computer system, all components are connected in series. Fault in any component leads to a failure of the entire system. Thus, designing reliable computers starts from components. Special attention must be paid to parts selection to ensure reliability and autonomous operation through the mission life, even in the presence of harmful ionizing radiation. Two major effects of cosmic rays are: overall component degradation and single event upsets. Component degradation leads to change of the component's functional parameters, increased power consumption, and finally, loss of function. Single event upsets (SEU) are cosmic ray induced, sudden changes in digital bistable elements: memories, registers, and complex LSI devices like processors. An upset may even trigger a condition called latch-up: a short circuit current which may lead to component destruction. Sensitivity for component degradation and sensitivity for SEU are not necessarily related with each other. A component may exhibit excellent tolerance against degradation, but still be sensitive for SEU or even latch-up.

Our focus is on instrument control computers, which have no functions critical for the safety of the mission. In this case, we may tolerate certain amount of errors. Component selection becomes thus less critical. However, effects of radiation must be carefully analyzed, in order to select suitable protection and redundancy concept from a large reservoir of possible techniques. When fault detection and recovery are selected instead of fault masking, the system becomes less hardware intensive and thus, more reliable. The role of software has increased significance.The computer system needs special software functions to support autonomy and safety of the processor, but the application software itself must have a proper structure.

2. Effects of Space Radiation

The effects of space radiation to integrated circuits can be divided into long-lived effects and transient effects, SEU's. The long-lived effects cause gradual degradation of performance and at last functional failure of a component. The long-lived effects are mainly caused by two mechanisms: ionisation and atomic displacement. In atomic displacement a particle of space radiation collides with an atom in the target material causing the atom to leave its position in the lattice and leave a vacancy or defect. Ionisation is a more important cause of failure for present day integrated circuits than atomic displacement. For this reason, atomic displacement is not treated in this paper. Transient effects can be non-destructive "soft errors" or they can in some cases cause permanent damage. SEU's are especially problematic in high-density RAM-memories and microprosessors. It is very important to evaluate the SEU rate for a space computer system, especially for critical systems. In the *ionisation* process the energy loss of radiation in material is converted to the form of electron-hole pairs. Thus the conductivity of any solid material is higher than normally for a time. The deposited energy in a material by means of ionisation is called "dose" and it is measured in rads or Grays (1 Gray = 100 rad). Ionisation can be produced in space by electrons, protons and X- and gamma rays. An important and harmful source of X-rays is the case material of electronic equipment. When a high-energy electron penetrates material it declerates, and part of the energy is converted to a photon. The emitted radiation is called bremsstrahlung. The wave lengths of the emitted photons are mainly in the X-ray part of the spectrum. The attenuation of X-rays in a material is low and thus bremsstrahlung is of great concern.

2.1 Total dose effects in MOS-components

Most of the components in modern computer systems are fabricated by MOS-technology. Especially CMOS-components are very suitable to be used in space computers due to the low power consumption and high speed of the newest components. Therefore it is important to know the effects of radiation in MOS-components. The degradation of MOS-transistors is mainly due to two phenomena: the trapping of positive charge (holes) in the gate oxide film and the rearrangement of atomic bonds at the oxide-silicon interface ("interface states"). The trapped charge causes the threshold voltage of an n-channel MOS-transistor to shift to more negative direction. This means that the transistor turns "ON" by applying lower gate voltage than before irradiation. Finally it becomes impossible to turn the transistor OFF. In p-MOS transistors the threshold voltage shift is to the same direction as in n-MOS transistors because the trapped charge is always positive. Thus more negative voltage is required to turn the p-MOS transistor ON, and finally the transistor can not be turned ON. When charge is accumulated to the oxide of a CMOS-component the loss of functions appears in the following order:

1. Noise immunity reduction, minor reduction of switching speed
2. Quiescent state current is increased strongly
3. Switching speed reduction
4. Functional failure, change of logic state impossible.

The effect of the interface states is that the I_D-U_G curve is reduced in slope. In n-MOS transistors this partly compensates for the threshold voltage shift caused by trapped charge. In p-MOS transistors the threshold voltage shift becomes even worse due to the effect of interface states. In both types the transconductance of the channel is reduced and this may cause further reduction of switching speed.

Total dose tolerance of standard CMOS components is quite low, typically between 5 and 20 krad [1]. Many CMOS components are, however, available as radiation hardened (RadHard-) versions. In RadHard manufacturing processes the purity and growth process of the oxide films are controlled very tightly. By this way there will be less defect centres in the oxide films and less charge gets trapped. Table 1 shows a summary of radiation tolerances of some CMOS logic families, microprocessors and memory components. Some representative values are shown. Radiation tolerance depends on the manufacturer and the process used.

Component type	Max. dose parametric /krad	Max. dose function /krad
4000-series logic	about 5	about 30
4000 series logic (RadHard)	100-1000	100-1000
54HC-series logic	5-10	20-40
PROM	-	20
EPROM	-	about 5
EEPROM	-	10-50
(8k*8) RAM (stat.)	>30	>30
(32k*8) RAM (stat.)	-	6-15
MAS281, 16-bit CPU	>100	>100
T414, 32-bit CPU	2-5	2-60
80C86,16-bit CPU	9-14	16
80C86(RadHard 16-bit CPU)	>100	>100
SBP9989, 16-bit CPU	20-4000	20-6000

Table 1. Summary of radiation tolerances of some CMOS logic families, microprocessors and memory components. [2] - [16]

2.2 Total dose effects in digital bipolar integrated circuits

Radiation tolerance of digital bipolar integrated circuits is in general larger than that of CMOS circuits. The degradation of bipolar transistors is mainly due to trapping of charge in passivation oxide layers and atomic displacement damage in silicon. These effects cause reduction of gain and increase of junction leakage current. Most sensitive of digital bipolar integrated circuits are those using advanced oxide isolation process such as FAST , ASL , IIIL , ISO-Z and IMOX [17]. These families are susceptible to failure at doses between 10 krad and 1 Mrad. Low power schottky (LS) family will operate within specification limits after 1 Mrad. IIL devices operate within specification limits after about 100 krad - 1Mrad depending on the manufacturer and process. ECL technology is very hard against radiation. Many ECL devices are operational after 10 Mrad.

3. Effect of shielding to total dose

When energetic particles pass through material they lose energy by interaction with the atomic structure of the material. The range of a particle in a material is the thickness of material penatrated before the particle loses all its energy. Range is expressed either in units of depth or as the product of depth and density (gcm^{-2}). The latter unit is commonly used as a measure of absorber thickness, and it is often called "shield thickness" or "mass thickness". The range in gcm^{-2} of a particle at a given incidence energy depends slightly on the material. It can be said that as a rough approximation the shielding effect of material is dependent on the mass per area of the shielding material. When particles collide with atoms in the shielding material they generate photons whose energy is in the X-

ray spectrum. This radiation is called bremsstrahlung and it also causes ionisation in electronic components. A heavy element will generate bremsstrahlung more efficiently than a lighter one. Aluminium is the most commonly used construction material in space instruments. Figure 1 shows the total dose versus Al thickness as an example of the effect of Al shielding on the total dose on the orbit of Soho. On the outer surface of spacecraft and with reasonable shield thickness, radiation dose in interplanetary, near-earth space is order of a few kilorads per year. Within the magnetosphere the value is higher: geosynchronous orbit yields order of ten kilorads per year.

[figure omitted in online version]

Figure 1. Total dose versus Al shielding thickness on Soho in 2 years.
*4*pi dose at the centre of Al spheres. [1].*

4. Effect of component bias on radiation tolerance

In MOS components the trapping of charge is strongly dependent of the gate voltage during irradiation. Typically the threshold voltage shift of a CMOS-component, which is biased one half of the irradiation time, is about 50% of the shift of a component which is continuously biased [1]. If the supply voltage is turned completely OFF during irradiation the threshold voltage shift is typically only about 5% of the shift of a component which is continuously biased. The effect of total dose can thus not be totally neglected even if the supply voltage is OFF.

As a result, a method for improving radiation tolerance is to switch off electronic parts whenever they are not needed. Another aspect is, that radiation damage is partially self-healing. Increase of supply current may be used as an indication of radiation damage, when the circuits are still functioning. By switching off electronics in case of observed damage for some time, the operational life of the electronics may be prolonged.

5. Single Event Upset

Single Event Upset (SEU) is caused in space environment by an energetic ion penatrating to the silicon chip. The ion produces a burst of hole-electron pairs. If the produced charge of the burst is large enough then a digital electronic circuit can change its logic state. This can appear in a CPU component as a bit-flip in a register, stopping of the CPU, program jump, etc. In a RAM-component the contents of a memory location is changed.

SEU can also cause permanent damage of the component. Most common damage mechanism is the triggering of an internal parasitic thyristor structure or the so-called latch-up effect. This effect is common in older CMOS-components like 4000-logic circuits which are manufactured by bulk-CMOS process. In general latch-up does not appear in CMOS-circuits manufactured by epitaxial or CMOS/SOS processes. Some epitaxial components have, however, been reported to be sensitive to latch-up [18]. In CMOS/SOS components latch-up is not possible because the transistors are grown on a sapphire substrate which gives excellent isolation between transistors. Some other kinds of permanent damage have also been reported.

The linear energy transfer (LET) of an ion is the rate at which energy is deposited per unit pathlength of the ionising particle. The unit of LET is $MeVcm^2/mg$. The SEU sensitivity of a component is described by two main parameters. The first is the limiting cross section or saturated error rate which does not increase when the LET of the ions is increased. The second is the threshold LET which is the minimum LET required to produce a SEU. The two parameters are acquired for each component by bombing the component with ions from a cyclotron accelerator. In order to acquire the threshold LET various ions at various accelerating potential are used. The limiting cross section can be measured using simpler test equipment, eg. CASE which is based on Californium-252 radioactive source [20].

SEU is especially a problem in new high-integrity memory components and microprocessors because as the size of the transistors is decreased the less charge is needed to change the logic state.

Also multiple bit errors can be produced by a single ion if the LET of the ion is sufficient [12,21,22]. Double, triple, quadruple and quintuple errors have been observed. The share of multiple bit errors depends on the LET of the ion. For example at the worst case LET (least number of single bit errors) the share of single, double, triple and quadruple errors was 44%, 33%, 15% and 8% respectively for a 256 kbit static CMOS RAM manufactured by Hitachi [12]. Fortunately many memory chips are organized so that none of the bits in a single byte address are located in close physical proximity to another bit of the same byte. Thus the multiple errors are not usually in a single byte. This fact makes it possible to use error detection and correction (EDC) schemes.

Logic circuits are far less sensitive to SEU. The ranking of logic circuits is according to tests as follows with hardest components listed first: [19,23]

1. 4000-series CMOS and CMOS/SOS
2. Other CMOS (HC, HCT, SC, AHCT)
3. Standard bipolar TTL (54-series)
4. Other bipolar TTL (54L-, 54S-, 54F-series)
5. Low power schottky (54LS-series)
6. Advanced low power schottky and advanced schottky (54ALS-, 54AS-series)

5.1 Estimation of SEU rates

SEU's can be caused by energetic particles by direct ionisation or by fission products of nuclear reactions initiated by particles that originated outside the spacecraft. In the latter case the initiating particles are usually protons, and thus these kind of SEU's are significant especially in the inner radiation belt of the Earth. The particles causing direct ionisation originate from galaxy (galactic cosmic rays) or the Sun (solar flare particles). The solar activity affects both to solar flare particles and galactic cosmic rays. At solar maximum the solar flare particles are also at their maximum while the galactic cosmic rays are at their minimum. The number of solar flare particles can be reduced significantly using shielding of a few Al-mm. For example increasing shielding from 2.5 mm Aluminium to 10 mm decreses the number of solar flare particles whose LET is greater than 10 $MeVcm^2/mg$ to 1/30 [24]. By contrast, shielding is quite ineffective against galactic cosmic rays. For example, about 190 mm aluminium is needed to reduce the cosmic ray intensity by one order of magnitude.

The near-earth particle environment has been modelled based on data from satellite measurements. The models include galactic cosmic rays and solar flare particles. The LET spectrum inside a box with certain wall thickness can be calculated using these models when the orbit of the spacecraft is known. The upset rate (SEU's/day) of a component can be estimated using the limiting cross section and the LET-threshold of the component and the LET spectrum. A detailed estimation is quite complicated and it is usually done by computer programs.[25]

Analytic methods have been developed to estimate SEU rates and to compare components [26,27]. These methods are very useful in the selection of components because they are easy to use.

The expressions for SEU rate according to Binder [27] are:

$$R = (302 * s/L_c^2) * (1 - 0.64 * L_c^{-0.08}), \quad \text{when } 1 < L_c < 40,$$

$$R = (287 * s/L_c^2), \quad \text{when } L_c > 40,$$

where s is the limiting cross section in cm^2,
L_c is the threshold LET in $MeVcm^2/mg$ and
R is the SEU rate in errors/day.

The expressions above have been compared to experimental data and found to give results very close to the actual SEU rates. They can be used to estimate the SEU rate in deep space or in geosynchronous orbits during the maximum heavy ion flux in the 11 year solar cycle. During solar flares the rate can be 100-10000 times higher [24]. Table 2 contains results of our calculations according to Binder expressions for some interesting components. The cross sections and LET thresholds of the components are published in test reports of research institutes or component manufacturers.

Component type	SEU rate /day
(2k*8), RAM (stat.)	$3.5*10^{-6}$
(8k*8), RAM (stat.)	0.7
(256k*1), RAM (dyn.)	25
(32k*8), RAM (stat.)	15
T414, 32-bit CPU	0.009 (*)
80C86, 16-bit CPU	0.1
SBP9989, 16-bit CPU	10^{-3}-10^{-4}
logic chips	10^{-3}-10^{-6} or no upset
(8k*8), EEPROM	$1.7*10^{-5}$
(32k*8), EEPROM	no upset
(2k*8), CMOS PROM	$1.7*10^{-3}$
(1k*8), bipol.PROM	$3.4*10^{-7}$

(*) Assumed that the internal RAM and links are not in use.

Table 2. Calculated SEU rates for some digital components usable in computer systems.

5.2 Design rules to reduce SEU's

Some general design rules to reduce the probability of single event upsets in electronic circuits in space environment can be stated as follows:

1. Acquire data about limiting cross sections and LET thresholds of processor, memory components, other high density components and components manufactured with technology sensitive to radiation. Estimate the SEU rate of components using computer program or analytic method. Select components so that the SEU rate is acceptable for the project needs.

2. SEU's caused by solar flare particles can be reduced by shielding in environments where the shielding effect given by the magnetic field of the Earth (geomagnetic shielding) is neglible.

3. Shielding is not effective against galactic cosmic rays.

4. The combined effects of geomagnetic and material shielding must be considered. On some low altitude and low inclination Earth orbits a thin shielding can in some cases give a lower SEU rate than a thick shielding.[31]

5. It is best to ignore geomagnetic shielding for solar flare heavy ions because the effectiveness of geomagnetic shielding for solar flare heavy ions is uncertain. This conclusion is due to the results, which show that we cannot be certain of the ionic charge of solar flare ions at any energy. More data about the charge state of flare particles as a function of atomic number and energy is needed before the effectiveness of geomagnetic shielding can be estimated. [31]

6. Estimates of the SEU rate for orbits below 13 000 km given by the present models are probably too low because there may be significant amounts of heavier ions trapped in the inner radiation belt.[31]

6. Redundancy concept

In a typical scientific instrument, it is maybe not required to maintain continuous or uninterrupted operation. As well, there may be no need for 100 % data integrity. If temporary interrupts in operation are allowed together with some amount of errors in scientific data, hardware redundancy concept becomes significantly lighter. In this case, instead of fault masking, an error recovery procedure is sufficient. Hardware redundancy is thus not needed against soft errors. Here, a two- phase method may be followed: 1. temporary errors are managed by soft methods, possibly supported by hardware, and 2. permanent errors are managed by hardware redundancy, usually in combination with dedicated software functions. However, we want to point out, that although the basic idea is simple, software and hardware must be always considered together. In the following paragraphs, three important issues are treated: hardware fault tolerance, software fault tolerance, and functional and structural requirements for reliable onboard software.

6.1 Fault tolerant hardware

Principle of hardware redundancy is simple: in order to survive after hardware faults, we must have spare parts onboard (or functional subsystem to take over vital tasks, but this is another matter). It is well understood, that if fault masking is not required, cold spares are the best choice. There are several clear reasons for this: 1. a cold spare consumes no power, 2. an unbiased electronic module is known to be more reliable: a factor of ten is often used, and 3. unbiased components tolerate much higher radiation doses than biased ones. Figure 2 displays a comparison between different redundancy methods for a relatively long mission.

[figure omitted in online version]

Figure 2. Reliability with different kind of redundancy

First of all, the designer should consider whether redundancy is needed at all. This choice is not quite obvious, and careful analysis is needed. General reasons for redundant structures are: extended mission length, and specific reliability requirements. However, redundancy always adds extra complexity to the system, and the fault rate is always higher than for a non-redundant system. The task of redundant structures is to reduce the resulting system failure rate.

There is usually some portion of the system which is not possible to make redundant, known as "hardcore". In order to minimize the hardcore, a system level redundancy should be applied. On the other hand, component level redundancy gives best tolerance against multiple faults. A reasonable compromise may be a suitable module level redundancy. For a computer system, it is a common approach to let the bus be a hardcore.

It is interesting to consider effects of SEU on microprocessors. A most typical consequence is a change in program counter. This produces an uncontrolled jump, and indirectly may lead to a very long or endless loop. Other, less common consequences of SEU are program halt, and erraneous data. To prevent failure propagation and to reduce effects of this kind of error, the situation should be rapidly detected. A watchdog timer is frequently used to detect processor upsets. Other methods exist: program flow control by software or hardware monitors. [33]

6.2 Software fault tolerance

Software may contain three types of errors: first, there may be design errors, from specification, compiling, coding or loading phases of the software development cycle. Secondly, the program code may become erraneous during the flight, because of soft or hard faults in memory components carrying the code. And a third error source: program code may be overwritten, because of some distant software or hardware error.

In a non-critical instrument software, known methods against design errors like recovery blocks or N-version programming, are not needed: these methods are elaborate and introduce memory space and performance overheads. It is obviously quite sufficient to offer a possibility to repair or reload program sections by ground commands. Some hardware support may be necessary for this. Flight-time program updates, as well as operational parameters subjected for changing later on, may be conveniently stored in a non-volatile memory. The non-volatile storage may be a RAM memory with battery backup and write protection. An EEPROM memory would be ideal for non-volatile storage, if radiation and single event upset tolerance are sufficient. A bubble memory chip may be used as well. Ferrite core memories are bulky and technically obsolete.

To resist damages in the program store, following methods may be used:

- detection of memory faults
- program or data memory reallocation
- sufficient redundancy, at least for vital parts of the software
- error detection and correction hardware (for bitwide and bytewide memories)
- switchable memory chips (for bytewide chips)
- protection unit
- write protection

(One should notice, that error correction and memory protection methods are as well effective against soft errors, like cosmic ray induced single event upsets). Redundant memory modules could be distributed in the address space of the processor, or they may be switched on and off by a special hardware.

Software should have a proper structure for efficient reconfiguration in a faulty hardware. A basis of this approach is a clear task decomposition and a method to manage these tasks. In the event of permanent memory faults, tasks should be deallocated, to avoid faulty memory modules. Passivation of (faulty) tasks may be used as well. Task reallocation requires certain addressing methods to be used- or a memory mapping hardware. Passivation may be effective in combination with reallocation, new space could be arranged by passivating less important modules.

It is clear that certain parts of the software form a kind of hardcore: the telemetry command interpreter and the task manager/scheduler. This hardcore may be protected by memory redundancy or by sufficient radiation hardness.

7. Examples of some space computer projects

In this chapter component selection for two space computers are described. Both computers are data processing units (DPU's) of scientific instruments. The instruments are Promics-3 to be flown on USSR Interball satellites and ERNE, to be flown on ESA's Soho satellite.

The processor of the DPU of Promics-3 was chosen to be SBP9989, manufactured by Texas Instruments. The main reason for the choice was that tolerance for both total dose and SEU's is very good (see tables 1 and 2). The radiation tolerance requirement of the auroral Interball satellite is quite demanding, about 45 krad/year inside shielding of 4 mm Al. The radiation tolerance of SBP9989 depends on the injection current and clock frequency. These operating conditions were selected so that the radiation tolerance is good and the processing speed is acceptable. The injection current used was 350 mA and the clock frequency was 3 MHz. Other reasons leading to choice of SBP9989 were that it has been used in many previous space projects and is found to be reliable.

Bipolar PROM chips of size 4k*8 were selected as program memory. They were organized as 8k*16 memory system. The reason was the total dose tolerance requirement. The program was loaded to CMOS RAM after power-up sequency and the PROM's were switched off in order to save power.

Intel MC51C98 and Cypress CY7C164 16k*4 CMOS RAM's were tested by VTT as potential RAM candidates for Promics-3 DPU [32]. The total dose tolerance of the chips was found to be 10-20 krad, which is insufficient for the Interball mission. After the tests HM65641 8k*8 RAM's became available. Their standby current is within specifications after at least 30 krad and they are functional far beyond that. By utilising extra shielding given by adjacent printed circuit boards this tolerance was acceptable. The SEU rate due to worst case cosmic rays for a 16k*16 memory system is about 2.8 SEU/day. This is quite high but can be accepted for a scientific instrument. HM65641 is manufactured by epitaxial process and latch-up has not been detected.

ERNE instrument is a particle detector to be flown on Soho in 1995. The requirement for total dose tolerance is not as stringent as in Promics-3. Total dose is estimated to be 12 krad during the extended 6 year mission inside shielding of 4 mm Al. SEU is a serious problem in ERNE, because SEU's are most likely to happen during large solar flares, which are the most interesting objects to be studied by ERNE.

MAS281 manufactured by Marconi Electronic Devices Ltd. was selected for the processor for ERNE because of its good SEU tolerance, fast computing speed and low power consumption. MAS281 is manufactured by same CMOS/SOS process as MAS6116 RAM's, which are extremely resistant to SEU's. The computing speed is about 2-3 times faster than that of 80C86 depending on application. The power consumption of the processor is typically about 350 mW. Other alternatives for processor

of ERNE were Inmos Transputer T414 and Harris 80C86. T414 was attractive due to its performance. The performance is greatly due to the use of fast internal RAM. The RAM was found to be sensitive to SEU's and thus lower speed external RAM would have to be used instead of the internal RAM. This reduced the performance of T414 so that it was not significantly better than MAS281. Also the CPU of T414 is quite sensitive to SEU's (table 2). 80C86 was not chosen, because of its insufficient speed and sensitivity to SEU's.

SEEQ 28C256 EEPROM was selected for program memory because of its good SEU tolerance, low power consumption and high density. The chip contains 32k*8 bits. MAS6116 chips are used as data and partly as program memory. MAS6116 contains 2k*8 bits. 16 chips are organized as 16k*16 RAM. The expected SEU rate for the memory system due to cosmic rays is $16*3.5*10^{-6}=5.6*10^{-5}$ per day. Even during a large solar flare if the number of particles is 1000 times more than pure cosmic rays the SEU rate is only $5.6*10^{-2}$/day. This means that SEU's are extremely rare in RAM's and error correction and detection is not needed.

8. Discussion

Component selection for radiative environment, balanced with redundancy and protection concepts is a basic issue in space computer design. Tolerance against cosmic radiation is characterized by the total dose tolerance and single event upset sensitivity, which are not necessarily related. Total dose tolerance may be improved by reducing operation time under bias and by external shielding. Single event upset rate estimation appears to be extremely important. Solar flares introduce a hazard for computer constructions which are susceptible for SEU. During a large flare, SEU rate may be as much as 10 000 times higher than on average. High enough SEU rate produces multiple errors to memories, thus reducing efficiency of hardware error correcting schemes. If the microprocessor is sensitive to SEU, error recovery overhead may become excessive during high SEU rates. Protection methods in form of redundancy, error detection and recovery, or other schemes, should be planned simultaneously with parts selection. By allowing some amount of data errors and computer restarts, hardware overhead may be reduced.

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