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Multi-component high-*K* gate dielectrics for the silicon industry

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Abstract

The exponential growth of the silicon industry can be attributed to that fact that silicon has a native oxide that is silicon dioxide. With SiO_2 soon approaching its fundamental limit, we must find an alternate to SiO_2 or a new switch to replace MOSFETs. In this paper we focus on the leading alternate gate dielectrics. We first discuss the selection criteria for alternate gate dielectrics and why it is important to have an amorphous gate dielectric. SiO_2 and aluminum oxide remain amorphous at very high temperatures. For dielectrics with $K > 15$ and gate power < 100 mW/cm^2, it may be necessary to stabilize the amorphous phase of metal oxides by adding Al or Si to the oxide, thus forming multi-component dielectrics such as aluminates. We then benchmark aluminates with aluminum oxide and silicon dioxide.

Keywords: Gate dielectric; Scaling; High-*K* dielectrics; Aluminum oxide and aluminates

1. Introduction

The basis of the trillion-dollar semiconductor industry or ''silicon age'' is that silicon has a native oxide that is silicon dioxide. To achieve high performance (M-MIPS), high density (GBits) and low power CMOS technology, silicon dioxide has been hyper-scaled to 1.5–1.8 nm, soon approaching its fundamental limit [1]. Many high-*K* gate dielectrics (metal oxides) are being investigated as an alternate to SiO_2. There is a loaded question facing the silicon industry today: when high *K*, what *K* and what dielectric? [2]. The simple-minded answer to this complex question would depend on the technology node. If we decide to replace SiO_2 at $t_{eq} > 1.3$ nm, the leading contenders are doped aluminum oxide [3–6] or silicates [7]. For the silicon industry beyond the 70 nm node (for $t_{eq} < 1.3$ nm), we may need gate dielectrics with $K > 15$ and aluminates may the right choice [8,9]. In this paper we first discuss the criteria to select alternates to SiO_2 and with that in mind we then benchmark the dielectric and interface properties of SiO_2, aluminum oxide and aluminates.

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2. Dielectric selection

As we scale the technology beyond 70 nm node and therefore SiO_2 thickness to less than 1.5 nm, the direct tunneling current though the gate stack becomes very high (>1 A/cm^2). For low power applications the acceptable power dissipation through the gate stack should be less than 100 mW/cm^2 [2]. Therefore, for the 70–50 nm technology nodes we need to replace SiO_2 with $K>8$ and for technology dimensions less than 50 nm we need to search for an alternate gate dielectric with $K>15$. The gate dielectric should meet the following fundamental/practical requirements:

- thermodynamic stability on silicon with respect to formation of SiO_2 and MSi_x;
- amorphous after device integration, implying that the dielectric should remain amorphous after S/D/poly activation;
- low conduction for low leakage and low power. For metal oxides, it is well known that band-gap/band-offset is inversely related to K (with aluminum oxide as an exception). A low leakage current implies a large band-offset for electrons and holes. The figure of merit is $K\times(\Phi_B)^{3/2}\times(m^*)^{1/2}>10$ (a.b.u.);
- high carrier mobility at the dielectric/Si interface. Therefore, low D_{it} ($<2\times10^{11}$/cm^2 eV^{-1}). Therefore, a low bulk charge or a low effective fixed charge at the dielectric/Si interface;
- high breakdown strength and acceptable reliability. For metal oxides, breakdown strength is inversely related to K.

Most metal oxides become polycrystalline at relatively low temperatures (<500°C). Polycrystalline dielectrics have a non-uniform leakage distribution and can give rise to large statistical variation for nanometer devices across the chip. Therefore, replacement gate strategies have been proposed to prevent crystallization and deleterious effects of mass and electrical transport along grain boundaries [8]. However, the economics of this industry may not permit a new process structure and also an alternate gate dielectric. Therefore, it is essential to invent an alternate gate dielectric remaining amorphous after device integration. Doped aluminum oxide, aluminates and silicates are likely to meet these challenges. The purpose of scaling is to increase the drive current. Therefore, at the end of the day, the devices made with the selected dielectric should have carrier mobility at the dielectric–silicon interface comparable to the mobility at the Si/SiO_2 interface and acceptable low leakage/power across multi-billion devices on 300 mm wafers.

3. Why doped aluminum oxide/metal oxides for the gate dielectric?

Aluminum oxide is not a novel dielectric! Aluminum oxide has been proposed for various IC applications, including a gate dielectric for metal-gate PMOS devices manufactured in the early 1970s [10]. The characteristics of aluminum oxide are listed in Table 1. It has a dielectric constant of $K\sim10$, with a large band-gap and, more importantly, it has a large band-offset, giving rise to a figure of merit of >10. Aluminum oxide remains amorphous at $T>900$°C and also the oxygen diffusion rate through aluminum oxide is very low. Due to the large band-gap and band-offset (>2 eV), aluminum oxide has a very low leakage current density.

The early work on aluminum oxide was performed on relatively thick films (>10 nm). To evaluate

Table 1
Characteristics of dielectrics

	Dielectric				
	SiO_2	Al_2O_3	HfO_2	ZrO_2	$ZrSi_xO_y$
K	3.82	9.5	20–25	20–25	10–12
Band gap,	9	8.8	4–5	5.8	~6
Φ_B (eV)	3.2	>3	?	>1	>1
E_{bd} (MV/cm)	>10	~10	?	4–5	~10
Amorphous phase stab.	High	High	Low	Low	?
Oxygen diff. 950°C (cm^2/s)	2×10^{-14}	5×10^{-25}	?	10^{-12}	?

the characteristics of thin films (3–10 nm), aluminum oxide was deposited using the reactive target sputtering method with a Varian M2000. A pure (MOS grade) Al target (as opposed to an alumina target) was used as the source and sputtering was carried out in a partial oxygen/argon ambient. The plasma glow was achieved with a DC pulse power supply between the cathode and anode. During deposition, the substrate temperature was 380°C, the deposition rate was ~0.11 nm/s and uniformity was better than 2% across an 8 in. wafer. To fabricate doped aluminum oxide films, the pure Al target was replaced by a doped-Al target made with the specified dopant concentration (Zr or Si, 0.5–5 wt.%). After deposition, the films were annealed at various temperatures (550–900°C) in oxygen, nitrogen or argon gas.

For doped and un-doped aluminum oxide films, the conduction and interface characteristics were measured on large area capacitors. As shown in Figs. 1 and 2, the addition of 0.5% Zr or 1% Si to the Al target reduces the measured leakage current to $<10^{-13}$ A/mm^2. The addition of dopants also reduces the mid-gap interface-trap density to $<5\times10^{10}/cm^2$-eV at the dielectric/Si interface without inserting SiO_2 between Si and aluminum oxide. The addition of these dopants does not have a significant effect on the tunneling turn-on field (Fig. 3) or the breakdown strength of the dielectric

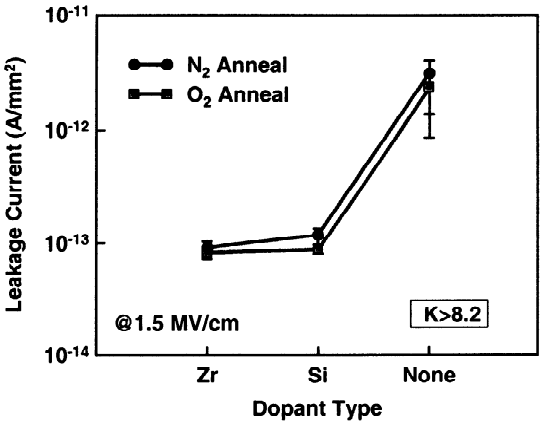

Fig. 1. Conduction characteristics of doped and un-doped PVD aluminum oxide films deposited directly on silicon with HF last treatment. Film thickness, 10 nm.

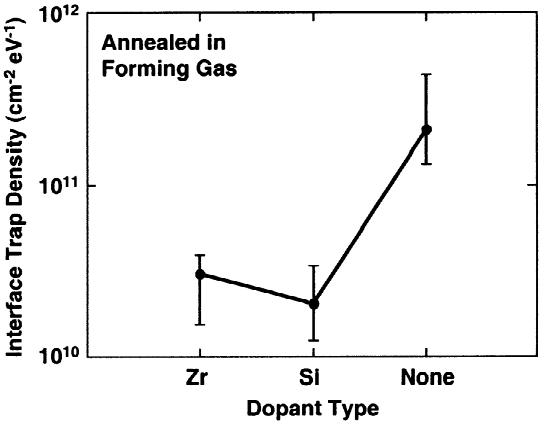

Fig. 2. Interface characteristics of doped and un-doped PVD aluminum oxide films deposited directly on silicon with HF last treatment. Film thickness, 10 nm.

(Fig. 4), implying that these dopants are not generating electrically active trap levels at the interface or in the bulk of the aluminum oxide film. The concept of doping was discovered by experimental serendipity. Our further thinking and previous theoretical work performed on glasses suggest that dopants act as network modifiers and therefore quench the dangling bonds of excess oxygen in aluminum oxide or metal oxides and therefore reduce the conduction current and the interface state density. Network modifiers can also stabilize the amorphous phase of metal oxides.

The gate dielectric should have acceptable characteristics at the capacitor level and, more importantly, these characteristics should remain intact after device integration. Doped and un-doped aluminum oxide are stable during poly-silicon deposition. The gate-stack can be patterned with dry etching. The gate-stack with aluminum oxide is compatible with the standard self-aligned CMOS technology. However, doped and un-doped aluminum oxide have a high fixed charge ($5–10\times10^{12}$/

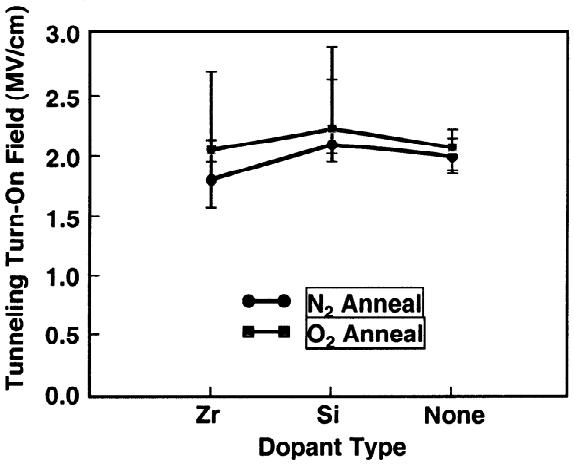

Fig. 3. Tunneling turn-on field for doped and un-doped aluminum oxide. The presence of dopants does not affect the tunneling characteristics of doped aluminum oxide.

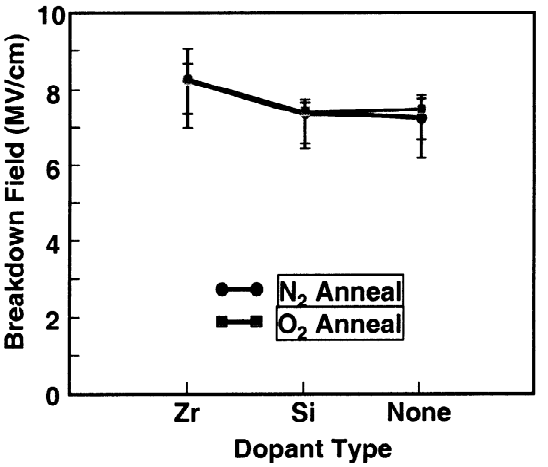

Fig. 4. Breakdown strength of doped and un-doped aluminum oxide films. The presence of dopants in the aluminum oxide does not have a significant effect on the statistical breakdown field values.

cm^2) and therefore reduced electron mobility. Even aluminum oxide deposited with the state-of-the-art ALCVD has a large amount of fixed charge and therefore reduced mobility [5]. The fixed charge may be one of the critical show-stoppers for aluminum oxide to qualify as an alternative to SiO_2.

4. Multi-component high-*K* gate dielectrics

For $t_{eq} < 1.3$ nm, aluminum oxide may face a scaling challenge and therefore we may need an alternate gate dielectric with $K > 15$. As shown in Table 1, ZrO_2 and HfO_2 have the right K and figure of merit, but do not remain amorphous at $T > 500$°C. On the other hand, SiO_2 and aluminum oxide remain amorphous to very high temperatures. To stabilize the amorphous phase of ZrO_2 or HfO_2, we can either add the minimum necessary SiO_2, thus forming a multi-component dielectric silicate, or we can add the minimum necessary aluminum oxide, thus forming a multi-component dielectric aluminate. The silicates may have the desired interface characteristics and may also have have a low fixed charge [7]; however, due to the very low dielectric constant of SiO_2, silicates with $K < 10$ may face the same scaling challenge as aluminum oxide. For $K > 15$, aluminate may be the right choice.

To evaluate the characteristics of aluminates, dielectrics with varying concentrations of aluminum were deposited using an off-axis sputtering system. The deposition was carried out on either silicon substrates or on thin metal films on silicon substrates. Figs. 5 and 6 show the X-ray diffraction patters of thick (~80 nm) hafnium and zirconium aluminates. For hafnium aluminates, the crystalline phase is stable down to 70% Hf after annealing at 800°C for 30 min. However, for zirconium, the amorphous phase is stabilized by 30% Al after the same anneal. Fig. 7 shows the K values for zirconium and hafnium aluminates. These K values indicate that zirconium aluminate is a preferred dielectric over hafnium aluminate. To achieve a high K value, we chose a high Zr/Al ratio and added a small amount of silicon as a network modifier to reduce traps and further stabilize the amorphous phase at high temperature. Zirconium oxide is known to have a very high oxygen diffusion rate. During process integration, oxygen can diffuse through the dielectric and react with the underlying silicon, thereby

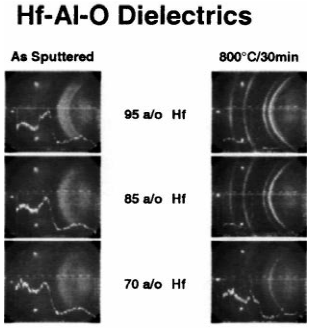

Fig. 5. X-ray diffraction patterns of Hf aluminates. The crystalline phase is stable down to 70% Hf, after 800°C/30 min.

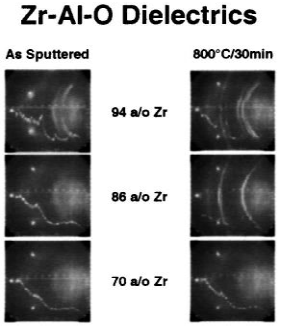

Fig. 6. X-ray diffraction patterns of Zr aluminates. The amorphous phase is stabilized by 30% Al, even after 800°C/30 min.

reducing the effective *K*. As shown in Fig. 8, the addition of Al also reduces the rate of oxygen diffusion through the aluminate. As shown in Figs. 5–8, for Al concentrations between 25 and 35 at.%, one obtains an amorphous dielectric with *K* between 18 and 20 with a reduced rate of oxygen diffusion.

The above dielectric optimization was performed on relatively thick films (~80 nm). To evaluate

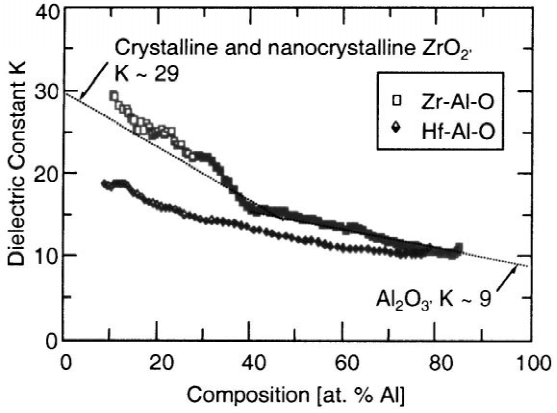

Fig. 7. Dielectric constant, *K*, for Hf and Zr aluminates as a function of Al content.

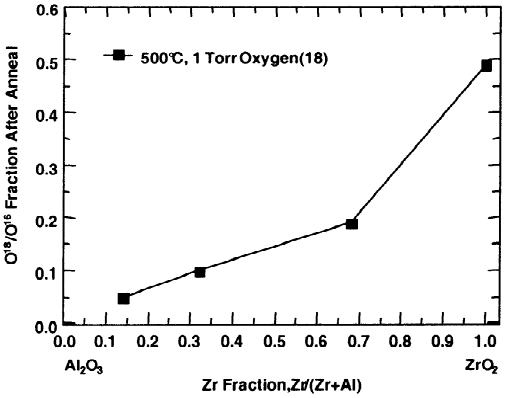

Fig. 8. Oxygen diffusion through Zr aluminates (O^{18} isotopic replacement experiment).

thin films of Zr–Al–Si–O, a composite target of Zr–Al–Si was made for an 8 in. sputtering system. Ultra-thin metal films (1–2 nm) were deposited on silicon with uniform 0.5 nm SiO_2 or Si–O–N films. The metal was oxidized at low temperatures and subsequently annealed in nitrogen at high temperatures. It was found that the dielectric with this composition reacts with poly-silicon and therefore is not compatible with the poly-silicon gate. To make gate stacks with zirconium aluminate, reactively sputtered films of TiN were deposited directly on the dielectric and the gate stack was dry etched in Cl_2/BCl_3. For dielectric evaluation, long channel NMOS devices were fabricated with the standard CMOS technology (S/D activation by RTA at 1050°C). As shown in Fig. 9, the gate dielectric (zirconium aluminate) retains the amorphous phase after standard device integration and therefore does not require replacement gate technology. NMOS devices made with Zr–Al–Si–O/TiN gate stacks were benchmarked with NMOS devices made with 1.5 nm Si–O–N or 3 nm SiO_2 using either TiN or poly-silicon gates. It was found that the evaluated composition of Zr–Al–Si–O was not compatible with the poly-gate. Fig. 10 shows the conduction characteristics of TiN/Zr–Al–Si–O/Si gate stacks. The gate dielectric can be scaled to $t_{eq} \sim 1.2$ nm with a leakage current density of less than 50 mA/cm^2 and a gate power of less than 5 mW/cm^2 at 1 V, both almost a factor of 100 less than the equivalent thickness of Si–O–N or SiO_2. The conduction characteristics have a very weak temperature dependence and the leakage remains low even at $T > 150$°C, indicating a low bulk trap

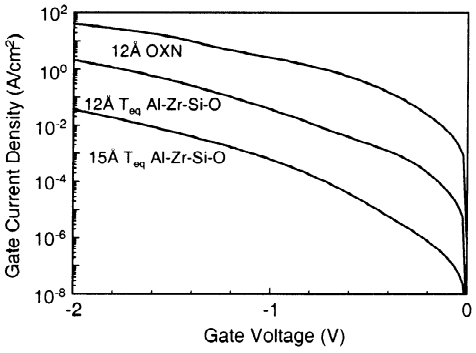

Fig. 9. HRTEM of TiN/Zr–Al–Si–O/Si gate stacks.

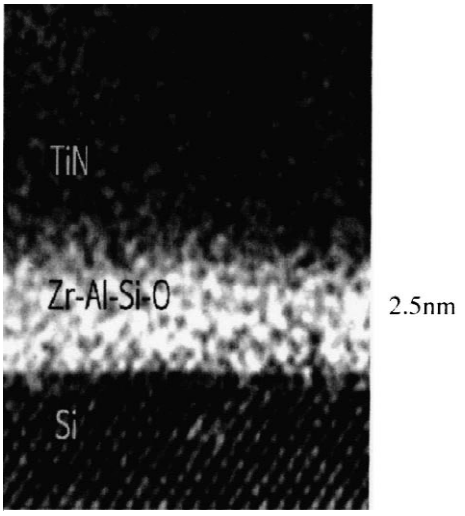

Fig. 10. Conduction characteristics of TiN/Zr–Al–Si–O/Si and TiN/OXN/Si gate stacks.

density in Zr–Al–Si–O films. Thin films of Zr–Al–Si–O have a high breakdown strength (>6 MV/cm). The interface-state D_{it} depends on the starting substrate (Si, SiO_2 or Si–O–N). The measured value at the dielectric/Si interface is in the range $1–5\times10^{11}/cm^2$. These values of D_{it} indicate that a forming gas anneal does work on zirconium aluminates. However, these Zr–Al–Si–O films have a high fixed charge of $>5\times10^{11}/cm^2$ and therefore the measured mobility is a factor of 2 less than devices made with SiO_2.

5. Critical issues and conclusions

- The characteristics of aluminum oxide are very similar to those of SiO_2. It remains amorphous at high temperatures. It is thermodynamically stable on silicon. It has a band-offset of >2 eV and therefore exhibits a very low leakage current density with a poly-silicon gate. Furthermore, the addition of dopants reduces the conduction current and also reduces the interface state density ($<10^{11}/cm^2$-eV). Using ALCVD, aluminum oxide can be scaled to a thickness of ~1.3 nm. However, doped and un-doped aluminum oxide deposited by PVD or ALCVD films have a fixed charge density ($>10^{12}/cm^2$) and therefore a reduced carrier mobility at the dielectric/Si interface. The fixed charge remains a critical show-stopper for aluminum oxide to move into manufacturing.
- For $t_{eq}<1.3$ nm, multi-component dielectrics such as aluminates may be a viable choice to achieve $K>15$ and a stable amorphous phase without switching to replacement gate technologies. The zirconium aluminates investigated in this work show an amorphous phase even after S/D activation with standard CMOS technology. After full device integration with a TiN gate, zirconium aluminate can be scaled to a thickness of <1.2 nm with a leakage current density of <50 mA/cm^2 and a gate power of <5 mW/cm^2 (gate area is 10% of the chip area). However, the investigated zirconium aluminate composition is not compatible with a poly-silicon gate. Recent research indicates that hafnium oxide is more compatible with a poly-silicon gate; therefore, for

$t_{eq} < 1.3$ nm, hafnium-based multi-component dielectrics may emerge as leading contenders to replace SiO_2.

- Finding an alternative to SiO_2 is an enormous challenge for the materials, device and integration research community. Dielectric/Si interface control remains the critical show-stopper for high K to move into IC manufacturing.

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