A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter

Andrew M. Abo and Paul R. Gray, *Fellow, IEEE*

***Abstract*—A 1.5-V, 10-bit, 14.3-MS/s pipeline analog-to-digital converter was implemented in a 0.6-μm CMOS technology. Emphasis was placed on observing device reliability constraints at low voltage. MOS switches were implemented without low-threshold devices by using a bootstrapping technique that does not subject the devices to large terminal voltages. The converter achieved a peak signal-to-noise-and-distortion ratio of 58.5 dB, maximum differential nonlinearity of 0.5 least significant bit (LSB), maximum integral nonlinearity of 0.7 LSB, and a power consumption of 36 mW.**

***Index Terms*—Analog to digital, low voltage, reliability.**

I. Introduction

In mixed-mode analog-to-digital (A/D) interfaces, there are many applications where a video-rate A/D converter (ADC) is integrated with complex digital signal-processing (DSP) blocks in a compatible, low-cost technology—particularly CMOS. Such applications include camcorders, wireless local-area-network transceivers, and digital set-top boxes.

Advances in CMOS technology, however, are driving the operating voltage of integrated circuits increasingly lower. One forecast of operating voltages for CMOS technology is shown in Fig. 1 [1]. From this general trend, it is clear that circuits will need to operate at 1.5 V and below within a decade [1], [2]. One of the main issues driving this reduction in voltage supplies is device reliability. Therefore, as device dimensions shrink, the applied voltages will need to be proportionately scaled in order to guarantee long-term reliability.

The voltage limitations of the technology dictate that integrated ADC's operate at the same low voltage as the digital circuitry. Furthermore, in achieving low-voltage operation, the reliability constraints of the technology must not be violated. Previous low-voltage, video-rate ADC's have either used clock multiplication techniques that introduce potential reliability problems [3] or utilized special enhancements to the CMOS technology such as low-threshold devices [4] or BiCMOS [5]. This paper describes a 1.5-V, 10-bit, 14.3-MS/s, pipeline ADC that avoids reliability problems. It was also implemented in a CMOS technology with standard threshold voltages.

II. Pipeline-ADC Architecture

The ADC uses a pipeline 1.5-bit/stage architecture with nine stages, as shown in Fig. 2. Each stage resolves two bits with a sub-ADC, subtracts this value from its input, and amplifies the resulting residue by a gain of two. The stages are buffered by switched-capacitor gain blocks that provide a sample-and-hold between each stage, allowing concurrent processing. The resulting 18 bits are combined with digital correction to yield ten bits at the output of the ADC.

This architecture has been shown to be effective in achieving high throughput at low power [3], [6]. The low number of bits per stage coupled with digital correction relaxes the constraints on comparator offset voltage and dc op-amp gain.

The implementation of each pipeline stage is shown in Fig. 3. Although a single-ended configuration is shown for simplicity, the actual implementation was fully differential. A common, switched-capacitor implementation [3] was chosen, which operates on a two-phase clock. During the first phase, the input signal V_i is applied to the input of the sub-ADC, which has thresholds at $+V_{\rm ref}/4$ and $-V_{\rm ref}/4$. The input signal ranges from $-V_{\rm ref}$ to $+V_{\rm ref}$ (differential). Simultaneously, V_i is applied to sampling capacitors C_s and C_f. At the end of the first clock phase, V_i is sampled across C_s and C_f, and the output of the sub-ADC is latched. During the second clock

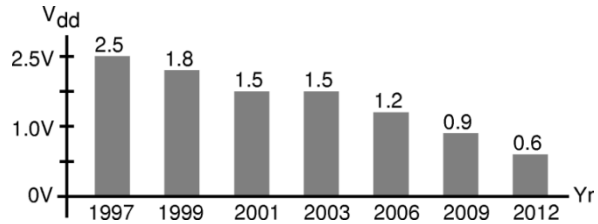

Fig. 1. Semiconductor Industry Association 1997 forecast of CMOS voltage supply.

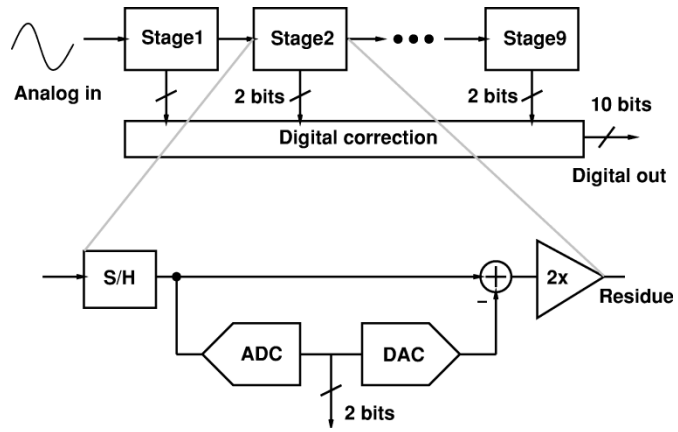

Fig. 2. Pipeline-ADC 1.5-bit/stage architecture.

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The authors are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA.

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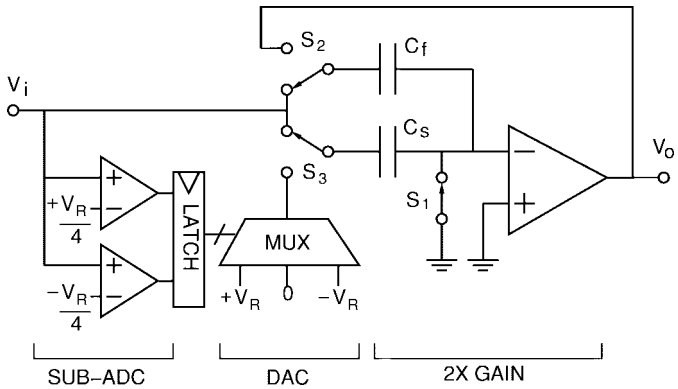

Fig. 3. Switched-capacitor implementation of each pipeline stage.

phase, C_f closes a negative feedback loop around the op-amp, while the top plate of C_s is switched to the digital-to-analog converter (DAC) output. This configuration generates the stage residue at V_o. The output of the sub-ADC is used to select the DAC output voltage $V_{\rm dac}$ through an analog multiplexor. $V_{\rm dac}$ is capacitively subtracted from the residue, such that

$$V_o = \begin{cases} \left(1+\dfrac{C_s}{C_f}\right)V_i - V_{\rm ref}, & \text{if } V_i > V_{\rm ref}/4 \\ \left(1+\dfrac{C_s}{C_f}\right)V_i, & \text{if } -V_{\rm ref}/4 \le V_i \le +V_{\rm ref}/4. \\ \left(1+\dfrac{C_s}{C_f}\right)V_i + V_{\rm ref}, & \text{if } V_i < -V_{\rm ref}/4 \end{cases}$$

In the 1.5-bit/stage architecture, $C_s = C_f$ is chosen to give a gain of two in the transfer function. The DAC levels can be generated from a single differential reference because the negative reference and differential zero are readily available by using the reverse polarity or shorting the outputs together.

A precision interstage gain is required to achieve the desired overall ADC linearity. Because the capacitor ratio C_s/C_f determines this interstage gain, capacitor matching is critical. In the prototype, a capacitor trim array was used to ensure better than 0.1% matching. This array could be set either manually or automatically with a self-calibration scheme [9]. Also, the dc op-amp gain must be sufficiently large (>60 dB) to reduce finite gain error. Last, the op-amp must settle to better than 0.1% accuracy in one clock phase (one half-cycle). It is this settling time that limits the overall pipeline throughput.

III. Low-Voltage, Switched-Capacitor Design Issues

The reduction in supply voltage introduces several factors that complicate the design of low-voltage, analog circuits. This discussion focuses specifically on CMOS switched-capacitor circuits.

As the supply voltage is scaled down, the voltage available to represent the signal is reduced; therefore, dynamic range becomes an important issue. To maintain the same dynamic range on a lower supply voltage, the thermal noise in the circuit must also be proportionately reduced. There exists, however, a tradeoff between noise and power consumption. Because of this strong tradeoff, it will be shown that under certain conditions, the power consumption will actually increase as the supply voltage is decreased.

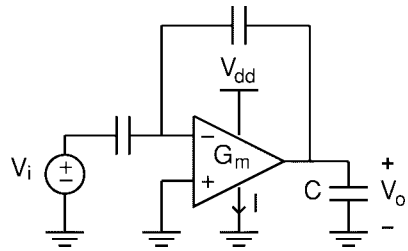

Fig. 4. Typical class-A, switched-capacitor circuit.

Consider the typical switched-capacitor circuit shown in Fig. 4. It consists of a class-A, operational transconductance amplifier (OTA) operating from a supply voltage $V_{\rm dd}$ with a static bias current I. The OTA is configured with capacitive negative feedback and drives a fixed capacitive load. For high-resolution applications, the dynamic range of such a circuit is often limited by thermal noise. If the circuit is then optimized for minimum power, it can be shown that the power will tend to increase as the supply voltage is lowered [7]. This result can be seen from four simple assumptions. First, the power in the circuit is the static bias current times the voltage supply

$$P \propto I \cdot V_{\rm dd}. \tag{1}$$

Second, if the OTA can be modeled as a single transistor, then the bias current is proportional to the transconductance times the gate overdrive

$$I \propto g_m \cdot (V_{\rm gs} - V_t). \tag{2}$$

Third, the closed-loop bandwidth of the circuit must be high enough to achieve the desired settling accuracy at the given sampling rate f_s

$$\frac{g_m}{C} \propto f_s. \tag{3}$$

Last, the dynamic range (DR) is proportional to the signal swing $\alpha V_{\rm dd}$ (where $0 < \alpha < 1$) squared over the sampled kT/C thermal noise. α represents what fraction of the available voltage supply is being utilized

$$\text{DR} \propto (\alpha V_{\rm dd})^2 \Big/ \frac{kT}{C}. \tag{4}$$

From these assumptions, it follows that for a given dynamic range and sampling rate, the power will be inversely proportional to the supply voltage $V_{\rm dd}$ (5). Furthermore, the power is inversely proportional to the square of fractional signal swing α. Although the supply voltage is a fixed constraint of the technology that cannot be modified, the circuit designer can choose α. Therefore, to minimize power consumption, it is important to use circuits that maximize the available signal swing α

$$\Rightarrow P \propto kT \cdot \text{DR}\left(\frac{V_{\rm gs} - V_t}{\alpha^2 V_{\rm dd}}\right) \cdot f_s. \tag{5}$$

Another critical problem in designing switched-capacitor circuits on a low-voltage supply is the difficulty of implementing MOS switches. Typically, in a switched-capacitor

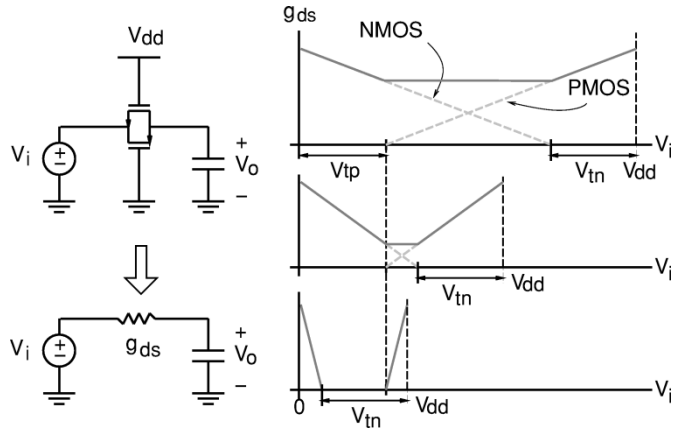

Fig. 5. Conductance of MOS switches.

circuit, an analog input signal V_i is sampled through a MOS switch or transmission gate, as shown in Fig. 5. Ideally, the switch in the on-state acts as a fixed linear conductance $g_{\rm ds}$. In practice, the conductance of the switch varies with the signal voltage, as shown in Fig. 5. Plotted in the figure is the switch conductance versus input signal V_i for three different supply voltages. The dashed line shows the individual conductances of the NMOS and PMOS devices, and the solid line shows the effective parallel conductance. In the top case, $V_{\rm dd}$ is much larger than the sum of the two threshold voltages $V_{\rm tn}$ and $V_{\rm tp}$. In this case, it easy to achieve a large on-conductance from rail to rail for V_i. In the middle case, $V_{\rm dd}$ is comparable to the sum of the threshold voltages, and there is a substantial drop in conductance when V_i approaches $V_{\rm dd}/2$. Last, in the bottom case, where $V_{\rm dd}$ is less than the sum of the two threshold voltages, there is a large range of V_i for which the switch will not conduct. Previous work [3], [8] has addressed this problem by using voltage-boosting circuits that subject devices to large terminal voltages. This technique, however, introduces potential long-term oxide reliability problems. Section IV introduces an alternate approach to this problem.

Last, operational amplifiers become more difficult to implement at low voltage. Section IV describes a folded-cascode, common-source cascade that achieves gain and bandwidth sufficient for moderate-resolution video-rate applications.

IV. Low-Voltage Circuit Techniques and Reliability

To design within the reliability limits of the technology, it is important to understand the mechanisms of device breakdown. Oxide breakdown, gate-induced drain leakage, hot-electron effects, and punch-through can all cause CMOS circuit failure. A CMOS technology is typically designed such that all these failure modes occur at a similar stress level, which is an important factor in determining the rated supply voltage. Therefore, if the following device voltages are kept within the rated supply voltage, a long circuit lifetime can be assured with high confidence.

Instantaneous and time-dependent gate-oxide breakdowns limit the gate-source and gate-drain potential differences that can be applied to a transistor (6) [15]. $E_{\rm bd}$ is the electric field in the oxide that causes breakdown. For a circuit lifetime of 30 years, $E_{\rm bd}$ is typically 5 mV/cm [14]. $t_{\rm ox}$ is the gate-oxide thickness. As the oxide voltage $V_{\rm ox}$ increases beyond $E_{\rm bd}$, the lifetime of the oxide decreases exponentially, as shown in (7), where $\tau_0(T) \approx 10^{-11}$ s and $G(T) \approx 350$ mV/cm for $T = 300$ K

$$V_{\rm ox} < E_{\rm bd} \cdot t_{\rm ox} \tag{6}$$

$$t_{\rm BD} = \tau_0(T) e^{G(T) t_{\rm ox}/V_{\rm ox}}. \tag{7}$$

Similarly, gate-induced drain leakage (GIDL) tunneling current limits the voltage across the oxide (8) [16], where $E_{\rm gidl}$ is electric field in the oxide that induces tunneling (typically 4 mV/cm), 1.2 V is the bandgap voltage, and $V_{\rm FB}$ is the MOSFET flat-band voltage (approximately 0 V for n+ poly over n+ drain; and 1.1 V for n+ poly over p+ drain)

$$V_{\rm gd} < E_{\rm gidl} \cdot t_{\rm ox} + 1.2V - V_{\rm FB}. \tag{8}$$

When the device is on, hot-electron effects can damage the device and degrade performance over time [16], limiting the $V_{\rm ds}$ and $V_{\rm gs}$ that can be applied. This constraint is described by (9), where $V_{\rm dsat}$ is the saturation voltage of the device (which is a function of bias and channel length L), E_c is the critical field, $l_{\rm LDD}$ is the effective length of the lightly doped drain and X_j is the drain/source junction depth

$$V_{\rm ds} < V_{\rm dsat}(L) + E_c \cdot (l_2 + l_{\rm LDD}) \tag{9}$$

$$l_2 = 0.2 t_{\rm ox}^{1/3} X_j^{1/2}. \tag{10}$$

Similarly, punch-through limits the magnitude of $V_{\rm ds}$ when the device is off, as described by (11), where $N_{\rm sub}$ is the substrate doping concentration

$$V_{\rm ds} < V_p \propto \frac{N_{\rm sub} L^3}{X_j + 3t_{\rm ox}}. \tag{11}$$

If these critical terminal voltages $V_{\rm gs}$, $V_{\rm gd}$, and $V_{\rm ds}$ are kept within the rated operating voltage $V_{\rm dd}$ of the technology, device reliability can be assured. Furthermore, these terminal voltages are only relative *to each other* and not to an absolute reference such as ground. Therefore, for example, the absolute V_g referenced to ground may exceed the rated $V_{\rm dd}$ if $V_{\rm gs} < V_{\rm dd}$ is maintained. This fact has been exploited in implementing the low-voltage MOS switch described below. Care must be taken, however, that the source-to-substrate and drain-to-substrate junctions do not exceed reverse breakdown voltages. These voltages are referenced to absolute ground (assuming a grounded substrate). This reverse breakdown, however, is typically much larger than the supply because the substrate is doped much less than the drain and source diffusions.

A. Reliable, High-Swing MOS Switch

Transmission gates were used extensively in the switched-capacitor gain stages of the pipeline. Because the threshold voltages of the NMOS and PMOS transistors were 0.7 and 0.9 V, respectively, conventional transmission gates with any usable signal swing were not directly realizable. Therefore, a bootstrapped switch was required. Earlier bootstrap implementations [3] resulted in (relative terminal) voltage stress that exceeded the supply by a large margin. In this work, a

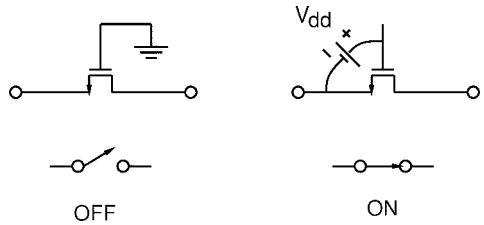

Fig. 6. Bootstrapped MOS switch.

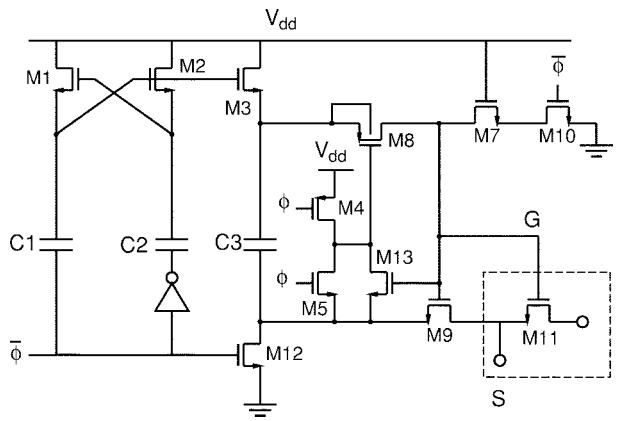

Fig. 7. Bootstrap circuit and switching device.

bootstrap switch was designed to observe device reliability considerations. This switch is conceptually a single NMOS transistor, as shown in Fig. 6.

In the "off" state, the gate is grounded and the device is cutoff. In the "on" state, a constant voltage of $V_{\rm dd}$ is applied across the gate-to-source terminals, and a low on-resistance is established from drain to source independent of the input signal. Although the absolute voltage applied to the gate may exceed $V_{\rm dd}$ for a positive input signal, none of the terminal-to-terminal device voltages exceeds $V_{\rm dd}$.

Fig. 7 shows the actual bootstrap circuit. It operates on a single phase clock ϕ that turns the switch M11 on and off. During the off phase, ϕ is low. Devices M7 and M10 discharge the gate of M11 to ground. At the same time, $V_{\rm dd}$ is applied across capacitor C3 by M3 and M12. This capacitor will act as the battery across the gate and source during the "on" phase. M8 and M9 isolate the switch from C3 while it is charging. When ϕ goes high, M5 pulls down the gate of M8, allowing charge from the battery capacitor C3 to flow onto gate G. This turns on both M9 and M11. M9 enables gate G to track the input voltage S shifted by $V_{\rm dd}$, keeping the gate-source voltage constant regardless of the input signal. For example, if the source S is at $V_{\rm dd}$, then gate G is at $2V_{\rm dd}$; however, $V_{\rm gs} = V_{\rm dd}$. Because the body (n-well) of M8 is tied to its source, latch-up is suppressed.

Two devices are not functionally necessary but improve the circuit reliability. Device M7 reduces the $V_{\rm ds}$ and $V_{\rm gd}$ experienced by device M10 when $\phi = 0$. The channel length of M7 can be increased to further improve its punch-through voltage. Device M13 ensures that $V_{\rm gs8}$ does not exceed $V_{\rm dd}$.

C3 must be sufficiently large to supply charge to the gate of the switching device in addition to all parasitic capacitances in

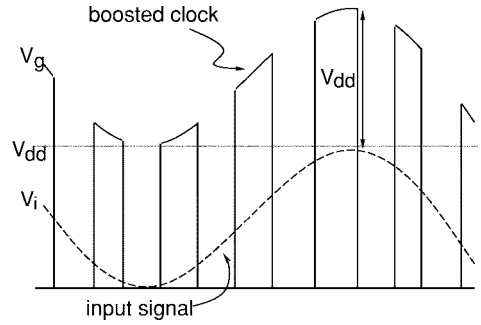

Fig. 8. Conceptual bootstrap circuit output.

the charging path. Otherwise, charge sharing will significantly reduce the boosted voltage according to (12), where C_p is the total parasitic capacitance connected to the top plate of C3 while it is across the main switching device M11

$$V_g = V_s + \frac{\rm C3}{\rm C3 + C_p} V_{\rm dd}. \tag{12}$$

In this design, typical values of C3 were 0.5–1.8 pF, which is approximately six times C_p. These capacitors were implemented with poly over n-diffusion layers with approximately 2 fF/μm^2.

M1, M2, C1, and C2 form a clock multiplier [3] that enables M3 to unidirectionally charge C3 during the off phase. This entire circuit was carefully designed such that no device experiences a relative terminal voltage greater than $V_{\rm dd}$. This circuit is similar to previous low-distortion sampling switch approaches [17]–[21] that provide a constant $V_{\rm gs}$ across the switching device. In this case, however, there is the added constraint of device reliability.

Fig. 8 shows the conceptual output waveforms of the bootstrap circuit. When the switch is on, its gate voltage V_g is greater than the analog input signal V_i by a fixed difference of $V_{\rm dd}$. This ensures that the switch is operated in a manner consistent with the reliability constraints. Because the switch $V_{\rm gs}$ is relatively independent of the signal, rail-to-rail signals can be used, which is important in minimizing power consumption as discussed in Section III. The switch linearity is also improved, and signal-dependent charge injection is reduced. Variations in on-resistance due to body effect, however, cannot be eliminated.

Due to the auxiliary devices, significant parasitic capacitance is introduced at node "S," particularly if there is a large bottom-plate parasitic associated with floating capacitor C3. Therefore, it is best to drive this node with a low-impedance output. Because one bootstrap circuit is required for every switch (that sees a different input voltage), the combined loading of these circuits can present a substantial capacitance to any op-amp driving the switch input node. In the prototype ADC presented, this was one of the factors limiting the reduction in overall power consumption.

This circuit can still be used in the transfer switch of an integrator, which sees a high impedance. If a fully differential integrator is used, the charge sharing between the added

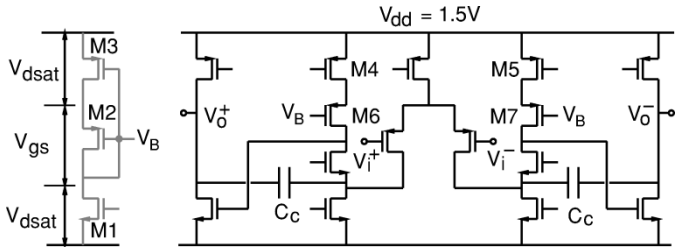

Fig. 9. Bias generator and low-voltage op-amp.

parasitic capacitance and the integrator summing node creates a benign signal-independent, common-mode error. If there is a mismatch in the parasitic capacitances of the two differential halves, a dc offset proportional to the mismatch is added to the integrator. This offset, however, is indistinguishable from an op-amp offset.

One potential transient reliability problem exists for this circuit. If the rise time of the voltage at the gate "G" is too fast, a large voltage could exist across the oxide of the switching device before a channel is formed to equalize the potential between the source and drain. Consider the case where the switching device's source is driven by a low-impedance voltage $V_{\rm dd}$ and the drain is attached to a large sampling capacitor discharged to ground. As the switching device turns on, a voltage of approximately $2V_{\rm dd}$ will be generated on the gate. Before a channel is formed and before the sampling capacitor is charged to $V_{\rm dd}$, an excessive voltage greater than $V_{\rm dd}$ may exist across the gate-to-drain terminals. This effect could create an oxide reliability problem. One solution would be to reduce the rise time by decreasing the W/L of M9 and/or M8. Simulations for this particular ADC prototype showed that even during edge transitions of 1 ns, no relative terminal voltages exceeded $V_{\rm dd}$. It should also be noted that the lifetime of gate oxide is roughly inversely proportional to the voltage-stress duty cycle [22]. Therefore, such transient stress is less harmful than dc stress. A more thorough investigation of these transient effects using a reliability simulator such as the Berkeley reliability tool [23] would be useful.

B. Op-Amp

The op-amp topology used in the pipeline stages is shown in Fig. 9. To achieve an overall linearity of ten bits, the (first-stage) op-amp dc gain must be greater than 60 dB and settle to 0.1% accuracy in less than one-half clock cycle (35 ns). This two-stage, fully differential amplifier consists of a folded-cascode first stage followed by a common-source second stage. The common-source second stage increases the dc gain by an order of magnitude and maximizes the output signal swing for a given voltage supply. As discussed in Section III, this is important in reducing the power consumption. Cascode compensation [10], [11] was used to improve the bandwidth over conventional Miller compensation. A high bandwidth was necessary to achieve fast linear settling. Switched-capacitor common-mode feedback operating on a 50% duty cycle was employed to stabilize the common-mode output voltage. The high-swing switches discussed above were used to connect and disconnect the common-mode sensing capacitors.

To bias the cascode devices, a stack of devices driven by a current source was used as shown on the left side of Fig. 9. The PMOS version is shown here; the NMOS version is similar. This scheme provides a high-swing cascode bias [12], [13]. M3 operates in the triode region, M2 is a diode-connected device operating in the saturation region, and M1 acts as a current source. M3 is sized to create a $V_{\rm ds}$ sufficient to keep M4 and M5 in the saturation region. M2 has the same current density as M6 and M7; therefore, $V_{\rm gs2} = V_{\rm gs6} = V_{\rm gs7}$. Thus, the minimum operating supply voltage is

$$V_{\rm dd} > V_{\rm dsat1} + V_{\rm gs2} + V_{\rm dsat4,5} \tag{13}$$

$$> 3V_{\rm dsat} + V_t. \tag{14}$$

This sets the minimum supply voltage for the op-amp. Due to the limited operating voltage of 1.5 V, several devices were biased at moderate-to-weak inversion.

The sampling and feedback capacitor sizes are determined by kT/C thermal noise constraints. In the first stage, both capacitors were 585 fF. Based on layout extraction the external loading driven by the op-amp is approximately 2.3 pF. Based on HSPICE simulation, the approximate power consumption of the first-stage op-amp was 1.9 mW. Last, although the op-amp dc gain and settling time cannot be directly measured, the measured overall converter performance shows that the op-amp dc gain exceeds 60 dB and the 0.1% settling time is less than 35 ns (at 14.3 MS/s). Due to relaxed accuracy constraints in later pipeline stages, the sampling and feedback capacitors were scaled down to help reduce power consumption [3]. There are a total of eight op-amps in the ADC; the last stage of the pipeline does not need to generate a residue and does not require an op-amp.

C. Comparator

The sub-ADC in each pipeline stage consists of two fully differential comparators, as shown in Fig. 10. In the 1.5-bit-per-stage architecture, the sub-ADC thresholds are $+V_{\rm ref}/4$ and $-V_{\rm ref}/4$, where the ADC input range is $-V_{\rm ref}$ to $+V_{\rm ref}$ differential. The switched-capacitor comparator operates on a two-phase nonoverlapping clock. The differencing network samples $V_{\rm ref}$ during phase ϕ_2 onto capacitor C, while the input at capacitor $3C$ is shorted giving differential zero. During phase ϕ_1, the input signal V_i is applied at the inputs of both capacitors, causing a differential voltage proportional to $V_i - V_{\rm ref}/4$ to appear at the input of the comparator preamp. At the end of phase ϕ_1 ($\overline{\phi_1}$ high), the regenerative flip-flop is latched to make the comparison and produce digital levels at the output V_o. Based on matching and common-mode charge-injection errors, C was chosen to be near minimum size, approximately 40 fF.

The preamp and latching circuit is shown in Fig. 11. Due to digital correction, a comparator error of $V_{\rm ref}/4$ (200 mV) can be tolerated. With such a large allowable offset, a fully dynamic comparator is often used in order to reduce static power consumption [3]. At this low voltage, however, there are significant metastability problems with a fully dynamic

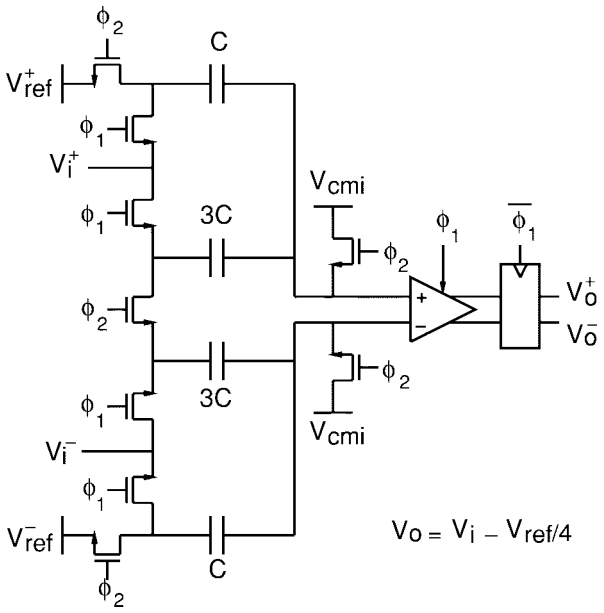

Fig. 10. Differential comparator.

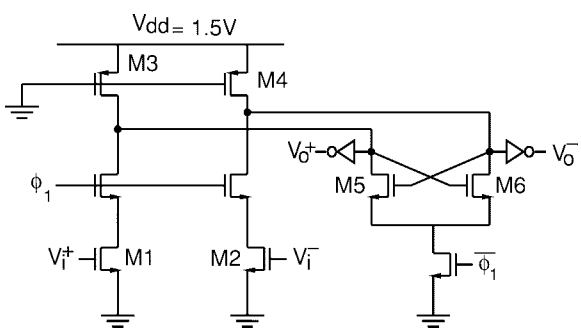

Fig. 11. Comparator preamp and latch.

comparator. Therefore, a class-AB approach was used. During phase ϕ_1, the input $(V_i^+ - V_i^-)$ is amplified by the input transistors, M1 and M2, which are connected to PMOS triode load devices, M3 and M4. During phase $\overline{\phi_1}$, the input is disconnected and the NMOS flip-flop regenerates the voltage difference. Digital inverters buffer the outputs and restore full logic levels.

The comparator latches during the clock nonoverlap period, giving approximately 4 ns to make a decision. The regenerative time constant of the latch was chosen to make the system mean time to metastability on the order of years at 14.3 MS/s. The regeneration time constant is given by (15), where C_T is the total parasitic capacitance at the drain of M5. For the first pipeline stage, the bandwidth of the preamplifier must exceed the bandwidth of the input signal being digitized, which is 7.15 MHz for the prototype. The static power consumption of the preamplifier is approximately 200 μW based on HSPICE simulation. There are a total of 18 comparators in the ADC (two per stage)

$$\tau \propto \frac{C_T}{g_{m5}}. \tag{15}$$

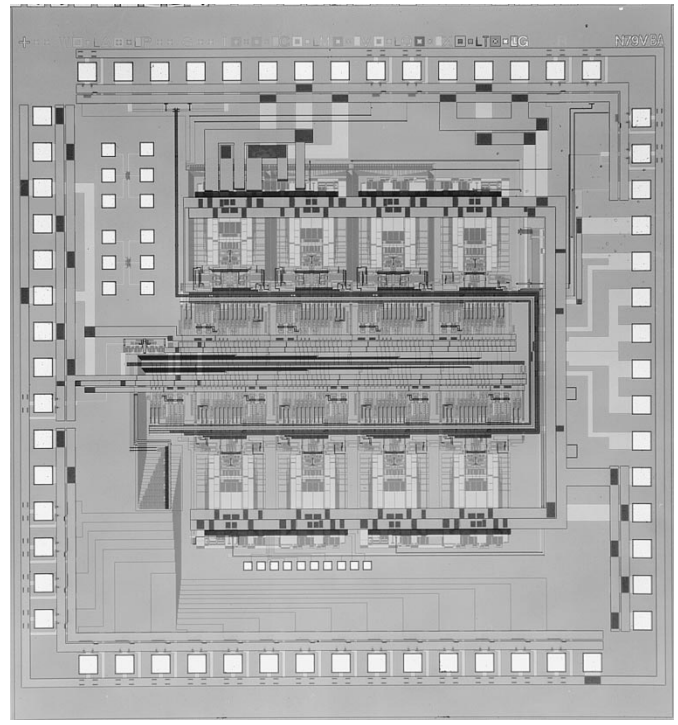

Fig. 12. Die photo of prototype.

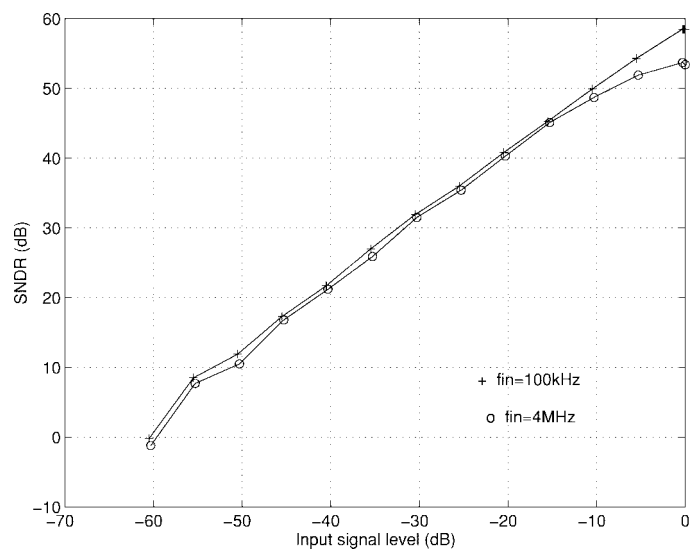

Fig. 13. Output SNDR versus input signal level.

V. Measured Results

An experimental prototype of the ADC was fabricated in a 0.6-μm, single-poly, triple-metal CMOS technology with threshold voltages $V_{\rm tn} = 0.7$ V, $V_{\rm tp} = 0.9$ V, and a poly/n+ linear capacitor option. The die area not including the pad ring is 2.3 $\times$ 2.5 mm^2. Fig. 12 shows the die photo. The input signal enters the chip from the upper left corner and is processed by a cascade of nine pipeline stages. The eight op-amps are visible in two rows of four.

The dynamic linearity of the ADC was measured by analyzing a fast Fourier transform of the output codes for a single input tone. The peak signal-to-noise-and-distortion

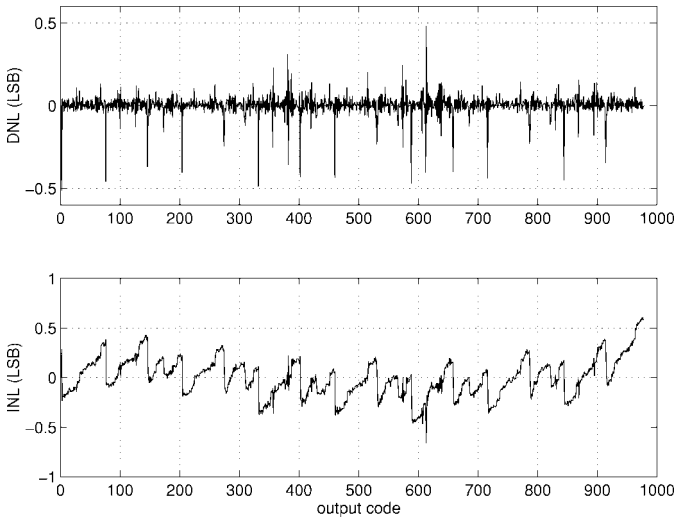

Fig. 14. DNL and INL versus output code.

TABLE I
MEASURED A/D PERFORMANCE AT 25°C

V_{dd}	1.5 V
Technology	0.6-μm CMOS $V_{tn} = 0.7$ V, $V_{tp} = 0.9$ V
Resolution	10 bits
Conversion rate	14.3 MS/s
Active area	2.3 × 2.5 mm^2
Input range	±800 mV differential
Power dissipation	36 mW (w/o pad drivers)
DNL INL	0.5 LSB 0.7 LSB
SNDR	58.5 dB ($f_{in} = 100$ kHz)

ratio (SNDR) for a 100-kHz sinewave input was measured at 58.5 dB with a clock frequency of 14.3 MHz. For a 4-MHz sinewave input, the peak SNDR was 53.7 dB. Fig. 13 shows the SNDR versus input level at a clock frequency of 14.3 MHz.

The static linearity of the ADC was measured using a low-frequency (100-kHz) tone and analyzing over 10^6 output codes. The maximum differential nonlinearity was measured at 0.5 least significant bit (LSB), and the maximum integral nonlinearity using a least squares fit was measured at 0.7 LSB. Fig. 14 shows the differential nonlinearity (DNL) and integral nonlinearity (INL) versus output code. The power consumption at a clock frequency of 14.3 MHz was 36 mW from a 1.5-V supply. Table I summarizes the measured results.

VI. CONCLUSION

The trend toward lower voltage supplies is driven by reliability considerations as device geometries become increasingly smaller. Therefore, an emphasis was placed on reliable, low-voltage design. The bootstrapped MOS switch achieves rail-to-rail signal swing at low voltage without requiring low-threshold devices. Furthermore, this was achieved without overstressing any MOS devices. This 1.5-V, 10-bit, 14.3-MS/s, 36-mW pipeline ADC implemented in a 0.6-μm CMOS technology demonstrates that video-rate analog signal processing can be achieved at low voltage without requiring special enhancements to CMOS technology.

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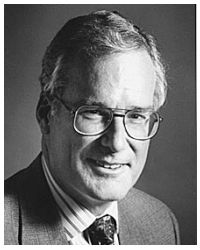
Andrew M. Abo received the B.S. degree in electrical engineering from the California Institute of Technology, Pasadena, in 1992. He currently is pursuing the Ph.D. degree in electrical engineering at the University of California, Berkeley.

His research interests include low-voltage design of switched-capacitor circuits for reliability and analog-to-digital conversion.



Paul R. Gray (M'69–SM'76–F'80) was born in Jonesboro, AK, on December 8, 1942. He received the B.S., M.S., and Ph.D. degrees from the University of Arizona, Tucson, in 1963, 1965, and 1969, respectively.

In 1969, he joined the Research and Development Laboratory, Fairchild Semiconductor, Palo Alto, CA, where he was involved in the application of new technologies for analog integrated circuits, including power-integrated circuits and data-conversion circuits. In 1971, he joined the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, as a Professor. His research interests during this period have included bipolar and MOS circuit design, electrothermal interactions in integrated circuits, device modeling, telecommunications circuits, and analog–digital interfaces in VLSI systems. He is the coauthor (with R. G. Meyer) of *Analysis and Design of Analog Integrated Circuits* (New York: Wiley, 1993), a widely used college textbook. During yearlong industrial leaves of absence from Berkeley, he was Project Manager for Telecommunications Filters with Intel Corp., Santa Clara, CA (1977–1978) and Director of CMOS Design Engineering with Microlinear Corp., San Jose, CA (1984–1985). At Berkeley he has held several administrative posts, including Director of the Electronics Research Laboratory (1985–1986), Vice-Chairman of the Electrical Engineering and Computer Sciences (EECS) Department for Computer Resources (1988–1990), and Chairman of the Department of EECS (1990–1993). He currently is Dean of the College of Engineering and is the Roy W. Carlson Professor of Engineering.

Prof. Gray is a member of the National Academy of Engineering. He was a corecipient of best paper awards at the International Solid State Circuits Conference and European Solid-State Circuits Conference. He was a corecipient of the IEEE R. W. G. Baker Prize in 1980, the IEEE Morris K. Liebman Award in 1983, and the IEEE Circuits and Systems Society Achievement Award in 1987. In 1994, he received the IEEE Solid-State Circuits Award. He was Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 1977 through 1979. He was Program Chairman of the 1982 International Solid State Circuits Conference. He was President of the IEEE Solid-State Circuits Council from 1988 to 1990.