

A Reconfigurable Low Power FPGA Design with Autonomous Power Gating and LEDR Encoding

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ABSTRACT: In this project, design of an asynchronous FPGA blocks is implemented with power optimization techniques. Concentrated on STANDBY and DYNAMIC power consumptions are presented and studied on various gating techniques. Standby power is reduced by using autonomous fine grain power gating and reducing the dynamic power by using the level encoding dual rail (LEDR) architecture. The proposed autonomous fine grain power gating method each lookup table has its own sleep transistor and related sleep controller. So when any lookup tables are inactive, they can be set to sleep mode immediately. LEDR encoding is used to data flow at input and output of FPGAs, it reduces the dynamic power.

KEYWORDS: STANDBY power, DYNAMIC power, level encoding dual rail (LEDR), fine grain power gating, sleep transistor, look up Table, FPGA, Asynchronous

INTRODUCTION:

Due to the dramatic increase in portable and battery-operated applications, lower power consumption has become a necessity in order to prolong the battery life. Power consumption is an important part of the equation determining the end product's size, weight, and efficiency. Field programmable gate array (FPGA)s are becoming more attractive for these applications due to their shorter product life cycle. FPGAs are programmable, so they allow product differentiation. Selecting an appropriate FPGA architecture is critical in achieving the best static and dynamic power consumption. Flash-based FPGAs by Micro semi are the low-power leaders in the industry. In addition to utilizing the low-power attributes of flash-based FPGAs, you can deploy several design techniques to further reduce overall power. The important FPGA power components to consider in the following sections:

- Power-up (inrush power): Inrush power is the amount of power drawn by the device during power-up.
- Configuration power: Configuration power is the amount of power required during the loading of the FPGA upon power-up (specific to SRAM-based programmable logic devices).
- Static (standby) power: Static power is the amount of power the device consumes when it is powered-up but not actively performing any operation. Dynamic (active) power: Dynamic power is the amount of power the device consumes when it is actively operating.
- Sleep power (low-power mode): Some FPGA devices offer low-power or sleep modes. In some cases, this may be different from static power. This application note focuses on reducing the dynamic power. In general, the dynamic power is calculated using the formula shown in EQ 1: $P_{dynamic} = C \cdot V^2 \cdot F$ Where D is the switching activity, C is the capacitive load, V is the supply voltage, and F is the frequency. In flash FPGAs, the components that consume dynamic power are clock networks, logic blocks, routing resources (nets), I/Os, memory, PLLs, etc. These components have different D , C , V , and F values. For example, the dynamic power of a net

depends on the average switching (D), the total capacitive loading of the net (C), the net's voltage swing (V), and the frequency (F). In FPGA design, the clock gating and power gating is important work. To implement clock gating, circulation is employed. The idea of circulation is to retain the contents of the flip-flop in the sleep state. Circulation can reduce the dynamic power consumption of registers and the gates in the fan-out of the registers. However, the standby power consumption of the clock network cannot be reduced. The standby power is a serious problem because it has an enormously large number of transistors to achieve its programmability. Low-cost FPGAs consume up to hundreds of milliwatts power. Power gating has emerged as the most effective design technique to achieve low standby power. Power gating techniques are based on selectively setting the functional units into a low leakage mode when they are inactive.

FPGA (Field Programmable Gate Array):

Field Programmable Gate Arrays are two dimensional array of logic blocks and flip-flops with a electrically programmable interconnections between logic blocks. The interconnections consist of electrically

programmable switches which is why FPGA differs from Custom ICs, as Custom IC is programmed using integrated circuit fabrication technology to form metal interconnections between logic blocks.

In an FPGA logic blocks are implemented using multiple level low fanin gates, which gives it a more compact design compared to an implementation with two-level AND-OR logic. FPGA provides its user a way to configure:

1. The intersection between the logic blocks and
2. The function of each logic block.

Logic block of an FPGA can be configured in such a way that it can provide functionality as simple as that of transistor or as complex as that of a microprocessor. It can be used to implement different combinations of combinational and sequential logic functions. Logic blocks of an FPGA can be implemented by any of the following:

1. Transistor pairs
2. combinational gates like basic NAND gates or XOR gates
3. n-input Lookup tables
4. Multiplexers
5. Wide fan-in And-OR structure.

Routing in FPGAs consists of wire segments of varying lengths which can be interconnected via electrically programmable switches. Density of logic block used in an FPGA depends on length and number of wire segments used for routing. Number of segments used for interconnection typically is a tradeoff between density of logic blocks used and amount of area used up for routing.

The ability to reconfigure functionality to be implemented on a chip gives a unique advantage to designer who designs his system on an FPGA. It reduces the time to market and significantly reduces the cost of production.

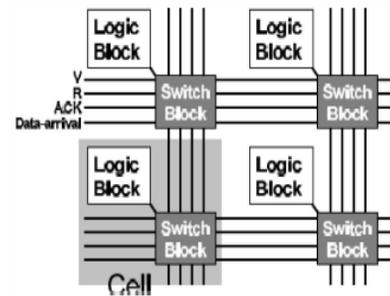


Fig1: FPGA architecture

Asynchronous Architecture

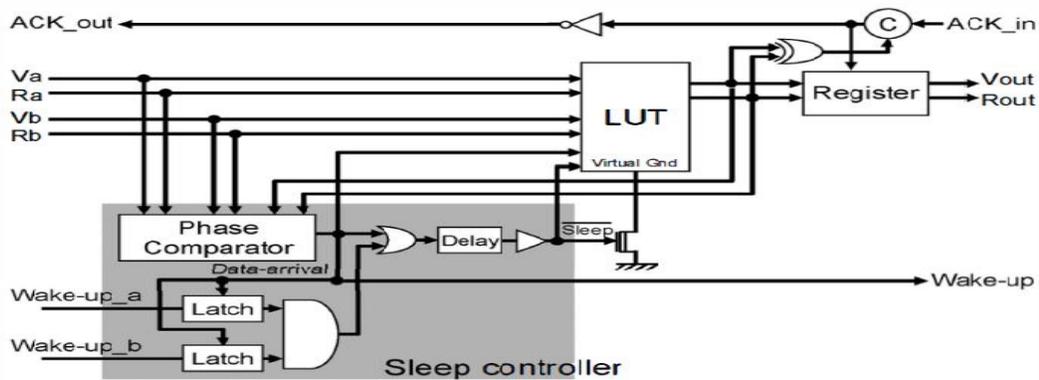
Design: The asynchronous architecture it detects the activity of a power gated domain. The activities are:

- 1) To determine when logic block is standby state, when sleep state & when active state.

2) It compares the phase of the input data and output data

3) It determines the function of lookup table. Dynamic power reducing purpose introduce dual rail encoding (existing)[2] and level encoding dual rail (proposed) architecture. Standby power reducing purpose introduced autonomous fine grain power gating technique. The registers store the data value and produce the output to switch block. Sleep controller monitor wake up the successive block when it gets data. The switch block consists of pass transistor switches. In a switch block, a wire-set consists of four wires: two for data lines (Vout and Rout),

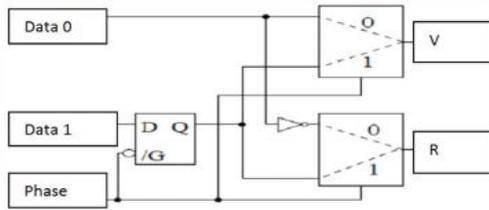
one for the acknowledge signal and one for the wake-up signal. A pass-switch block consists of four pass switches and a single memory bit. This FPGA architecture logic block can be connected to the switch block. In the switch block there are four signals 1) data signal (first bit) 2) data signal (second bit) 3) acknowledgement signal 4) data arrival signal. The above four signal acknowledgement signal and data arrival signal connected to pervious logic block. The two pass switches are used for the four wires of the wire-set, one Va, Ra, ack and wakeup signal wires respectively. The pass switches are controlled by the same memory bits.



The circuit can be implemented by using below the architectures. The logic block can be connected to the switch block. Each switch block connected to the other switch block. This logic block and switch block described below the architecture diagrams.

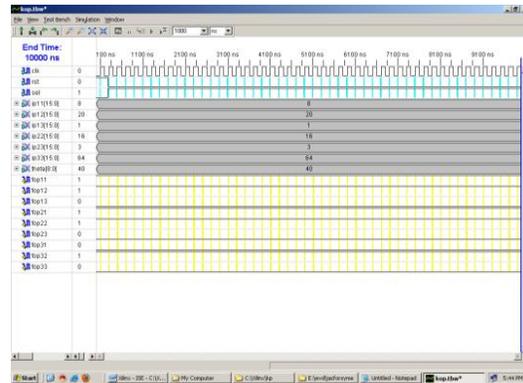
No need to include external clocks or oscillations.

AUTONOMOUS FINE GRAIN POWER GATING:



This architecture operation based on data's and phase signal. The D latch signal given to selectors and selectors produce the output of level encoding signal. In LEDR encoding, no spacer is required. Table 1 shows the code table of LEDR encoding. In LEDR encoding, each data value has two types of code words with different phases. Above example shows the data values "0," "0," and " 1" are transferred. The main feature is that the sender sends data values alternately in phase $^{\circ}$ and phase 1. Because no spacer is required, the number of signal transitions is half of four-phase dual-rail encoding. As a result, the throughput is high and the power consumption is small. Based on this observation, in the proposed FPGA, LEDR encoding is employed for implementing the asynchronous architecture to reduce the dynamic power.

RESULTS:



CONCLUSION:

In this paper, we presented a low-power asynchronous FPGA architecture which adopts several novel techniques to reduce power consumption. Design of Level encoding Dual Rail technique can effectively eliminate the excessive data transition without increasing loading on the global clock signal. The implementation of the autonomous fine-grain power gating has been done efficiently using the standby state to wake up the Logic block before the data arrives and power OFF the Logic block only when the data does not come for quite a while.

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