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# Improved SNM 10T-SRAM Cell Using ST Inverter

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***Abstract* —The reliability of memory is becoming the serious concern in the present technology with increased effect of PVT variation. In this paper we propose a novel Schmitt Trigger (ST) based fully differential10 transistors Static Random Access Memory (SRAM) cell to curb the effect of process variation and improve SNM (Static Noise Margin). This robust Schmitt trigger based memory cell unveils built in process variation tolerance and provide better read SNM, write margin. It utilizes fully differential operation and hence does not require any architectural changes from the present 6T architecture. The result of the proposed cell shows 150% improvement in read SNM compared to 6T SRAM cell.**

***Keyword*—SRAM, SNM, RSNM, ST (Schmitt Trigger), Write Margin**

## I. INTRODUCTION

Static random-access memory (SRAM) is the most common embedded-memory option for CMOS ICs. SRAM continues to be a critical component across a wide range of microelectronics applications from consumer wireless to high-end workstation and microprocessor applications. For almost all fields of applications, semiconductor memory has been a key enabling technology. It is forecasted that embedded memory in SoC designs will cover up to 90% of the total chip area. A representative example is the use of cache memory in microprocessors. The operational speed could be significantly improved by the application of on-chip cache memory that temporarily stored a fraction of the data and instruction content of the main memory.

Among embedded memories, six-transistor (6T)-based static random access memory (SRAM) continues to play a pivotal role in nearly all VLSI systems due to its superior speed and full compatibility with logic process technology. But as the technology scaling continues, SRAM design is facing severe challenge in maintaining sufficient cell stability margin under relentless area scaling. Meanwhile, rapid expansion in mobile application, including new emerging application in sensor and medical devices, requires far more aggressive voltage scaling to meet very stringent power constraint. Many innovative circuit topologies and techniques have been extensively explored and proposed in recent years.

With the silicon technology entering the sub- 65-nm regime, transistors no longer act deterministically.

Fluctuation in device dimensions due to manufacturing process (sub-wavelength lithography, chemical mechanical polishing, etc.) is a serious issue in nanometer technologies. Until approximately 0.35 µm technology node, process variation was inconsequential for the IC industry. Circuits were mostly immune to minute variations because the variations were negligible compared to the nominal device sizes. However, with the growing disparity between feature size and optical wavelengths of lithographic processes at scaled dimensions (below 90 nm), the issue of parameter variation is becoming severe.

The effects of variability in nanometer-scale integrated circuits cause significant deviations from the prescribed specifications for a chip. The magnitude of these deviations, together with tight performance specifications, implies that variability is an increasingly vexing problem as technologies continue to scale.

The sources of these variations can be categorized into several classes, depending on their origin:

*Process variations:* Theseare one-time variations that occur when a circuit is manufactured, and cause process parameters to drift from their designed values.

*Environmental variations:* are run-time variations that reflect the effects of altered operating conditions during the operation of a circuit. Such variations may be attributed to factors such as supply voltage changes, thermal effects, and radiation-induced soft errors.

*Aging variations:* reflect the fact that the behavior of a circuit degrades as it ages, due to the prolonged application of stress. Such degradations may result in parametric degradations or catastrophic failures.

These variations can impact key circuit performance characteristics: for digital circuits, the affected parameters include the delay, power, and lifetime of the circuit, while for analog circuits, the performance parameters to be monitored are specific to the type of circuit.

## II. LITERATURE REVIEW

Several SRAM bit cells have been proposed having different design goals such as bit density, bitcell area, low voltage operation and architectural timing specifications. Fig. 1 shows the four–transistor (4T) load less bitcell, PMOS devices act as access transistors [2].

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The design necessity is such that pMOS OFF state current should be more than the pull-down nMOS transistor leakage current for maintaining data "1" reliably.

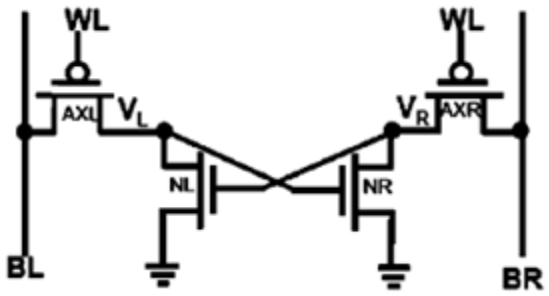


**Fig.1: 4T SRAM Cell**

With increasing process variations and exponential dependence of the subthreshold current on the threshold voltage, satisfying this design requirement across different process, voltage, and temperature (PVT) conditions may be challenging. In fig.2 shows 5T bitcell consists of asymmetric cross coupled inverters with a single bitline[7]. Separate bitline pre charge voltages are used for read and write operations. The intermediate read Bitline pre charge voltage requires a dc–dc converter. Tracking the read pre charge voltage across PVT corners would require Additional design margins in bit cell sizing and may limit its applicability.

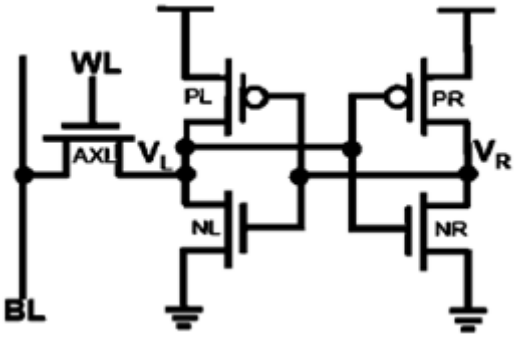


**Fig.2: Single ended 5T bit Cell**

A 6T bitcell comprises of two cross-coupled CMOS Inverters, the contents of which can be accessed by two nMOS access transistors as shown in the fig.3. The 6T bitcell is used in the present SRAM designs. Write-ability is achieved by modulating the virtual-VCC and virtual-VSS of one of the inverters.

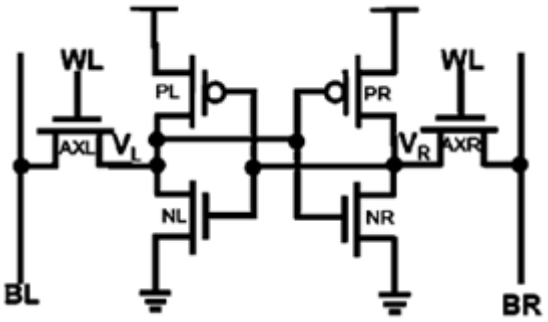


**Fig.3: 6T SRAM Cell**

Fig.4 shows the single-ended 7T bit cell proposed separately by Tawfik *et al.* and Suzuki consists of single-ended write operation and a separate read port [3], [4]. Single-ended write operation in this 7T bit cell needs either asymmetrical inverter characteristics or differential VSS/VCC bias.

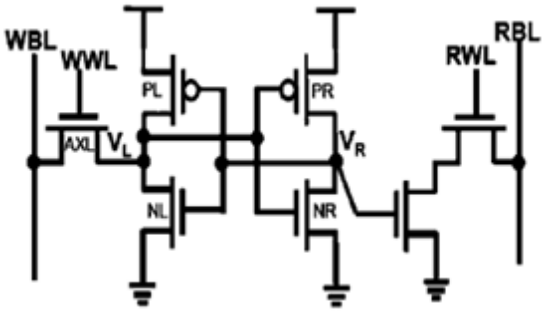


**Fig.4: Single ended 7T bit cell [Tawfic, Suzuki]**

In a single-ended 8T bit cell, extra transistors are added to the conventional 6T bit cell to separate read and write operation as shown in fig.5 [5]–[6]

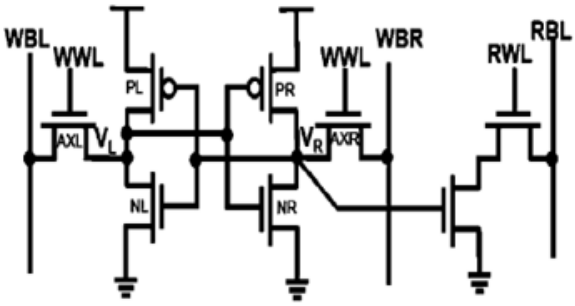


**Fig.5: Single ended 8T bit cell**

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## III. SCHMITT TRIGGER BASED SRAM

The conflicting read versus write design requirements in the conventional 6T bitcell, was the bottleneck of the design, to overcome this we apply the Schmitt Trigger (ST) principle for the cross-coupled inverter pair.

### *3.1 Schmitt Trigger Principles:*

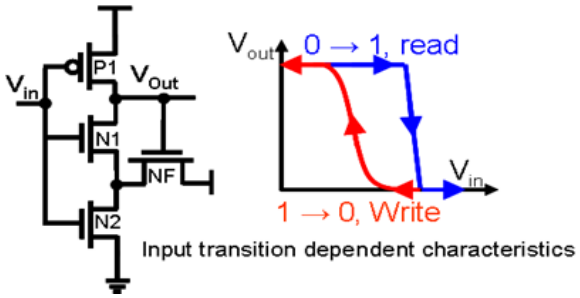


**Fig.6: ST inverter**

A Schmitt trigger increases or decreases the switching threshold of an inverter depending on the direction of the input transition as shown in the fig. The feedback mechanism is use in the pull down path only. During 0 → 1 input transition feedback (NF) transistor tries to preserve the logic 1 at the output by raising the source voltage of transistor N1.this gives the higher threshold voltage of inverter and gives very sharp transfer characteristic. For robust read operation. For 1 → 0 input transition the feedback is off and gives the smoother transfer characteristic for easy write operation.

### *3.2 ST-SRAM Cell:*

The proposed ST 10-transistor SRAM cell focuses on makingthe basic inverter pair of the memory cell robust. The cross-coupled inverter pair stability is of concern. To improve the inverter characteristics, Schmitt trigger configuration is used. A Schmitt trigger increases or decreases the switching threshold of an inverter depending on the directionof the input transition [5]. This adaptation is achieved with the help of afeedback mechanism.fig. shows the schematic of Schmitt trigger(ST) bit cell Transistors PL-NL1-NL2-NFL form one ST inverterwhile PR-NR1-NR2-NFR form another ST inverter. AXLand AXR are the access transistors. The positive feedback fromNFL/NFR adaptively changes the switching threshold of the inverterdepending on the direction of input transition.

During aread operation (with say and ), due to voltagedivider action between the access transistor and the pull-downNMOS, the voltage of node rises. If this voltage is higherthan the switching threshold (trip point) of the other inverter, the contents of the cell can be flipped, resulting in a read failureevent [1]. In order to avoid a read failure, the feedback mechanismshould increase the switching threshold of the inverterPR-NR1-NR2. Transistors NFR and NR2 raise the voltage atnode and increase the switching threshold of the inverterstoring "1". Thus, Schmitt trigger action is used to preserve thelogic "1" state of the memory cell. The proposed ST bitcell utilizesdifferential operation, giving better noise immunity [5]. Itrequires no architectural change compared to the conventional 6T cell architecture and hence can be used as a drop-in replacementfor the present 6T based designs

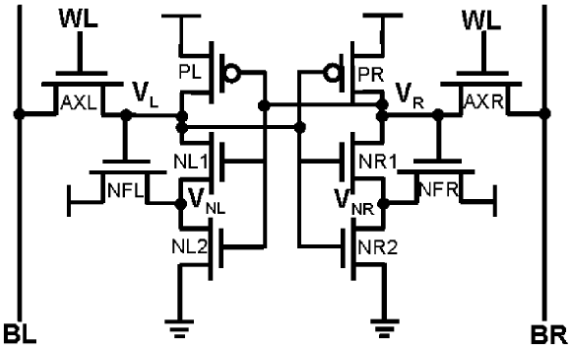


**Fig.7 ST-SRAM**

## IV. EXPERIMENTAL ENVIRONMENT & SIMULATION RESULTS

Tanner 14.1 tool is used to draw schematic and to simulate the proposed design. Schematic of the proposed cell is first designed on tanner's schematic editor and netlist of the cell is than taken out. This netlist runs with 45 nm Predictive Technology Model (PTM) file on tanner's spice simulator to get simulation results. From the result, SNM and RNM are calculated as shown in fig. 1. Similar process is used to calculate the result for the 6T SRAM cell. Simulation result shows that there is2.5x improvements in RSNM and 1.2x improvement in SNM.

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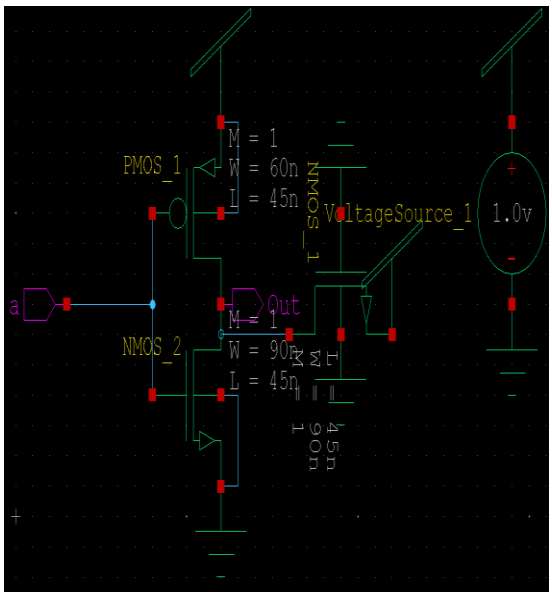
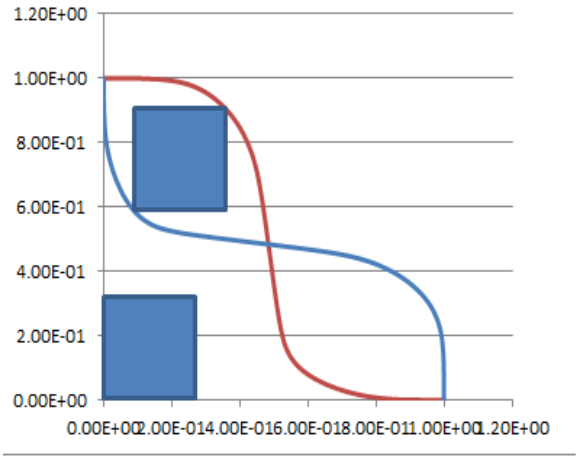
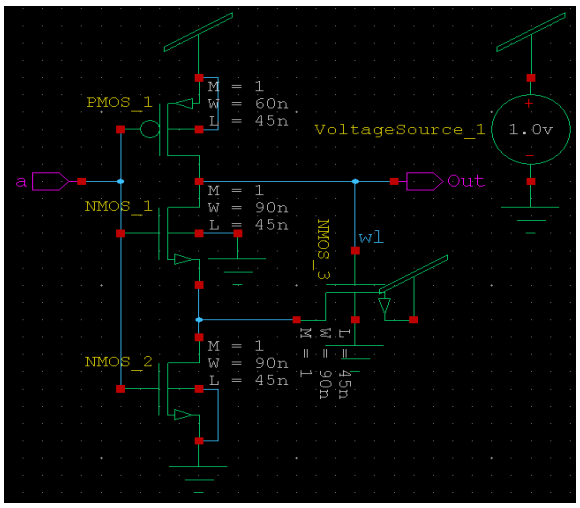


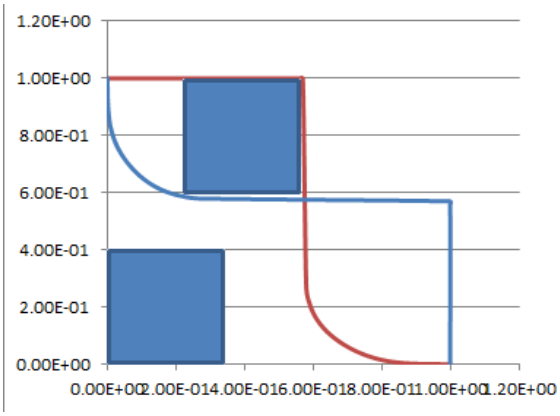

Half 6T-SRAM cell



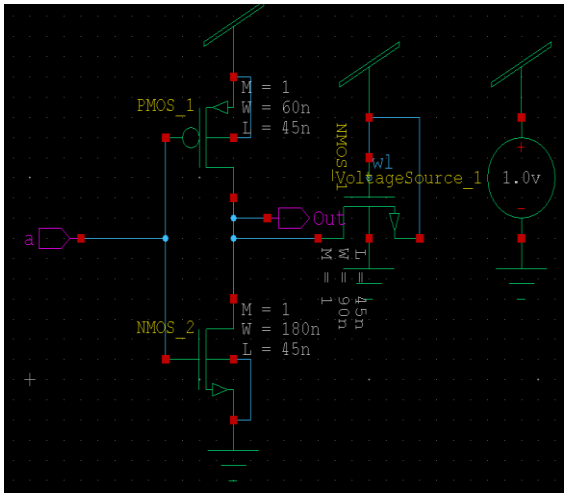

Butterfly graph for SNM 6T cell




Half ST-SRAM Cell




Butterflygraph forSNM ST cell




Half 6T-SRAM cell

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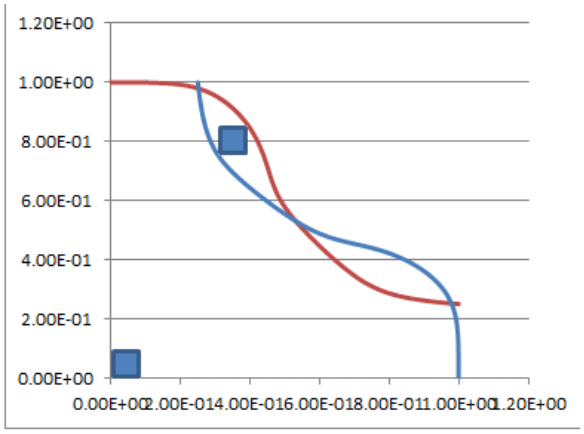
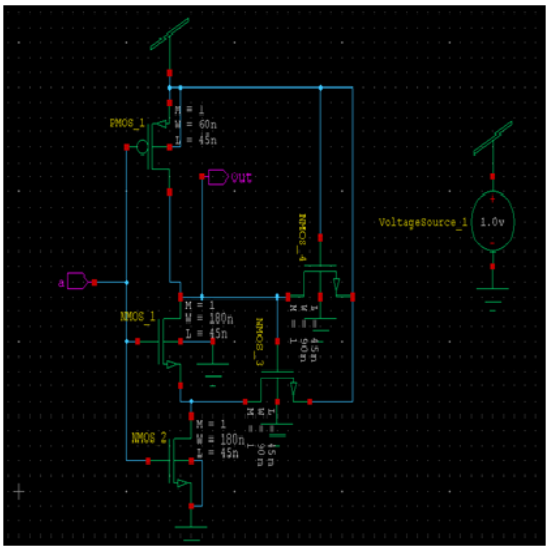
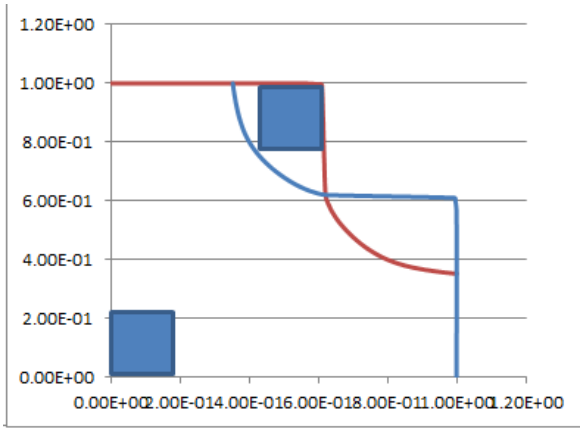



**Butterfly graph forRead SNM 6T cell**




**Half ST-SRAM Cell**




**Butterfly graph forRead SNM ST cell**

## V. CONCLUSION

Ultra-low voltage SRAM cell in sub-nanometer technology degrade the yield. The contradiction in RSNM and WSNM in 6T SRAM cell is overcome by the proposed STSRAM cell. The built-in feedback mechanism of the STSRAM cell weakens the effect of process variation and increasing the yield. Simulation result shows the effectiveness of the STSRAM cell over 6T SRAM cell.

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