Analysis and Simulation of Sub-threshold Leakage Current in P3 SRAM Cell at DSM Technology for Multimedia Applications

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Abstract — **In this work, the analysis and simulation work is proposed for the low-power (reduced subthreshold leakage) and high performance SRAM bit-cells for mobile multimedia applications in deep-sub-micron (DSM) CMOS technology. The sub-threshold leakage analysis of the P3 SRAM cell has been carried out. It has been observed that due to pMOS stacking and full supply body-biasing, there is a reduction of 70% and 86% in sub-threshold leakage current at V_{DD}=0.8V and V_{DD}=0.7V respectively as compared to conventional 6T SRAM cell. Due to this a reduction in the standby power has been achieved w.r.t the 6T and PP SRAM design at a bearable expense of the SVNM and the WTV.**

***Index Terms*—Sub-threshold Leakage, Standby Power, Stacking, Conventional SRAM cell, PP-SRAM, P3-SRAM**

I. Introduction

Today's portable devices have become computationally intensive devices as the user interface has migrated to a fully multi media experience. This migration leads to the growing demand of battery powered portable multimedia applications. According to the International Technology Roadmap (ITRS), 90% of the chip area will be occupied by the memory core by 2014 [1]. So, SRAM plays a critical role in the overall power, performance, stability and area requirements. In order to fulfill the demands, they must be specifically designed for every application. Devices such as cell phones, have low activity factor, i.e. their idle time is more than active time of device. Even at the idle time, the device battery service is affected by the leakage power loss. But with the scaling down of technology, SRAM bit-cell structures are facing serious challenge in maintaining performance because of leakage current issues, both in dynamic and standby modes. In standby mode of SRAM bit-cell, there are several sources for leakage current, e.g., the sub-threshold current due to low threshold voltage, while in dynamic mode, the gate leakage current due to very thin gate oxides, is the major contributor [2]. Process variation and leakage currents of transistors become more critical with the scaling down of technology, which is further affected by supply voltage variations and/or temperature [3]. The SRAM stability is further severely affected by supply voltage scaling. The SRAM leakage current has become a more significant component of total chip current as a large portion of the total chip transistors directly comes from on-die SRAM. Since the activity factor of a large on-die SRAM is relatively low. So, it is demanded to pay more attention towards reducing standby leakage currents. In this work, the subthreshold leakage current has been simulated and analyzed in the 6T, PP, and P3 SRAM cells in the standby mode of operation. Further, the stability has been analyzed.

The paper is organized as follows. In section II a brief functional view of conventional 6T SRAM bit-cell is presented. Basic leakage current mechanisms are presented in section III. The section IV reviews the PP and the P3 SRAM designs followed by the analysis of the three cells and conclusion in section V and VI respectively.

II. Conventional 6T SRAM Bit-Cell

The conventional SRAM (CV-SRAM) cell has six MOS transistors (Four-nMOS and Two-pMOS), Fig 1. The memory bit-cell has two CMOS inverters connected back to back (M1, M3, and M2, M4). Two more pass transistors (M5 and M6) are the access transistors controlled by the Word Line (WL). The cell preserves its one of two possible states "0" or "1", as long as power is available to the bit-cell.

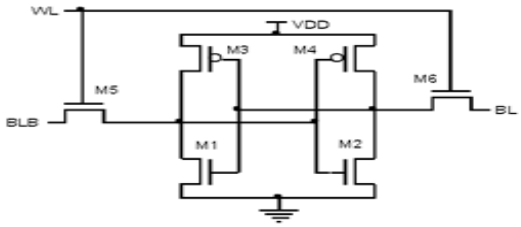

Figure1. 6T-CMOS SRAM Cell [4].

Here, Static power dissipation is very small. Thus the cell draws current from the power supply only during switching. But idle mode of the memory is becoming the main concern in the Deep Sub-Micron (DSM) technology due to its concerns in the leakage power and data retention at lower operating voltages. There are mainly the following three states of SRAM memory cell [5], the Write, Read, and Hold states.

III. Leakage Current Mechanisms

High leakage current in deep-submicron regimes is the major contributor of power dissipation of CMOS circuits as the device is being scaled. Various leakage mechanisms are

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show in Fig. 2, the dominant ones are the gate leakage, sub-threshold leakage, and reverse junction leakage current.

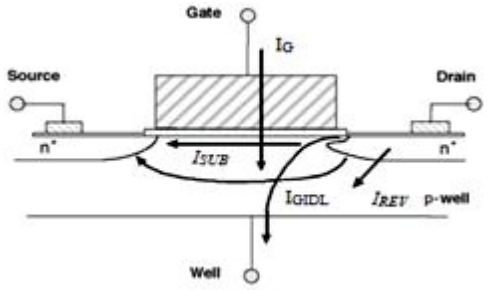

Figure2. Leakage current mechanisms of deep-submicron transistors.

SUB-THRESHOLD LEAKAGE (I_{SUB})

Current is the drain-to-source leakage current when the transistor is in the OFF mode. This happens when the applied voltage V_{GS} is less than the threshold voltage V_t of the transistor, i.e., weak inversion mode. Subthreshold current flows due to the diffusion current of the minority carriers in the channel of Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Equation (1) relates sub-threshold power with other device parameters.

$$P_{SubVf} = \frac{\mu W_{eff}}{L_{eff}} C_{ox} V_T^2 e^{(V_{GS}-V_{th})/nV_T} . (1 - e^{-V_{DS}/V_T}) \quad (1)$$

Where, $P_{Sub\text{-}Vf}$ is the Sub-threshold Power, m is Mobility, W_{eff} is the channel effective width, L_{eff} is the channel effective length, C_{ox} is the Oxide capacitance, $V_T = \frac{KT}{q}$ is the Thermal voltage, V_{GS} is the Gate-Source Voltage, V_{DS} is Drain-Source Voltage, K is Boltzmann's Constant, T is Temperature and q is the Charge.

As the supply voltage (V_{DD}) is being uniformly scaled down with successive technology nodes. The transistor delay is inversely proportional to the difference of supply and threshold voltage [6], the threshold voltage must also be scaled down proportionally with each technology node to maintain the circuit performance. This leads to an exponential increase in sub-threshold leakage current. Also, increasing the threshold voltage (V_T) of the transistor is an effective way to reduce sub-threshold leakage.As, the contribution of the sub-threshold leakage current is most dominant we thus analyze various SRAM cells for the Sub-threshold leakage in standby mode.

IV. A REVIEW TO RELATED WORK

In this section, we review some of the previously proposed SRAM cell structures. In [4], a P3 SRAM bit-cell structure at 45nm technology has been proposed for semiconductor memories with high activity factor based applications in Deep-Sub-Micron (DSM) CMOS technology. It has been proposed for the reduction of the active and the standby leakage power through the gate and sub-threshold leakage reduction in the active and standby mode of the memory operation.The *stacking transistor* pMOS (PM4), connected in series (in line), is kept OFF in standby mode and kept ON in active (read/write) mode.The pMOS transistors are used to lower the gate leakage current [7] while full-supply body-biasing scheme is used to reduce the sub-threshold leakage currents. P3 SRAM bit-cell made a significant fall in dynamic as well as standby powers in comparison to the conventional 6T SRAM bit cell, at the cost of small area penalty and issues with SNM.

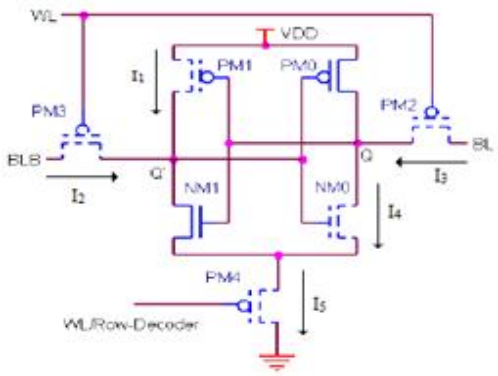

Figure3. P3 SRAM Sub-threshold Current Paths in Standby mode.

In [7], a gate leakage current reduction technique based on the pMOS pass-transistor SRAM bit-cell structure as PP-SRAM cell has been proposed at 45nm technology and 0.8V supply voltage. In this cell, in order to decrease the gate leakage currents of the SRAM bit cell, nMOS pass transistors are replaced by pMOS pass transistors. The use of pMOS leads to performance degradation due to different mobility coefficients for the nMOS and pMOS transistors. To overcome this problem, the width of pMOS pass transistor is selected as 1.8 times of that of the nMOS for technology used in this work. Thus, has area penalty.

V. LEAKAGE CURRENT ANALYSIS IN P3-SRAM BIT-CELL

To analyze the leakage currents and standby power in the P3, PP and 6T SRAM Cells, the simulation work is being performed in Cadence Virtuoso Environment at 45nm technology with oxide thickness of 2.4nm at 27°C and the supply voltage of V_{DD}=0.8V and 0.7V.

A. SUB-THRESHOLD LEAKAGE (I_{SUB})

Fig. 4 and fig. 5 shows the comparison of sub-threshold leakage current in the standby mode for 6T SRAM, PP SRAM and the P3 SRAM cell.

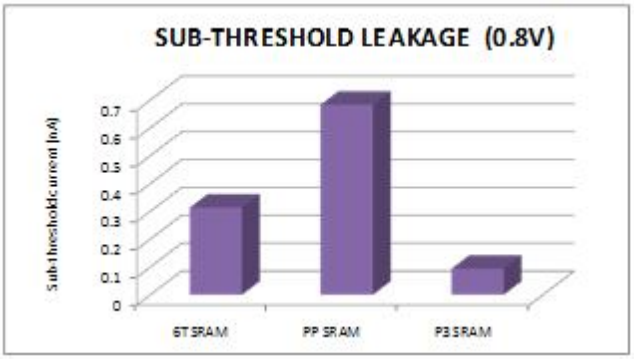

Figure 4. Sub-threshold Leakage Comparison at 0.8V

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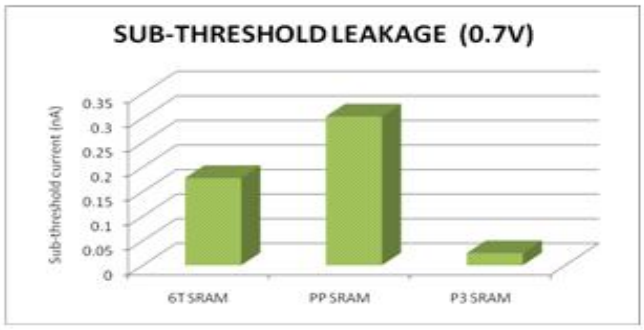

Figure 5. Sub-threshold Leakage Comparison at 0.8V

As the Gated-pMOS (PM4) is turned OFF (i.e. in hold state), it opposes the leakage current flow through it as there is no direct path between V_{DD} and ground, thus a decrease in the leakage current of 70% and 86% has been observed at V_{DD}=0.8V and 0.7V respectively with respect to 6T SRAM bit-cell. While compared to PP SRAM, the sub-threshold leakage reduction is 86.3% at V_{DD}=0.8V and 91.8% at V_{DD}=0.7V due to the stacking effect.

B. Standby power

Fig. 6, shows the total standby power consumption of all the three designs. It is clear that due to the lowering of the sub-threshold current in the P3 SRAM, the reduction in total standby power of up to 86% and 89% has been achieved with respect to conventional 6T and PP SRAM respectively.

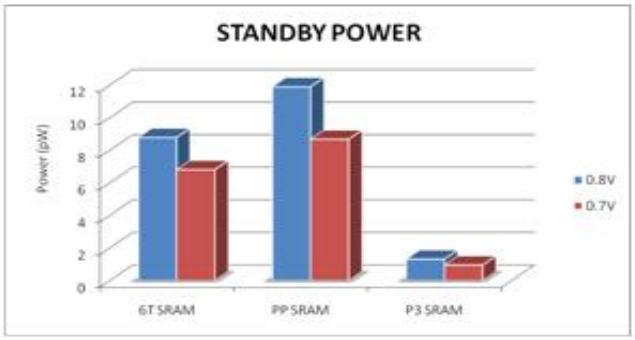

Figure 6. Standby Power Comparison

C. Stability

1. Static Voltage Noise Margin (SVNM)

Fig. 7, shows the SVNM comparison of all the three designs. Significant reduction of 52.4% and 56% in SVNM is made by P3 cell compared to 6T and PP cell respectively.

Figure 7. SVNM Comparison

2. Write Trip Voltage (WTV)

Fig. 8, shows that due to lowering of the sub-threshold current in the P3 cell WTV is reduced by 62.8% and 43.8% compared to 6T and PP SRAM cell respectively.

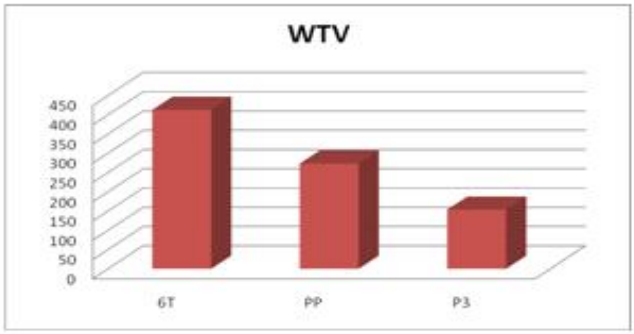

Figure 8. WTV Comparison

CONCLUSION

In this paper the sub-threshold leakage analysis of the proposed P3 SRAM cell has been carried out. It has been observed that due to pMOS stacking and full supply body-biasing, there is a reduction of 70% and 86% in sub-threshold leakage current at V_{DD}=0.8V and V_{DD}=0.7V respectively as compared to conventional 6T SRAM cell. While a significant leakage reduction of up to 91.8% is achieved as compared to PP SRAM at V_{DD}=0.7V. A reduction in the standby power of 86% and 89% has been achieved w.r.t the 6T and PP SRAM design at a bearable expense of the SVNM and the WTV.

Acknowledgment

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