# Automatic PCB Inspection Algorithms: A Survey

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## 1 abstract

The importance of the inspection process has been magnified by the requirements of the modern manufacturing environment. In electronics mass-production manufacturing facilities, an attempt is often made to achieve 100 % quality assurance of all parts, subassemblies, and finished goods. A variety of approaches for automated visual inspection of printed circuits have been reported over the last two decades. In this survey, algorithms and techniques for the automated inspection of printed circuit boards are examined. A classification tree for these algorithms is presented and the algorithms are grouped according to this classification. This survey concentrates mainly on image analysis and fault detection strategies, these also include the state-of-the-art techniques. A summary of the commercial PCB inspection systems is also presented.

## 2 Introduction

Many important applications of vision are found in the manufacturing and defense industries. In particular, the areas in manufacturing where vision plays a major role are inspection, measurements, and some assembly tasks. The order among these topics closely reflects the manufacturing needs. In most mass-production manufacturing facilities, an attempt is made to achieve 100% quality assurance of all parts, subassemblies, and finished products. One of the most difficult tasks in this process is that of inspecting for visual appearance - an inspection that seeks to identify both functional and cosmetic defects. With the advances in computers (including high speed, large memory and low cost) image processing, pattern recognition, and artificial intelligence have resulted in better and cheaper equipment for industrial image analysis. This development has made the electronics industry active in applying automated visual inspection to manufacturing/fabricating processes that include printed circuit boards, IC chips, photomasks, etc. Nello [1] gives a summary of the machine vision inspection applications in electronics industry.

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Human operators monitor the results of the more than 50 process steps required to fabricate a printed circuit board (PCB). They simply inspect the work visually against prescribed standards. The decisions made by these human inspectors often involve subjective judgment, in addition to being labor intensive [2] and therefore costly, whereas automatic inspection systems remove the subjective aspects and provide fast, quantitative dimensional assessments. These automatic systems do not get tired, do not suffer burnouts, and are consistent day in and day out. Applied at each appropriate step of the assembly process they can prevent value being added after a defect has occurred, reduce rework costs, and make electrical testing more efficient. All of this means better quality at a lower cost. Over the years many researchers [3, 4, 5, 6] have emphasized the importance of automatic inspection systems in the electronics industry.

The major PCB manufacturing stages and process steps involve bare-board fabrication, loaded board assembly, and soldered board process [5, 7, 8]. The increase in automated production line technology has rapidly initiated substitutes for human visual inspection. These systems have been produced with distinct and limited capabilities for covering the fault spectrum at each significant stage of PCB manufacture [5]. Even to date machine vision community considers automatic bare PCB inspection to be the most mature industrial visual inspection application. The problems of loaded-board and soldered-board inspection have been addressed but the results are typically limited to detection of more noticeable discrepancies [9]. Due to the following criteria, the sophistication in automated visual inspection has become a part of the modern manufacturing environment [6, 10, 11, 12, 13, 14]:

- They relieve human inspectors of the tedious jobs involved.
- Manual inspection is slow, costly, leads to excessive scrap rates, and does not assure high quality.
- Multi-layer boards are not suitable for human eyes to inspect.
- With the aid of a magnifying lens, the average fault-finding rate of a human being is about 90%. However, on multi-layered boards (say 6 layered), the rate drops to about 50%. Even with fault free power and ground layers, the rate does not exceed 70% [11].
- Industry has set quality levels so high that sampling inspection is not applicable.
- Production rates are so high that manual inspection is not feasible.
- Tolerances are so tight that manual visual inspection is inadequate.
- As packaging technologies become increasingly complex, substrates become more costly, hence scrap be minimized.

Most vision systems for automated industrial inspection are custom designed, so they are only suitable for one specific application. A variety of approaches for automated optical inspection of printed circuit boards (PCBs) have been reported over the last two decades. Though inspection of bare PCBs is the most mature industrial inspection application, there is no single publication which comprehensively surveys the techniques studied this far. The most recent review on automatic visual inspection [15, 16] has a section dedicated to the inspection of PCBs. This review covers very briefly some of the recent advances in PCB inspection, along with the

techniques that were published in [17, 18, 19]. Sanz and Jain [20] presented a good review of the printed wiring board algorithms. This survey is an attempt to put together the advances made solely in the field of bare PCB visual inspection. The significant improvements in this field justify this survey. In this survey, algorithms and techniques for the automated inspection of PCBs are examined. This survey concentrates mainly on image analysis and fault detection strategies, which include state-of-the-art techniques. Limitations of current inspection systems are presented. One of the goals of this study is to collect most (if not all) of the articles in this field published to date, to classify and discuss them according to the methodologies employed. All of these will be discussed under a consistent set of terminologies (where variations will be mentioned) in the hope that such a unified treatment will be helpful.

### 2.1 Types of Inspection

PCB flaw detection procedures can be broadly divided into two classes [12, 21]: electrical/contact methods and non-electrical/non-contact methods. Electrical test methods can find flaws such as shorts and opens; the others require some other methods of detection. Even though many design parameters can be successfully checked by electrical test [22], it has limitations that could allow defective products to pass. Potential defects such as line width or spacing reductions are not detected, nor are cosmetic defects or those caused by process problems. Defects like excess copper on an inner layer, which may cause failure of the final board, are also missed. Further, electrical testing is very setup-insensitive. As boards come to be designed on grids of less than 0.1 inches, the fixtures necessary for testing become extremely complicated and expensive. Electrical testing, therefore, augments visual inspection but cannot replace it. The double-lined boxes in Figure 1 designate stages at which electrical testing can in principle, be applied. An image of a PCB can be acquired using visible or invisible light and then analyzed for defects. Most common and reliable methods reported in the literature have made use of light in the visible part of the spectrum. This section briefly lists some of the different inspection systems based on different imaging technologies. Some of the non-contact automatic inspection methods that are currently available are [21, 23, 24, 25, 26]:

- Automatic Visual/Optical inspection : Automatic optical inspection (AOI) systems detect the same type of surface-related defects as manual inspection, including bare-board inspection, solder bridging, lack of solder, missing components, poor part orientation, lifted leads, tombstoning, and solder balls. Considering bare-board defects optical testers can find defects other than shorts, and opens, such as line width errors, pad mousebites, and trace misplacements. This paper focuses on the automatic inspection of bare-boards. The loaded-board inspection systems can be found in the following references [7, 27, 28]. Automatic optical inspection has the following characteristics that contact testing (electronic testing) does not have [11, 29, 30]:
  - It recognizes potential defects such as out-of-specs, line widths, line spacing, voids, pin holes, etc. These are not always traceable by contact testing methods. Narrow lines burn up over long periods or under fairly large currents. Also, in high frequency circuits, these defects may cause leakage, parasite capacitance, impedance or mutual inductance. Therefore, after electronic testing, a PCB may still not operate effectively at the system level.

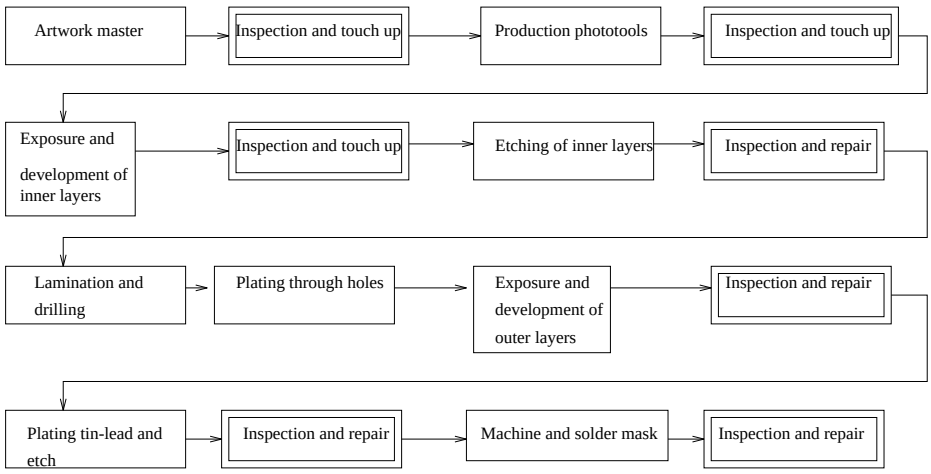



Figure 1: Stages in Multilayer PCB fabrication

  - An AOI system is not confined by a design grid during inspection - unlike most electronic testing equipment.
  - AOI can inspect artwork and provides strict product control from the onset of production.
  - AOI is a non-contact inspection, thus avoiding mechanical damage.
  - Electrical test methods are expensive because of the number of fixtures required.

- X-ray imaging : X-ray imaging systems [2, 24, 30] are used for rapid and precise measurement of multi-layered PCBs. Based on the measurements of individual test pads, the system supplies specific information on layer registration, distortion and the torsion of the layers. X-rays also reveal minute defects, such as hairline cracks, which escape other methods of inspection. SMD defects like heel cracking, voids, component misalignment, bridging, insufficient solder, excess solder, solder threads and balls, poor wetting, and bent leads can be detected using X-rays.

- Scanned-Beam Laminography : Laminography [30] provides cross-sectional X-ray imaging which separates the top and bottom sides, or any other layer of the PCB, into cleanly separated images. The basic principle of laminography is to move the X-ray source and the X-ray image detector around on opposite sides of the object. As long as the X-ray beam always passes through the same points in the object and the same points in the detector simultaneously, a cross-sectional image is formed in real time. By changing the size of the X-ray scanning circle, the field of view and magnification of the image can be varied on the fly. This enables inspection of fine-pitch components at high magnification and of other components at normal magnification to optimize throughput.

- Ultrasonic Imaging : Ultrasonic imaging technology best detects solder-joint defects such as internal voids, cracks, and disbands. An ultrasonic imaging system [31] generates precise

images by scanning a focused piezoelectric transducer signal in a raster pattern over the solder joints. A coupling fluid allows transmission of short pulses of ultrasonic energy produced by the transducer to reach the solder joints. Defects or the juxtaposition of dissimilar materials make their presence known by reflecting (echoing) the high-frequency pulses. In practice, this system is limited to simple solder-joint geometries. For extremely fine-pitch surface mount applications, the reflection and refraction effects may scatter the pulses, making detection difficult.

- Thermal Imaging : Thermal imaging systems [24] indicate hot spots on operating PCBs indicating shorts and overstressed components. Usually these systems find success in applications in which automated measurement of heat is utilized to understand process performance or in which temperature measurement and control are vital to process yield. Compared to optical and X-ray inspection systems, thermal inspection systems are less automated [30]. Laser scanning systems [2] belong to this category. They are successful in differentiating between PCB copper and substrate. Using infrared detectors distinctive thermal profile of the defective solder joints over normal joints can be detected.

## 2.2 Stages in Multilayer PCB fabrication

The actual inspection conditions that exist at different points of the multilayer PCB manufacturing process [12, 32] are as follows. Figure 1 depicts these stages along with the points where visual inspection can be applied.

- Artwork masters: These are silver halide 1 : 1 scale transparencies of the conductor pattern on film. For very high-quality products, glass masters are also in use. Artwork masters are produced in most cases by computer driven photoplotters. Defects on the master will directly affect all ensuing production batches of the given PCB. Therefore, a great deal of work is usually put into the incoming inspection and touch-up of artwork masters. Investigations of the propagation of defects from the artwork master and phototools to the finished board show that the smallest defect on the master or tool which is transmitted to the finished product has dimensions of approximately 1 mil. The most common defects on artwork masters are caused by scratches and dust particles. These show up on the finished product as opens, shorts, and pinholes or copper splashes.

- Phototools: These are silver halide or diazo transparencies obtained by contact printing from the artwork master. They are used for the actual exposure of the boards. The inspection needs and defects of artwork masters apply also to phototools.

- Inner and outer layers after exposure and development: These are sheets of copper-clad laminate, overcoated with photoresist, with the conductor pattern exposed on it. Many of the defects found after etching were already present as defects in the photoresist pattern. Inspection at this stage is very beneficial because of the possibilities to touch-up or strip-and-repeat the photoresist process. Defects caused by dust and other foreign particles during exposure can be added to the list of defects mentioned for artwork and phototools. Imperfect rinsing of the photoresist may leave excess material on the panel, which can create opens after etching.

- Inner layers after etch and strip: This is the point at which most of the visual inspection is invested in the multilayer manufacturing cycle, because this is the last inspection stage before lamination. After this point, a defective inner layer in the multilayer board is not repairable. Defects mentioned thus far can appear at this stage, in addition to subsequent defects like over- and under-etch, which lead to narrow conductors or spacings and excess copper. Exact gauging of conductor and spacing widths is usually necessary at this stage.

- Outer layers after etch: As in the case of inspection of the inner layers after etch, this is the last point at which repairs can be made on the conductor pattern. The AOI problem is different at this stage because of the appearance of holes and the necessity of inspecting their annular rings for width and breakout.

- Inspection after machining and solder masking: This is mainly a cosmetic final inspection. Defects in the conductor pattern can hardly be detected at this stage because the solder mask obscures the conductors.

### 2.3 Defects

Printed circuit boards are inspected extensively before the insertion of components and the soldering process to isolate defects (also called anomalies or faults). Even though automated approaches are used in the verification of artwork [33, 34, 35, 36], before beginning actual etching process on the board, bare-board defects still exist. Hall [33] outlines the processing and post-processing steps involved in the verification of artwork design. A variety of defects can afflict the copper pattern of PCBs; not all mean immediate rejection of the board from consideration. The types of faults range from hair-line (e.g., size equal to 100 microns) breaks and bridges as small as 1 mm between conductor paths, to unacceptable enlargements and reductions in line widths, to poorly formed plated through holes. The anomalies looked at, for example are: *unetched copper*, *open* (break or cut), *partial open* (mousebite or nicks), *scratches or cracks*, *shorts*(bridge), *incipient short* (fine wiring), *overetching*, *underetching* (abnormal wire width), *pad size violations*, *spurious* (excess or residual) *metal* or *metal specks*, *spurs* (protrusions or whiskers or smears), *cracking of walls of holes*, *violations of spacing of holes*, *violation of spacing of conductor traces*, etc. A wide variety of terminology is used in naming these faults. The above list gives the commonly associated names used in naming the defects, followed by other popular/unpopular names in parenthesis.

Figure 2 shows an artificial defect-free PCB image pattern. This figure depicts through-hole PCB patterns, printed wiring board patterns, and surface mount PCB patterns in the same image. Because most of the defects are common to all three varieties of boards, the three different patterns are shown in one example image. Figure 2.3 shows the same image pattern as in Figure 2 with a variety of defects shown in it. Though each defect shown in the figure is a representative example for that particular defect, the shape and size of the defect varies from one occurrence to another. Smaller and smaller lines and spaces make these defects more serious, more likely and harder to detect. Studies [29, 37, 38] show that open/partial open, short, pinhole, breakout, overetch, underetch are the most frequent defects that occur. These defects are caused due to one or more of the following errors [21, 37]:

- thermal expansion of the artwork during printing, or by defective etching,

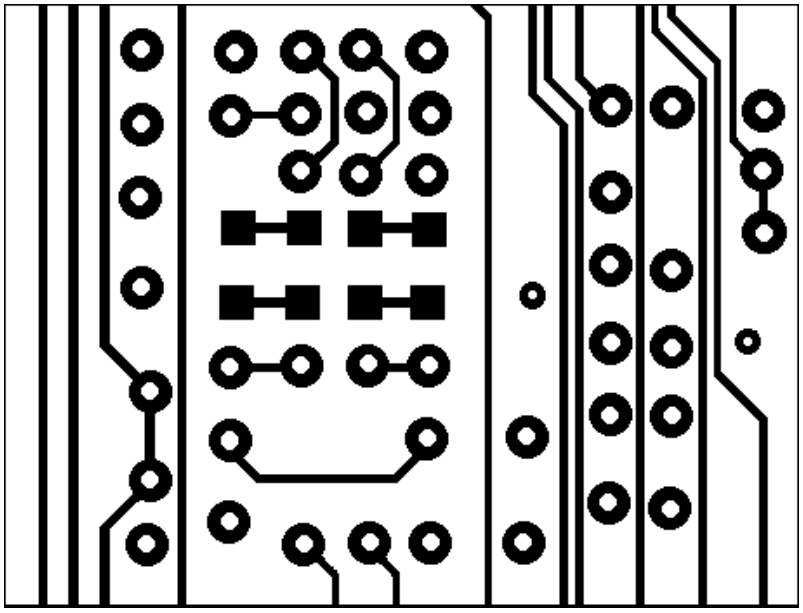
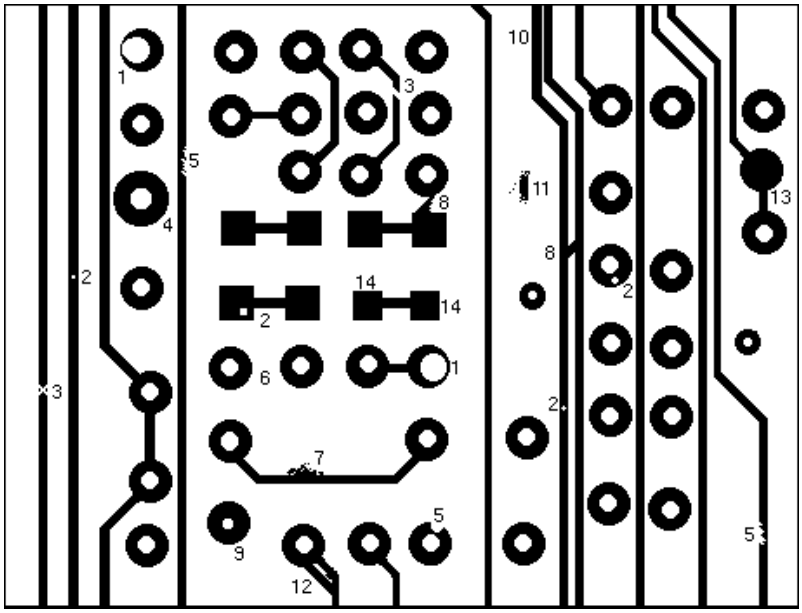


Figure 2: Example of Good PCB Patterns

- dirt on board, air bubbles from electrolysis,
- incorrect electrolysis timing,
- mechanical misregistrations,
- distortions of the PCB due to warping, etc.

Thibadeau in [39] gives a good summary of some defects and their causes that occur during the fabrication of PCBs. The dimensional variations in the conductor spacings and widths due to seasonal temperature and humidity changes should be taken into account. Further, 1 *mil* faults require at least 0.5 *mil* imaging resolution, therefore dust, hair, lint, and fingerprints become unwanted noise sources for false-alarms, making cleanroom conditions necessary [5]. Although it is possible to detect initial defects such as conductor breaks and short circuits through conductor tests, these tests cannot reveal overetched conductors, limited conductor spacing, and other defects that can lead to deterioration with age [32]. In addition to defect detection inspection of bare PCBs demands [40]:

- high speed,
- high data rate,
- high detection accuracy, and
- a low false-alarm rate.



1. Breakout
2. Pin Hole
3. Open Circuit
4. Underetch
5. Mousebite
6. Missing Conductor
7. Spur
8. Short
9. Wrong Size Hole
10. Conductors too close
11. Spurious copper
12. Excessive Short
13. Missing Hole
14. Overetch

Figure 3: Example of Defective PCB Patterns

# 3 Components and Terminology Involved

This section briefly defines the most commonly used terminology in this field. The reader is not provided with any rigorous and complete definitions. Interested readers are advised to refer to recent picture processing or machine vision text books to get a complete understanding of the individual subjects involved. This section also identifies the major components of an inspection system. Though there is distinction between printed circuit boards (multilayer), printed wiring boards, and surface mount boards, in this paper the generic term *printed circuit board* (PCB) is used to refer to all of them. This is because most of the defects and techniques of defect analysis are common for all of them. Also it is worth mentioning that some of these techniques are used in other types of inspection [8, 20, 41, 42, 43, 44, 45] like integrated circuit inspection, thick film and hybrid circuit inspection.

A typical inspection process involves observing the same type of object repeatedly to detect anomalies. The process involves digitization of the object to be inspected for visual data and the analysis involves the processing of the imagery to enhance relevant features and the detection of defects. One inspection procedure of such a system first precompiles a description of each of a known set of defects and then uses these models to detect defects in an image. Another procedure models the part by its normal, expected features and then uses the part model to verify in an image that the part under inspection has all the expected features. Foster *et al.* [10] and Chin [46] outlined the major issues involved in PCB inspection, and industrial inspection in general. The following discussion outlines some of the major components involved in automated visual inspection systems:

- Hardware System: Industrial PCB visual inspection ideally requires a cost-effective off-

the-shelf system. This means that it should be designed to take into account operation speed, reliability, ease of use, and modular flexibility, in order that it can be adapted to different inspection tasks [11]. The main hardware components of the inspection system are the material and component handling system, illumination system, image acquisition system, and the processor.

- Material and Component Handling System: This system comprises the mechanism which presents the part or assembly, denoted material, in different orientations to the components of the automated visual inspection system [47].
- Illumination System: Suitable lighting and viewing conditions facilitate inspection, avoiding the need for complex image processing algorithms. Many researchers have pointed out the importance of lighting techniques [48, 49, 50]. The main parameters that characterize the suitability of an illumination system to acquire an image of good quality are: (a) *intensity*, (b) *uniformity*, (c) *directionality*, and (d) *spectral profile*. The relative importance of these parameters and the degree to which each one must be controlled are largely governed by the surface characteristics of a given PCB and the constraints imposed by the camera. Examples of different surface characteristics include [51]: (a) etched clean copper, (b) oxide coated copper, (c) blue photoresist, (d) red photoresist, (e) solder before reflow, (f) solder after reflow, (g) layers that are opaque, (h) thin transparent layers, and (i) phototools. Most of the inspection systems built to date either require good lighting conditions or they employ different lighting techniques. Among the lighting techniques most commonly used are [37, 48, 49, 50, 52, 53]: standard light sources, indirect and back lighting, fluorescent

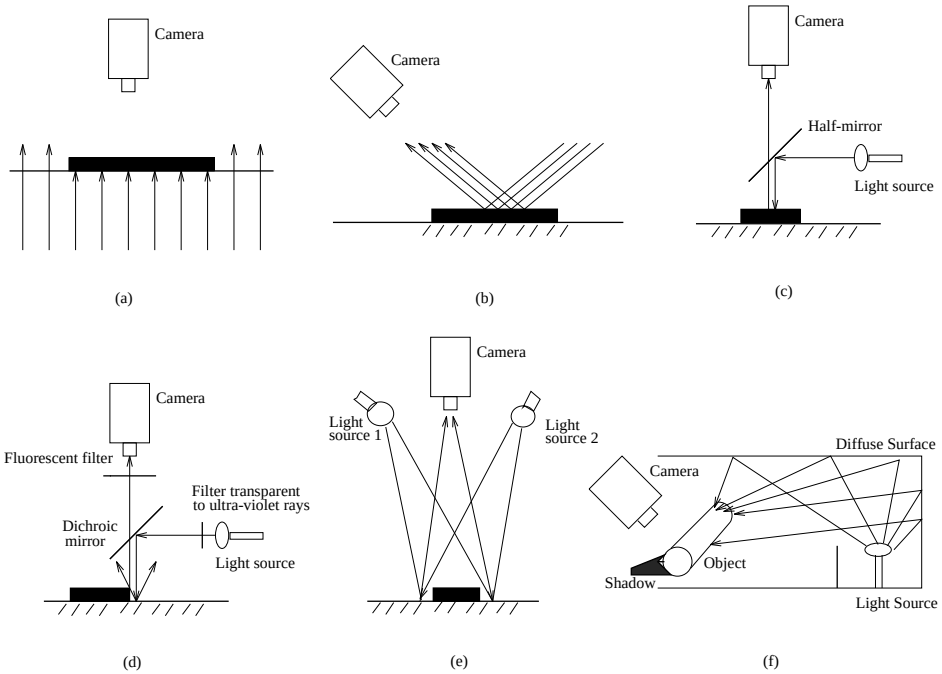



Figure 4: Different illumination techniques (a) Back lighting (b) Directed lighting (c) Vertical lighting (d) Fluorescent lighting (e) Bidirectional lighting and (f) Diffuse lighting

lighting, reflected (vertical) lighting, bidirectional lighting, diffuse illumination, fiber-optic, quartz-halogen light sources, etc. Some of these lighting techniques are shown in figure 4. An appropriate lighting configuration is determined by judgement and experimentation. For example, Hara *et al.* [54] have experimented with reflected and fluorescent lighting techniques. In case of reflected light Figure 4(c), the PCB was illuminated with a super high-pressure mercury lamp, and the reflected light is detected by using a CCD linear image sensor. In fluorescent light detection Figure 4(d), as the amount of fluorescent light emitted by the base material is small, a high sensitive image tube type TV camera is used to detect the light signals. A dichroic mirror is used to reflect short wavelength radiations along with various types of filters used to completely separate the excitation radiation from the super high pressure mercury lamp, leaving adequate fluorescent light signals.

  - Image Acquisition System: Images are usually acquired by use of a camera or a digitizer that acts as a sensor. There are a several types of cameras available and the determination of the appropriate type is dictated by use. Examples of different types are television camera (a charged coupled device (CCD) camera), laser scanner camera, etc. AOI System Corp. developed the AOI-20 system that utilizes as many as 20 CCD cameras [32]. The MOP-5002 system operates with one or two cameras which scan the PCB image through linear CCD sensors, where high precision lenses guarantee the maximum possible resolution and a wide depth of field. Every camera has its own microprocessor system just for camera functions such as automatic focus, automatic exposure, and automatic contrast adjustment. Grey scale processors and real time digitization facilities break the image down into individual points.
  - Processor: The processor system usually consists of a high speed computer system. Most of the commercially available systems have special processors designed solely for inspection purposes. A commercially available inspection system, AOI-20, uses a high speed parallel processing system [32]. Anzalone *et al.* [55], implemented their inspection system on the SMAE multiprocessor SIMD/MIMD architecture emulator.

- Resolution: Any adequate vision system must have sufficient resolution to detect the potential faults under inspection. The pixel size of the smallest fault to be detected should be at least twice that of the vision system; i.e., *two mil* minimum fault size requires a *one mil* system pixel size. A smaller pixel size usually means a smaller field of vision if no compensating techniques are employed (multiple cameras, etc.).

- Image Enhancement: Involves removal of noise, enhancement of edges, enhancement of contrast, etc. Thresholding (point processing operation), convolution (group processing operation), and picture processing (processing over the entire image) are some of the techniques used for enhancement of the images [47, 56].

- Feature Extraction: The decision regarding what features to be considered is rather subjective and depends on practical situations. Features are less sensitive with respect to the encountered variations of the original noisy gray-scale images and provide data reduction while preserving the information required for the inspection. Most of the procedures used for feature extraction are simple edge-detection, line tracing, and object shape properties.

- Model-Based System: The most common inspection technique is the model based process,

which performs inspection by matching the part under inspection with a set of predefined models.

- Modeling: Modeling involves *training*, in which the user uses a model part to teach the system the features to be examined, their relations, and their acceptable tolerances.

- Detection/Verification: Detection process consists of matching the extracted features from the image under inspection with those of the predefined model. A typical detection procedure involves simple comparison, like image subtraction. The detection process becomes very complex if the image to be inspected is noisy and the features could occur at random positions and orientations. Detection using representative features and their relationships provide a way to inspect a part and locate defects on the basis of measurements taken from key features. These methods are usually computationally intensive.

- Boundary Analysis: Models of good boundaries are compared with those of the board being inspected [57, 58].

- Thinning, Contraction, and Expansion: These are image-to-image transformation operations [59, 60]. These operations are defined using neighborhood connectivity relations. An expansion sets all background pixels in an image to foreground pixel value, if any one of the neighboring pixel values is equal to the foreground pixel value. Contraction is realized by first expanding the complement of an image and then taking the complement of the result. Thinning reduces an entity to its skeleton, a simplified version contained in the original entity that retains the basic shape of an entity. Unlike expansion or contraction, thinning maintains the connectivity [61] of an entity and preserves its holes (none are removed or added). Different definitions and implementations of these operations can be found in [62, 63, 64, 65].

- Morphology: This refers to a branch of nonlinear image processing and analysis. The basic idea is to probe an image with a structuring element and to quantify the manner in which the structuring element fits (or does not fit) within the image. The operations of dilation, erosion, opening, closing, etc., are used in this type of image processing. A complete treatment of this subject can be found in references [66, 67].

# 4 Algorithms

Eduardo [15] has grouped the conventional visual inspection tasks into three broad categories based on the types of defects they detect: (a) dimensional verification, (b) surface detection methods, and (c) inspection of completeness. The conventional PCB bare-board inspection algorithms could as well be put into these categories. Sanz and Jain [20] classified the printed wiring board inspection techniques into the following four different categories: run-length-based methods, boundary analysis techniques, pattern detection methods, and morphological techniques. A classification based on the nature of the information (design specification data/direct or indirect image related data) of the algorithms use for fault identification is presented here. A large number of PCB inspection algorithms have been proposed in the literature to date, Figure 5 shows the classification of these algorithms. In general, they fall into one of three categories: reference comparison (or referential approaches), non-referential approaches, and hybrid

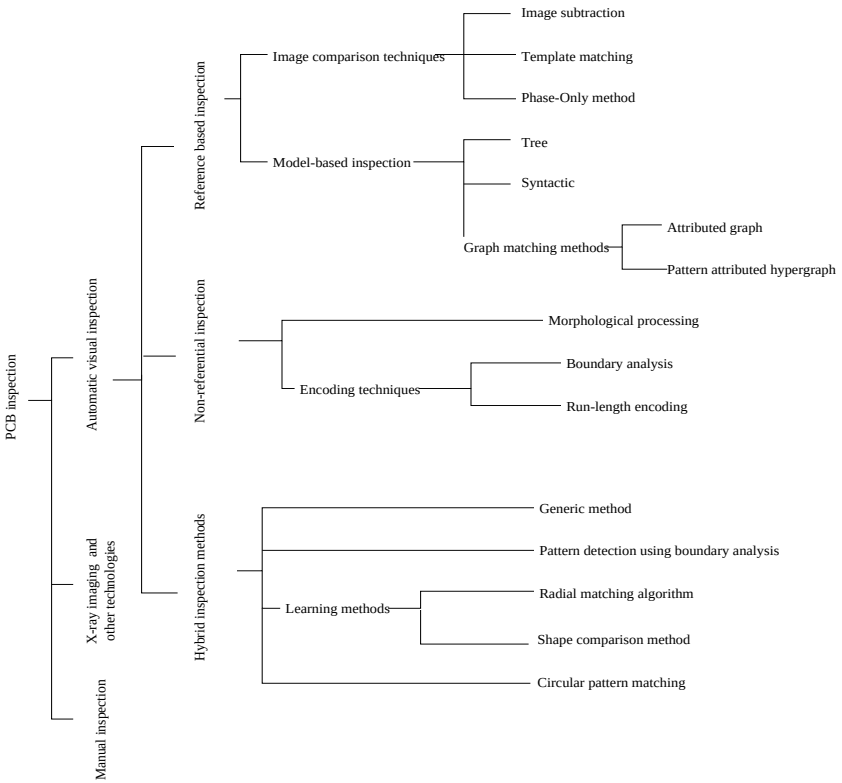



Figure 5: Classification of Inspection Algorithms

approaches - which involve a combination of more than one of these methods. The reference comparison approaches use complete knowledge of the circuit under test, whereas the non-referential approaches use the knowledge of properties common to a circuit family but not knowledge of the specific circuit under test. There are two types of reference comparison methods: the simpler approaches involve some kind of direct image comparison, between pixels in the test image and in an idealized reference image. Somewhat more sophisticated approaches involve recognition of circuit features in the test image followed by a comparison against a set of reference features. The non-referential approaches either work on the assumption that features are simple geometric shapes and the defects are unexpected irregular features or on directly verifying the design rules. Basically, these methods, use local neighborhood processing techniques over the image to be inspected. In these methods, the task is to determine whether each feature falls within the required dimensions. This approach does not require precise alignment, but might miss large flaws and distorted features.

## 4.1 Referential Modeling

The referential methods execute a real point-to-point (or feature-to-feature) comparison whereby the reference data from the surface image of a "good" sample is stored in an image database. These methods detect errors like missing tracks, missing termination, opens, shorts, etc. The drawback of this method is that, since differences between the PCB under inspection and a "golden board" or CAD data are called defects, board distortions, as a consequence of processing, may be identified as anomalies [29].

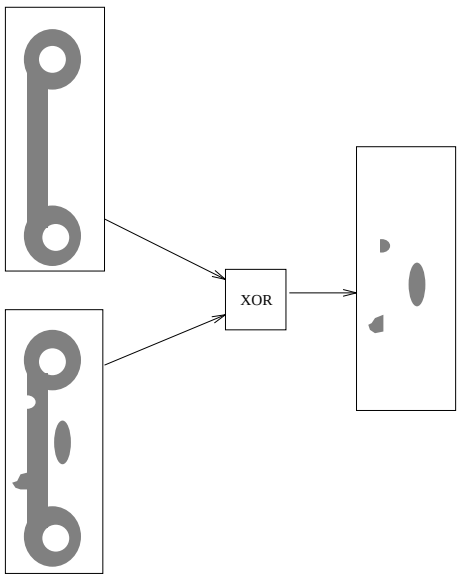


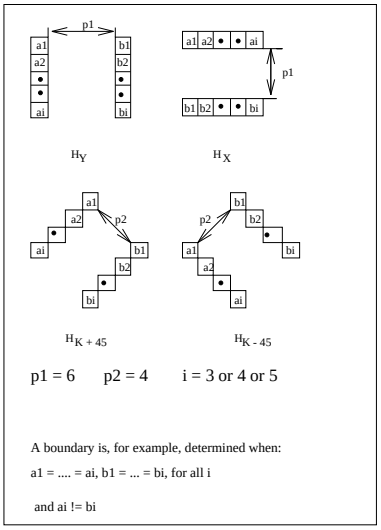

Figure 6: Image Subtraction

#### 4.1.1 Image Comparison Techniques.

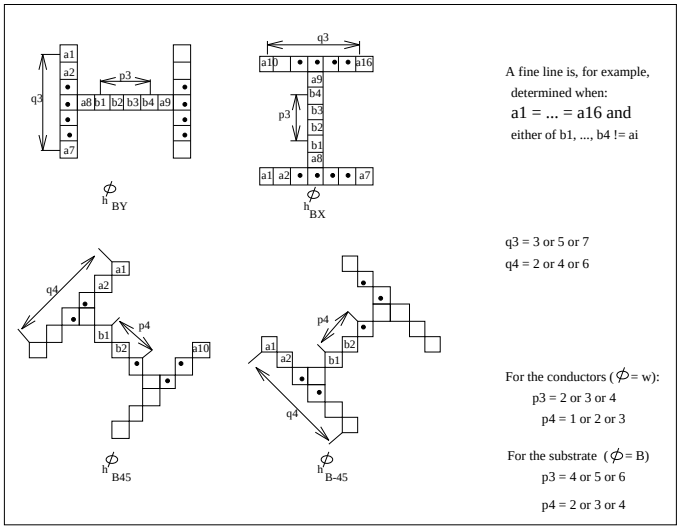
**Image Subtraction** Image subtraction is the simplest and most direct approach to the PCB inspection problem. This is one of the earliest techniques employed in inspection [68]. The board to be inspected is scanned and its image is compared against the image of an ideal part. The subtracted image, showing defects, can subsequently be displayed and analyzed. Figure 6 shows this direct subtraction process as a logical XOR operation on the subimage patterns of the PCB. The advantages of this method is that it is trivial to implement in specialized hardware and therefore high pixel rates can be obtained. Another advantage is that it allows for verification of the overall defects in the geometry of the board. This technique suffers from many practical problems, including registration, color variation, reflectivity variation, and lighting sensitivity. A fairly high tolerance of the PCB board makes the method too restrictive for practical use. One other problem is that statistical analysis must be performed to determine if the differences are due to nonconformities or due to alignment.

**Feature Matching** Feature matching is an improved form of image subtraction, in which the extracted features from the object and those defined by the model are compared. The advantage of this matching is that it greatly compresses the data for storage, and at the same time reduces the sensitivity to the input data and enhances the robustness of the system. This matching process is called *template matching* [69, 70]. One of the major limitations of template matching for inspection is that an enormous number of templates must often be used, making the procedure computationally expensive. This problem can be eliminated if the features to be matched are invariant in size, location, and rotation. The disadvantages of this method are that it requires a large data storage for the ideal PCB patterns, and precise registration is necessary for comparison. It is sensitive to illumination and digitization conditions, and the method lacks flexibility. Hara *et al.* [54, 71, 72] developed at Hitachi a defect detection method based on feature extraction and comparison. Large defects are detected by extraction of boundaries using $H_{KX}, H_{KY}, H_{K45}$, and $H_{K-45}$ operator templates, shown in Figure 7(a), in the four directions $(0^o, 90^o, +45^o, -45^o)$. These templates are used for detection of all defects of width greater than a fixed value and for isolated defects. Narrow defects, like fine wiring and whiskers, are detected by searching in four directions $(0^o, 90^o, +45^o, -45^o)$ using $h^{\phi}_{BY}, h^{\phi}_{BX}, h^{\phi}_{B45}$, and $h^{\phi}_{B-45}$ operator templates, shown in Figure 7(b). The final result of extraction is a logical AND of the four direction features extracted. The sizes of the templates $H_{**}$ are not fixed and can be regulated by setting limits on the lengths, orientations and widths of the patterns. These different sizes are necessary to precisely identify the boundaries, as the trace pattern widths may change and also big hops can be made using larger template sizes in the uninteresting regions (e.g., which do not have trace pixels), thus reducing unnecessary computation time.

Figure 7(c), explains the extraction of pattern features and defect recognition procedure: (1) shows the two patterns f (defective pattern) and g (non-defective pattern) that are compared; (2) shows the boundary images $F_K$ and $G_K$ obtained by applying the $H_{KY}$ operator in Y direction; and (3) shows the fine-line boundary images $F_B$ and $G_B$ obtained by applying the $h^{\phi}_{BX}$ operator in the X direction. Defect recognition involves the comparison of $F_K$ and $G_K$ (or $F_B$ and $G_B$)




(a) Boundary Extraction Operators




(b) Fine-line Extraction Operators

| | Pattern f and its processed image | Pattern g and its processed image | Feature Extraction Operators | Result of comparison of F and G |
|---|---|---|---|---|
| (1) Detected patterns f, g | f | g | | |
| (2) Extracted boundry lined $F_K G_K$ in the Y direction | $F_K$ | $G_K$ | | |
| (3) Extracted fine line pattern $F_B$, $G_B$ in the direction X | $F_B$ | $G_B$ | | |

(c) Extraction of features and comparison of the extracted feature patterns

Figure 7: Local Feature Matching Method

images. When the corresponding points on the reference pattern and PCB test pattern exhibit the same features, the pattern is free from defects. Otherwise a defect exists. In part (3) of Figure 7(c), a short (shown as a narrow line) is detected. The advantage of this method is that the complete system can be implemented in hardware. The system works on 5.5 *mil* lines and 500 *mil* $\times$ 600 *mil* boards with a speed performance of 2.5 *min/panel*.

**Phase-Only Method** David *et al.* [73] discuss an alternative method to standard template matching technique which is based on phase-only imaging. A phase-only image is an image which has unit power spectral density amplitude so that all information is contained in the phase. Phase-only image comparison has the properties of redundancy removal (correlation between data points is removed) and edge enhancement. The method uses Fourier transform, followed by normalization of the resultant image, to spread over the entire grey scale range (by dividing each spectral point by its own magnitude), and then inverse Fourier transforms an image pair to produce a map of significant image differences. Because the correlations of any pair of data points in the image are removed, all periodic components of the image are suppressed. Two similar images can be compared by creating a composite image by placing them side-by-side and applying a phase-only transformation at once. If the two images are very similar, a strong periodic component with period equal to the subimage spacing appears in the spectrum of the composite image. By suppressing this component, all points which correspond to the two subimages will be suppressed, and only the differences remain. The paper presented examples of real and simulated images with different illumination levels, lighting gradients, and board substrate colors, all compared with the same master reference. This method has advantages over conventional template matching/comparison techniques because of its light intensity invariance, insensitivity to illumination gradients, tolerance to misregistration of the images to be compared, and invariance to translation. The method suffers from the disadvantage that it requires a large amount of computational time compared to simple template matching methods.

### 4.1.2 Model-Based Methods.

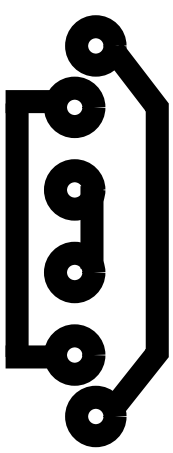
Model-based methods are techniques which perform inspection by matching the pattern under inspection with a set of predefined models. The selection of a suitable model representation of the training patterns strongly affects the performance of an inspection system. For example, one of the approaches that falls into model-based techniques is the syntactic approach, also called string matching technique. In the syntactic approach [74, 75], a PCB image is modeled as a finite set of alphabets/symbols. The method involves tracing the boundary to produce an ordered list of boundary points, and analyzing the shape to produce syntactic description of the shape using primitive shapes that best describe the PCB pattern. The detection of defects then involves the detection of local defective features expressed in finite regular expression form. One major limitation of this syntactic approach is that the choice of primitives in quantifying the basic shape involved in the patterns is a difficult problem. This makes the approach not applicable for a real time application like this.

**Graph Matching Methods** The graph matching methods are based on the structural, topological, and geometric properties of the image. The idea is based on the topological/structural comparison which compares the standard graph obtained from the conductor and insulator im-

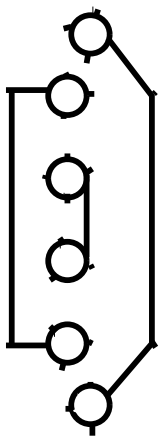
age patterns of the reference PCB with those of inspection boards. For example, topological information incorporates a weighted graph composed of several types of nodes, edges, connections, and their location [76]. Pavlidis [77] presented a technique for converting raster data into a line adjacency graph describing the transition between the conductor and the substrate. Then this graph is searched to obtain a list of the boundary points of the regions and holes in the image. A technique based on matching the linear adjacency graph of the test board to a model graph is presented as an application to printed wiring board inspection.

**Attributed Graph** Darwish and Jain [62] proposed a method that works in two main steps. In the first step, the image is transformed into a collection of nodes that describes the 2-D shape of the different objects in the image. These nodes are connected together depending on relational properties between primitives belonging to the same object and between different objects. Spatial relations are added to the graph in the form of directed attributes, which describes connectivity and neighborhood relationships. This graph is called an *attributed graph*(AG). The second step involves a model verification process. This matching process between the inspected and model patterns is the most time-consuming step during inspection. A similarity evaluation function is used to measure how well the scene graph matches the model graph. Experimental results indicated 100% detection of all shorts, cuts, and minimum width violations with a zero false-alarm rate. But the complexity of matching AGs is very large, since every node of an AG joins the coupling permutation at each iteration for every attributed relationship. This problem is overcome by Sun and Tsai [63] by reducing the large amount of unnecessary computations done in evaluating scores between impossible couples during the exhaustive permutations. The following section discusses this method.

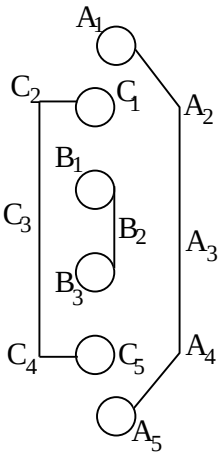
**Pattern Attributed Hypergraph** Sun and Tsai [63] present a representation called pattern attributed hypergraph (PAHG) and a structural inspection algorithm. The proposed graph, called PAHG, describes all segmented regions and the spatial relationship among them. These segmented regions are represented by a regional attributed graph (RAG) that represents a set of primitive features connected to one another within a region, which is the bottom level of PAHG. The top level of PAHG contains regional features and the spatial relations among them. This representation prunes the search space by performing only selective matching operations during the matching phase, thereby reducing the inspection time. This new representation, in which the information is represented in two different levels, is a major improvement over the attributed graph method. Figures 8(a), 8(b) and 8(c) show all the steps involved in the construction of the bottom level of PAHG. This step involves thinning of the binary image, then smoothing the thinned image using the pruning operation in order to eliminate spurious effects in thinning and then labeling the pruned pattern. Figure 8(a) is thinned to obtain Figure 8(b). Figure 8(c) is the labeled graph obtained after pruning the Figure 8(b). Figure 8(d) shows the RAG constructed for the sub-pattern of the PCB pattern A. Figure 8(e) shows the PAHG for the complete PCB sub-pattern shown in Figure 8(a). The matching algorithm proposed works by (a) verifying the top level of PAHG on the scene model and reference model, (b) finding the corresponding pairs of RAGs by evaluating the confidence scores between two PAHGs and the pair of RAGs, and (c) verifying each RAG of the scene model with the corresponding RAG of the reference model. A new inspection algorithm was proposed to utilize the hierarchical structure of PAHG



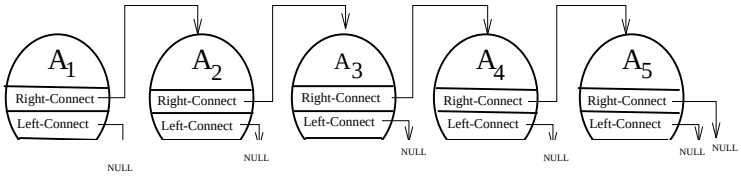
(a) PCB sub-pattern



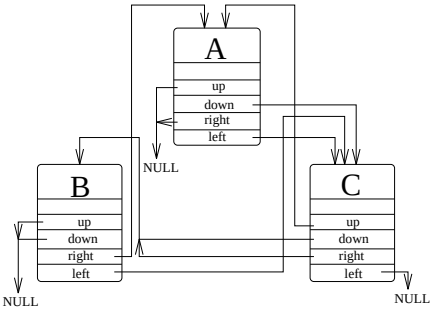
(b) Thinned sub-pattern



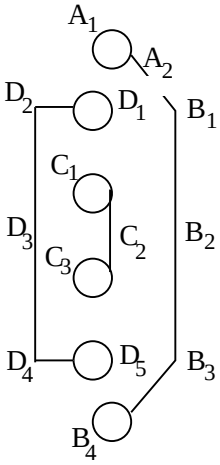

(c) Pruned sub-pattern with lables



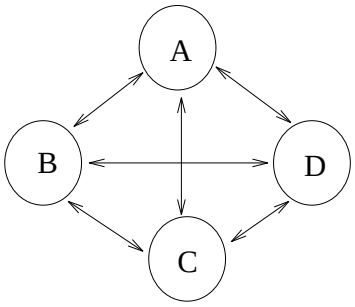

(d) Representation of RAG for segment A in Figure (c)




(e) Graphical representation of PAHG for the sub-image pattern (a)




(f) Pruned defective PCB pattern with lables




(g) PAHG for Figure (f)

Figure 8: Graph Matching Using Pattern Attributed Hypergraph

to improve the matching efficiency. The matching complexity of this method is $1/k^3$ of that of the AG approach, thus making the method more practical.

## 4.2 Non-Referential Inspection

Non-Referential methods do not need any reference pattern to work with, they work on the idea that a pattern is defective if it does not conform with the design specification standards. These methods are also called design-rule verification methods or generic property verification methods [21, 63, 64]. They basically use the design-specification knowledge in verifying the board to be inspected. Applying the design-rule verification process directly to the image patterns is a time consuming process, and hence the response time of the system decreases. Usually these methods process/transform the image into a form which reduces the verification time. The methods use the design characteristics of a PCB as a simple set of rules and feature dimensions and tolerances. Features specified include [78]:

- Minimum and maximum trace widths for all the different traces used,
- Minimum and maximum circular pad diameters,
- Minimum and maximum hole diameters,
- Minimum conductor clearance,
- Minimum annular rings, trace termination rules, etc.

Ejiri [60] developed the classic *expansion-contraction* technique that assumes defects exist in a high first-order spatial-frequency domain (viz., patterns that are small relative to the acceptable patterns). Expansion-contraction methods employ morphological operations like erosion, dilation, expansion, contraction, thinning, etc., in the pre-processing stage. The operators are designed in such a way that they embed the design specifications in them and the result of applying these operators directly reflects the discrepancies in the image patterns, if any exist. Design-specification information is embedded in these operators, such that the transformations generate images that could easily be interpreted for defects. Encoding techniques also transform the image patterns and the verification phase involves interpreting these transformed patterns by extracting the topological features and imposing localized constraints such as minimum or maximum widths to detect anomalies. The disadvantage of these non-referential methods is that they work well in identifying only some kinds of defects, such as in the verification of widths and spacing violations. Also, another drawback of this inspection is that it requires the standardization of the conductor trace types [11], for example:

- Conductor traces must end at solder pads;
- Conductor traces must have a minimum permissible width; and
- Conductor traces must be separated by a minimum permissible spacing.

These non-referential methods depend on sophisticated feature recognition algorithms and may miss flaws that do not violate the rules, such as shorts that are identical to conductors. However, speed is maximized and computer storage requirement is minimized.

### 4.2.1 Morphological Processing.

Morphological processing is one of the widely used techniques in PCB inspection. The inspection involves the expansion-contraction process, which does not require any predefined model of perfect patterns. Ye and Danielson [61] presented an algorithm for verifying minimum conductor and insulator trace widths. The method iteratively applies shrinking (similar to contraction operation) and connectivity preserving shrinking (similar to thinning) operations on the image. After some number of iterations, the difference (logical AND) between the results gives the defects present in the patterns. The main advantage of these methods is that the alignment problem is eliminated. But, the problem with these methods is that different pre-processing algorithms are to be applied to check different violations in the board, which automatically decreases the response time of the system.

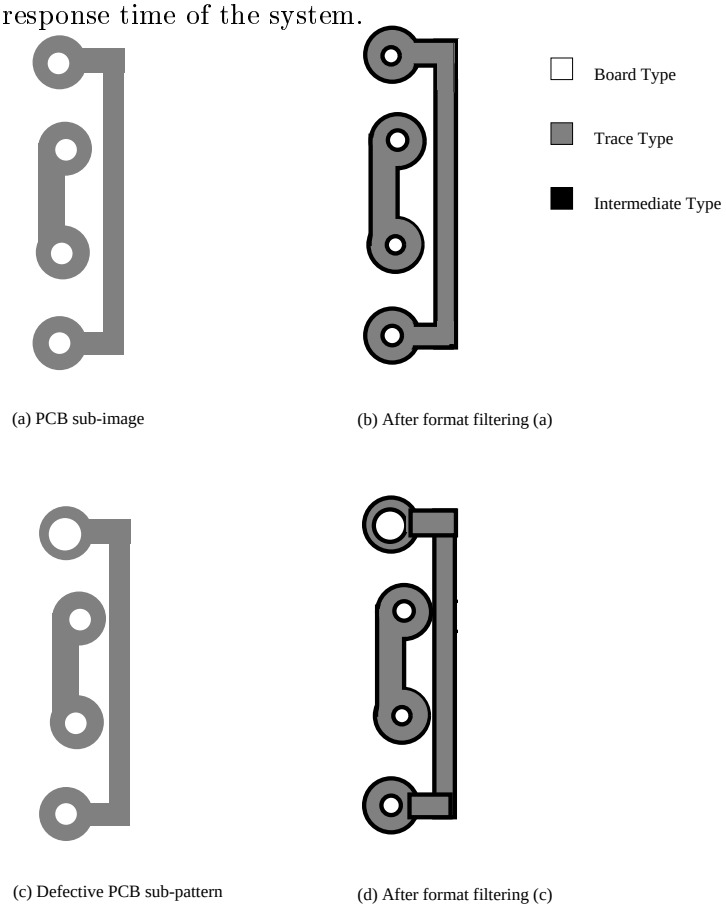



Figure 9: Expansion and Contraction Filtering

Griffin *et al.* [79, 80] discuss an inspection algorithm which is a variation of the shrinking method given by Mandeville [64]. In this method, the image is first enhanced by a formatting filter and then the connectivity through the circuit trace is checked. The formatting filter classifies each pixel of the observed circuit board into one of three types: trace type, board type, or indeterminate type. A pixel is classified a trace (board) type if it is surrounded by a circle of trace (board) pixels with a minimum radius. If this radius is equal to a specified minimum, then at that point the trace (board) satisfies minimum trace (board) requirement. Pixels which are not classified as either trace type or board type are classified as indeterminate. Figure 9(a) shows a PCB sub-image whose output pattern would look like Figure 9(b) after format

filtering. This classification provides a means to check for open/partial opens, minimum trace spacings and surface nonconformities on the circuit boards. Figure 9(c) shows a defective PCB sub-image, which has a mouse bite, wrong size hole and conductor too close defects, and whose output pattern looks like Figure 9(d) after format filtering. Opens/partial opens are identified by checking for connectivity along the trace, where failure of minimum width requirement indicates a break in the connectivity. Minimum spacing requirements are checked by verifying if there are any of the indeterminate pixels of one trace connected to indeterminate pixels of another trace, if any exist, then the minimum spacing requirements are not satisfied. Surface nonconformities like scratches and dust are inspected after the algorithm for width and spacing requirements has been performed. These nonconformities are identified to be the areas of high intensity pixels by subtracting the metal trace pixels from the image whose lighting configuration is such that the source is at an acute angle to the board.

The system proposed by [81] makes use of defect detection algorithms which are derived using image transformations based on mathematical morphology. The system detects: violations of minimum land width requirement (MLW), violation of minimum conductor spacing requirement (MCS), and the violation of minimum conductor trace width requirement (MCTW). The fundamental operations used in the transformations are hit/miss transformation, erosion operation, dilation operation, and symmetrical thinning. The PCB images are supposed to be 3-level digital images as shown in Figure 10(a): substrate pixels with value 0, conducting structure pixel values with value 1, and holes with value 2. A segmentation algorithm which separates the conductor lands surrounding the holes from the conductor traces is employed. This enables the system to apply design-rule checking easily and thus avoiding false-alarms. The following steps depict the algorithm:

1. the original image is transformed using the following rule $0- >0$, $1- >0$ and $2- >1$. Figure 10(b) shows the resultant binary image.
2. the hole locations are enlarged, as shown in Figure 10(c), such that they cover the surrounding lands using dilation operation.
3. transform the original image by the rule $0- >0$, $1- >1$, and $2- >0$. Figure 10(d) shows the resultant binary image.
4. Images obtained in steps 2 and 3 are ANDed. The resultant image after this operation on Figures 10(c) and 10(d) is shown in Figure 10(e).
5. Images in step 3 and 4 are EXORed, resulting the conductor trace image, as shown in Figure 10(f).

Algorithm for verifying minimum conductor spacing (MCS) works as follows. The algorithm can easily be understood with the help of Figure 11, which depicts each step in the process:

1. dilate the original PCB image Figure 11(a) by an isotropic structuring element (an elliptic one). The resultant image is shown in Figure 11(b).
2. the above image is symmetrically thinned and pruned to remove hair like protrusions. The resultant image is ORed with the original image. Figure 11(c) shows the application of this step.

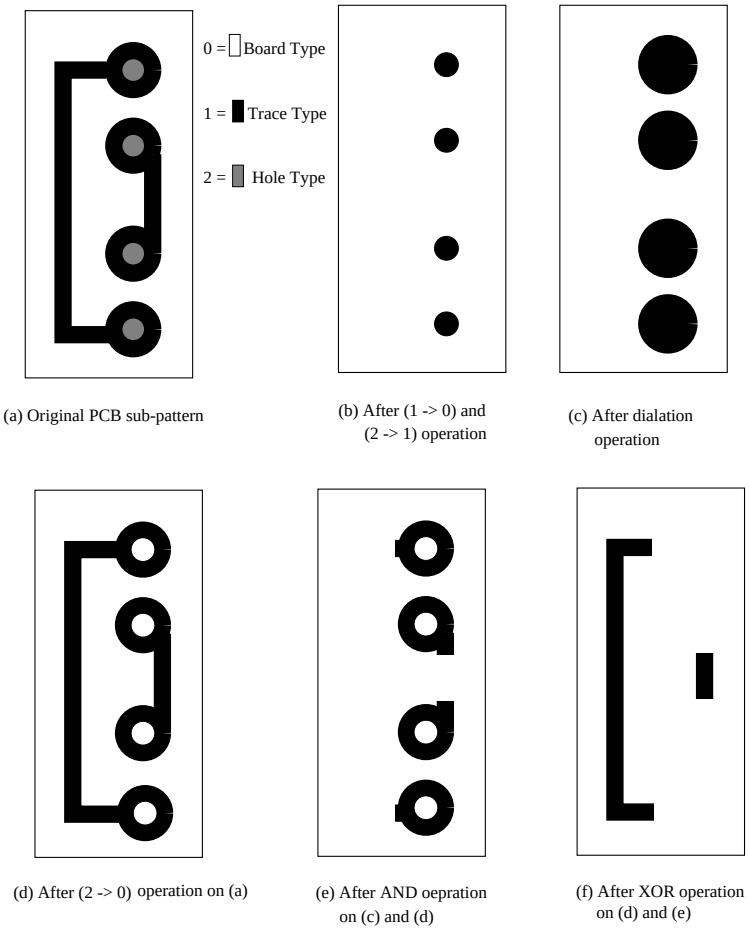
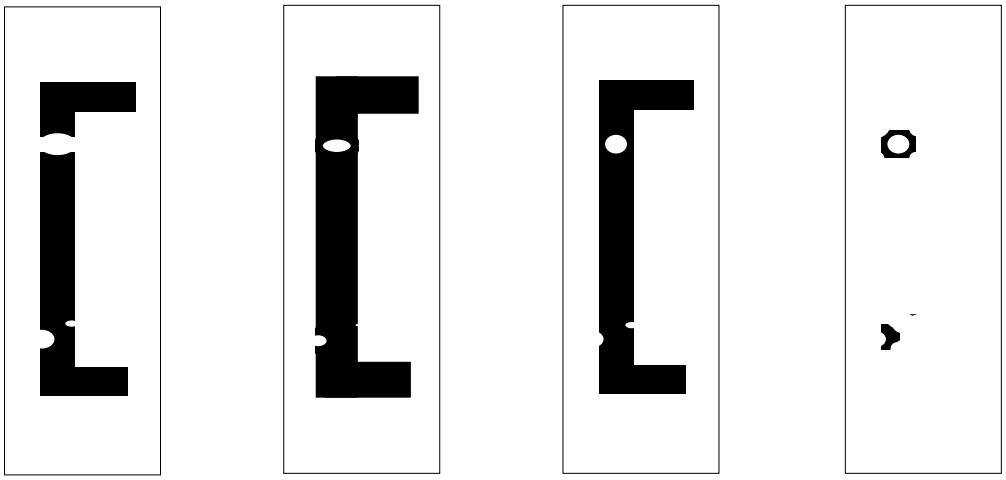



Figure 10: Separating Conductor Surrounding Holes from Other Conductor Traces

3. the original image is EXORed with the image obtained in the previous step, thus obtaining defective patterns as shown in Figure 11(d).



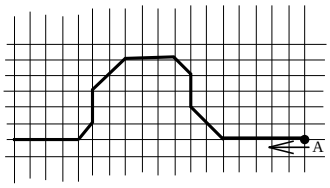
(a) (b) (c) (d)

Figure 11: Verification of Minimum Conductor Spacing

Similar algorithms are presented for verifying MLW and MCTW requirements. Also, a faster algorithm to speed-up the complete process is presented, which makes use of 2-D convolution and table look up operations as a means to implement morphological operations. The main advantage of morphological operations is that they are simple and easy to implement in hardware [15, 60, 64].

#### 4.2.2 Encoding Techniques.

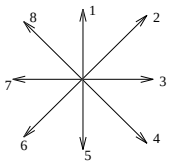
**Boundary Analysis Techniques** Boundary analysis techniques studied are based on the representation of the boundaries in a tractable form, followed by a rule verification procedure. West *et al.* [82, 83] implemented a boundary analysis technique to detect small faults by using Freeman chain coding [84] to describe the boundaries. Small faults are defined as those features that can easily be distinguished from the conductor patterns because of the presence of certain characteristics not normally found on boards. Freeman chain coding translates the boundary of a pattern into a polygonal approximation. This approximation tends to eliminate some digitization and thresholding noise from representation data at the cost of some small features of potential defects. Each line segment in the pattern is one of eight possible vectors of either 1.0 or 1.4142 resolution distances long and at incremental angles of 45 degrees as shown in Figure 12(c). The method works in three stages: (i) It compares the Euclidean distance and the



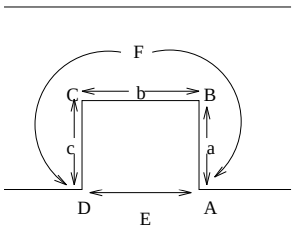

(a) Example of a small fault shape

```
Chain Code: 7777788118777665567777          (a)
Curvature code: 0001010-1-100-10-1011000    (b)
Changes in dir.: 01010-20-10-1020           (c)
Duration:  3 1 1 1 1 2 2 1 1 1 1 2 3        (d)

Extracted corners:

Changes in direction:   2  -2  -2   2       (e)
Duration:  3 2 3 2                          (f)
Distance from A:  4.5 8.0 12.5 16.0         (g)
```

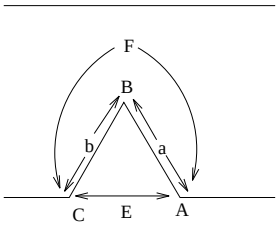
(b) Corner extraction on image in Figure (a)



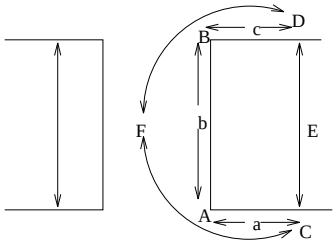

(c) Chain code directions




(1) Nick/Bump




(2) Nick/Bump




(3)Break/Short

(d) Fault shapes detectable by small fault detector

Figure 12: Fault Detection using Chain Coding Technique

boundary distance between two points on the boundary that are a constant number of chain code segments apart. It works on the assumption that, for a normal boundary, the difference will be small, but for a defective boundary the difference will be large. These boundaries which are detected as faulty are passed to the second stage of inspection. In the second stage the corners are extracted from the boundaries, using an iterative corner detection algorithm. This corner detection algorithm makes use of differential chain codes (curvature codes), which eliminate the orientation problems. Initially adjacent curvature codes that have the same sign are combined making the sharp corners more visible in the processed corner data. The changes in direction are defined as the total change in direction over adjacent curvature codes. The duration is defined as the number of curvature codes over which the change in direction occurs. The next step is to group the like signed changes in direction if they are separated by only one zero change in direction. This grouping is continued until no further grouping can be done. Finally all zero changes in direction are eliminated, as this corner combination is sufficient to discriminate different faults, like nicks, bumps, etc, using the sign of the codes. These edge corners on the boundary are processed using three different corner fault models by traversing along the boundaries in a clockwise direction. Lines (a) and (b) in Figure 12(b) are the Freeman chain codes and curvature codes respectively for the image pattern in Figure 12(a). The lines (c) through (g) in Figure 12(b) show the extracted corners with the changes in direction, duration, distance information. The following are example corner fault models for the fault in Figure 12(a).

(1) Four corner fault model:

```
(4.1) Combination + * - * - * +  or  - * + * + * -.
       where (-) is a negative going corner
             (+) is a positive going corner
             (*) is an optional corner of any direction
(4.2) a < 10.0 and b < 7.0 and c < 10.0
(4.3) E < 12.0
(4.4) F - E >  THRESHOLD.
```

(2) Three corner fault model:

```
 (3.1) Detection of corners + * - * +  or  - * + * -.
 (3.2) a < 15.0 and b < 15.0
 (3.3) E < 12.0
 (3.4) F - E < THRESHOLD.
```

(3) Two corner fault model:

```
 (2.1) Detection of corners + * * * * * * * * * * +  or
        - * * * * * * * * * * -.
 (2.2) b < 14.0
 (2.3) E > 7.0 and E < 14.0
 (2.4) F - E > 8.0
```

The sign of the corners is used to discriminate between different kinds of defects, for example, nicks with (+ - - +) and bumps with (- + + -). The "*" indicates that a corner of any sense may

appear between two corners allowing some flexibility in the fault shape. Again the Euclidean distance and the boundary distance between two points on the corner models are calculated for filtering, steps (4.4), (3.4) and (2.4). The processing can be stopped at this stage and good results can be obtained with a THRESHOLD value of 2.3. If processing is continued a value of 1.5 is recommended as a THRESHOLD value. (iii) In stage three the severity of the faults obtained in stage two is calculated. Severity is determined by measuring the minimum track width of a fault and the depth of the fault. The track width is measured along normals to the boundary between the outermost corners of the faults.

**Run-Length Encoding** The run-length encoding technique developed by Thibadeau[39] analyses both vertical and horizontal histograms of run-lengths. The method counts continuous runs of trace pixels along each row and column of the PCB image and constructs a histogram. This histogram reflects very short horizontal runs along a horizontal edge or vertical runs along a vertical edge. Also line-width of the conductors gets reflected in the histogram which is useful to detect flaws. The conductor minimum width requirement is verified by checking if run-length of pixels is shorter than a threshold value. This system was operational at 10 *mil* line panels with a speed performance of 4 megapixels per second. Sterling's run-length encoding method [85, 86] determines the position of the edges of the conductor on each scan line, which provides a convenient way to link the information on a scan line to the previous scan lines. The inspection process involves the tracking of regions from one scan line to other scan line, the extraction of topological features and the detection of anomalies by imposing localized constraints such as minimum and maximum conductor width. The speed performance of the system, operating at 1 *mil* resolution and over boards of 450 $mil \times 600$ *mil*, is about 4 minutes. The main advantage of this technique is that it eliminates the need for precise alignment and enables the process to be implemented in hardware. Although the features extracted need not change for different board styles, it is necessary to change the rules governing the features to be weighted against one another in order to decide whether a real defect has been detected.

## 4.3 Hybrid Inspection Methods

The hybrid flaw-detection techniques increase the efficiency of the system by making use of both referential and design-rule techniques exploiting the strengths and overcoming the weaknesses of each of the methods. These methods have the added advantage that they cover a large variety of defects compared to either referential or non-reference methods alone. For example, most of the design-rule verification methods are limited to verifying minimum conductor trace and land widths, spacing violations, defective annular ring widths, angular errors, spurious copper. Printed circuit board errors which do not violate the design rules are detected by reference comparison methods. These methods can detect missing features or extraneous features like isolated blobs, etc. The design-rule process detects all defects within small and medium sized features; the comparison methods are equally sensitive right up to the largest features. Figure 13 depicts the performance of both these methods based on the size of the features. Hybrid systems make use of both the design-rule methods and comparison methods as they complement each other and therefore achieve 100% error sensitivity, irrespective of feature sizes on the printed circuit boards.

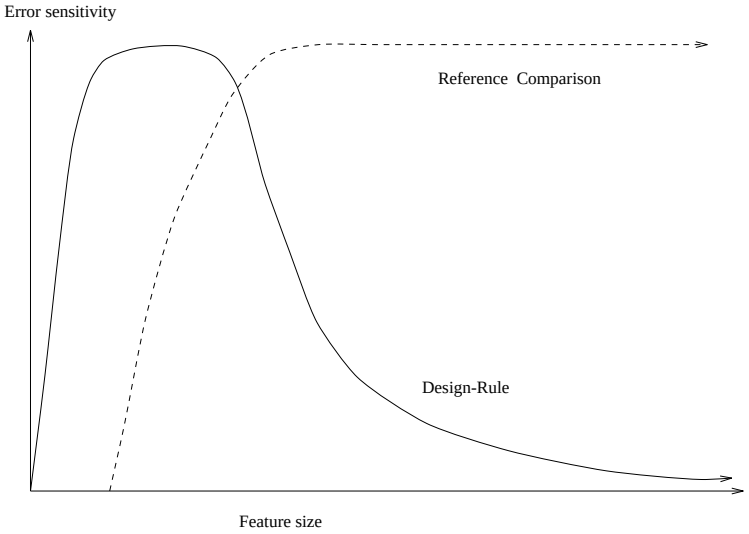



Figure 13: Comparison between Design-Rule and Comparison methods

### 4.3.1 Generic Method.

The generic method is a combination of referential and non-referential inspection algorithms. As Mandeville explains in [64], it is a synthesis of reference-comparison and generic-property approaches. The method does not compare a reference image and the test image pixel-by-pixel, it eliminates the need for the storage requirement, generation, registration, and the comparison of a reference image with the test image. Instead, the method compares a small list of predicted feature types and locations with a list of detected features. This method is a major improvement over design-rule approaches because it can detect missing features and extraneous circuitization that looks like good features. Unlike most design-rule approaches, this method is not limited to verifying just minimum conductor trace width and spacing; it also verifies pads, various trace connections, isolated blobs, holes, etc. Most of the false-alarms that can occur in design-rule approaches are overcome in this technique.

The method makes use of image-to-image transform operations like contraction, thinning, expansion, etc. The observation that the local geometric and global topological correctness of typical circuit features can be inferred from the correctness of skeletal versions of the circuit features in a test image, is used in the analysis of the printed circuit patterns. The method works as follows:

- transform the image to obtain a skeletal image from which defects and good circuit features can easily be detected,
- compare the detected feature list with a design feature list generated from circuit design data, and

- conflicting features imply defects.

The fact that the presence of 0-, 1-, T- and blob-joins is sufficient to infer the existence of typical defects. Figure 14(a) shows these joins: where an *n-join* is a nonzero element with n nonzero 8-neighbors ($0 \leq n \leq 8$); a *T-join* is a 3-join whose 8-neighbors are skeletal elements; a blob-join is a skeletal element with an 8-neighbor that is not a skeletal element. In the Figure 14(a), X is blob-join, s is a skeletal element (a nonzero element necessary to maintain the connectivity of its 8-neighbors), and b is a boundary element (a nonzero element with a zero 8-neighbor). Thinning reduces a connected set of ones in an image to its skeleton, a simplified version of the image with the basic shape. The 4- and 8- thinning operations removes the elements in each iteration with the following constraints: (a) the global connectivity of entities is maintained and the holes are preserved; (b) at each step, 4-thinning removes only elements with a zero 4-neighbor, whereas 8-thinning removes all elements with a zero 8-neighbor. The method can be used in verifying minimum conductor trace width and detecting open circuits, detecting excessive trace width, verifying minimum spacing and detecting short circuits, and verifying pad position, area, shape, and trace-to-pad connections.

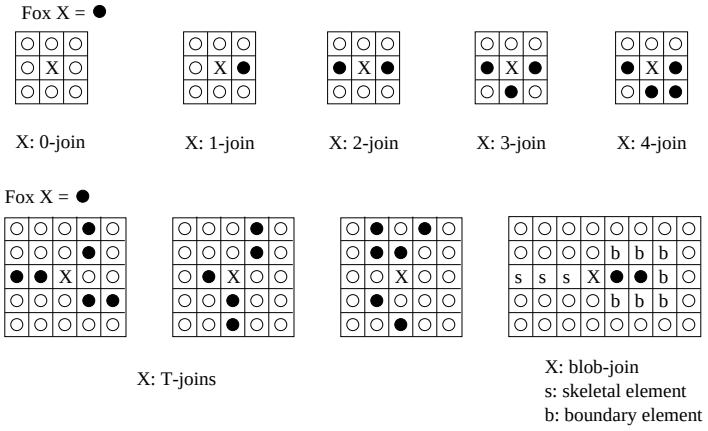
**Algorithm for verifying minimum conductor trace width (MCTW)**: Suppose that $W$ is the nominal trace width and $w$ is the minimum acceptable trace width, less than $W$. The algorithm works on the binary version of the test image as follows:

- alternately 4- and 8-thin the binary image ($\frac{w}{2}$) times. Figure 14(c) depicts the result of applying this operation on the original PCB sub-pattern in Figure 14(b).
- 8-thin ($\frac{W}{2} - \frac{w}{2}$) times the image obtained in previous step. Figure 14(d) depicts the 8-thinned output of Figure 14(c).
- detect 1- and blob-joins in thinned image obtained in previous step.
- compare the detected features in previous step with design list:
  - if 1-joins is not in design list, this implies trace width violations. The square boxes in Figure 14(e) are 1-joins, which implies the presence of defects (open).
  - if 1- and blob-joins in design list are not in detected features, then the image is missing these features.

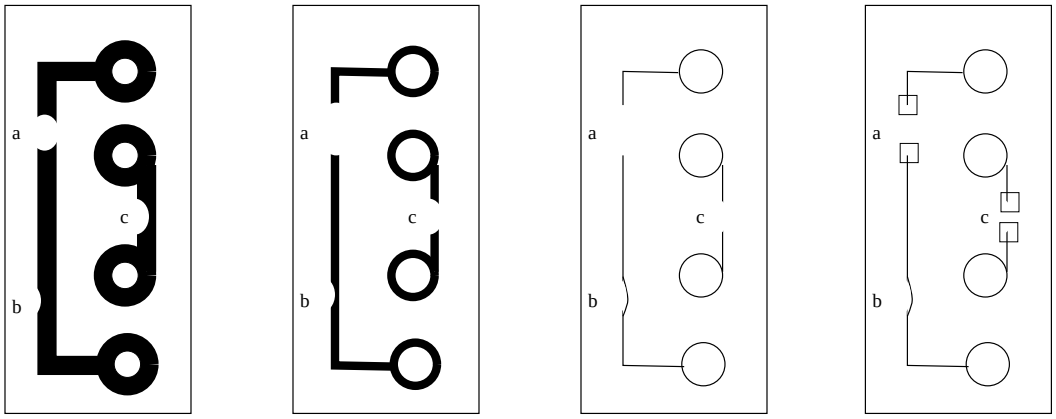
Each of the algorithms presented in the paper use a different thinning process such that a particular class induces a known corresponding class of skeletal features that can easily and reliably be detected. The techniques presented here are amenable to high-speed implementation in pipeline architectures in which each processing element of the pipeline is in charge of the execution of a morphological operation. Mandeville claims that by using 150 element pipeline, the inspection of a panel of 500 $mil \times 600$ $mil$ can be accomplished in 30 seconds at a resolution of 0.5 $mil/pixel$.

### 4.3.2 Pattern Detection using Boundary Analysis.

The inspection system proposed by Benhabib *et al.* [37] uses a hybrid flaw-detection technique based on pattern-detection and boundary-analysis techniques. For conductor flaws, the




(a) n-joins; T-joins and blob-joins




(b) Defective image (c) After contracting n-times (d) After thinning m-times (e) With joins identified

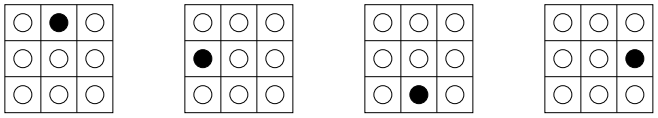
Figure 14: Verification of Minimum Trace Width

boundary-analysis algorithm locates areas that could have potential flaws, these are marked as non-standard edges, which are analyzed by a pattern-detection system to measure conductor widths. Thus this technique significantly increases the speed of the pattern-detection algorithm by isolating the conductor measurements only to those locations that could be flaws. Similarly, a pattern-detection algorithm measures land-widths for hole flaws, after locating the hole centers using an image subtraction technique. Flaw analysis for conductors involves:

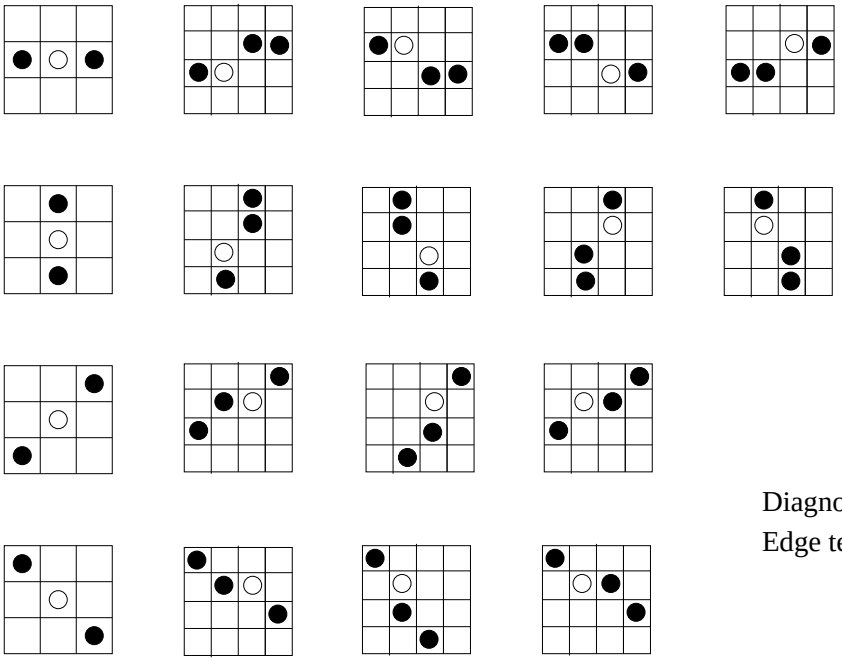
- *Edge detection*: where four edge-pixel templates, shown in Figure 15(a), are used to determine whether the pixels in a window belong to an edge of a conductor in the image.
- *Non-standard edge pixel determination*: where edge-pixels are classified as either standard or non-standard based on a set of horizontal, vertical and diagonal edge-templates, as shown in Figure 15(b). An edge-pixel that does not match any of the templates is considered to be a potential flaw location, hence marked as non-standard.
- *Edge-normal determination*: where three different operators $(T, Y, I)$, shown in Figure 15(c), are used to determine the edge-normals of non-standard conductor edge-pixels. First the T-operator is applied and if each pixel under this operator is classified as substrate, then the edge-normal is in the direction indicated by the operator base. When this operator fails, usually at internal square corners of conductors, the Y-operator is next applied at these locations. When both operators fail, the I-operator is applied.
- *Flaw detection involves*: (i) the non-standard edge-pixel and its counterpart on the opposite edge of the conductor are examined to determine whether they belong to a land or a conductor, (ii) the conductor width is compared with a specified minimum value to determine if there exists a flaw, (iii) the pin-hole size is compared, as a percentage with a specified maximum value to determine if there exists a flaw, (iv) the interconductor spacing is measured by counting substrate pixels in the opposite-normal direction until the first edge-pixel of the next conductor is located. This is compared with a minimum specified value to verify the existence of a flaw, and (v) a conductor-break-detection is performed by tracing from the current non-standard edge-pixel to the opposite edge-pixel along the edge of the conductor. If the trace succeeds within a specified number of edge-pixels, there exists a conductor break.

#### 4.3.3 Circular pattern matching.

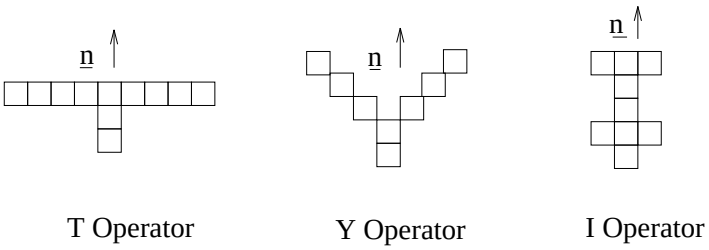
Shiaw-Shian Yu, *et. al.* [11] proposed and implemented a technique based on radial encoding into hardware for high speed inspection of artwork and bare-boards. The basic principle is that an image window of size $32 \times 32$ is moved over the PCB image from left to right and from top to bottom. A template comparator is used to perform the encoding, while the defect detection logic is used to verify the codes to judge if the codes are contradicting. A defect location recorder records the defect locations and total number of defects in that area. The defect detection logic works as follows. To detect if a trace width is as small as width $d$, a circle with $d$ is drawn, with the center of the circle on the trace edge. If the circle is divided into two areas, then it is a normal trace; otherwise, the trace width is smaller than $d$ or certain other defects exists. Figure 16(a) shows a trace width smaller than $d$. Figure 16(b)-(d) show the ability of this method to



(a) Edge pixel templates




(b) Edge templates




(c) Edge normal determination operators

Figure 15: Templates Used in the Pattern Detection

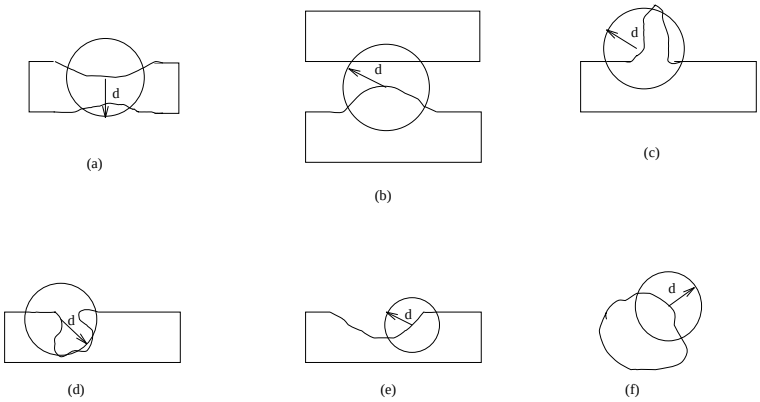



Figure 16: Defect detection using Template T2

diagnose other defects. This method is not sensitive to trace direction, but defects like Figure 16(e)-(f) cannot be discovered.

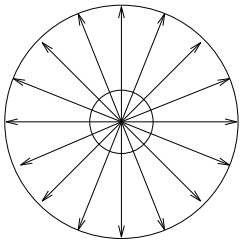


Figure 17: 16 Extension directions

To diagnose open circuits or short circuits, the extensibility of the line or substrate is inspected. Since the lines must end at the solder pads, which are greater in size than the line width, the lines in local areas, must maintain good extensibility. Figure 17 shows the directions of extension, altogether 16, each divided by an angle of 22.5 degrees. The small concentric circle in the middle is used to prevent inspecting the line edges and making incorrect extractions. The extensibility criteria is that all pixels within a distance $r$, from the center of the circle in that direction, have the same color. Figure 18(a)-(c) show lines that satisfy extensibility. Figure 18(d) is an open circuit, Figure 18(e) is a short circuit, both of which do not satisfy extensibility. It should be noted that the method relies on the judicious selection of the value $r$.

Templates T1 through T5 shown in Figure 19, are used as basic templates for analyzing the pixels on circle perimeters and line segments. The method assumes that the standard line width is 10 pixels. For example T1, T2, T3, T4 and T5 templates are used as follows:

- T1 is used to decide weather the present windows center is at a point on the edge. The

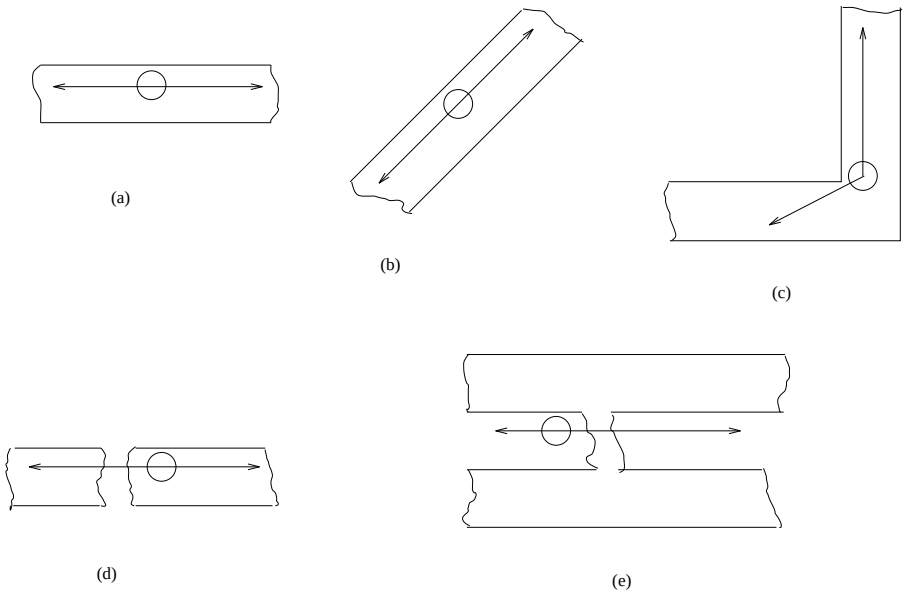



Figure 18: Extensibility test on a Conductor trace or Substrate

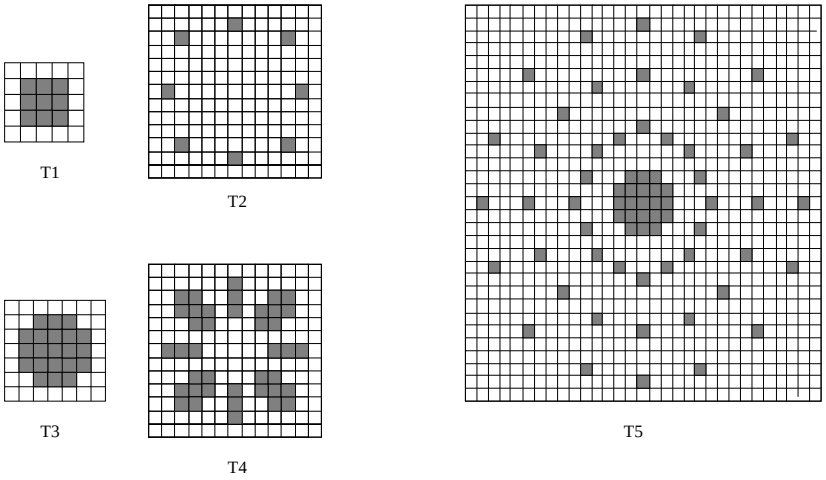



Figure 19: Templates used in the pattern matching

edge point means it is on conductor and its neighboring 8 pixels are divided into two regions.

- When the window center is located on the edge, T2 is used to check for a situation where the line width is smaller than 6 pixels and the line spacing is smaller than 5 pixels. It is also used to diagnose pin holes, copper specks, mouse bites, extrusions and other defects.
- T3 is used to check if the colors of pixels in the window are the same. T3 along with template T2 is used to inspect the lines or spacings of width smaller than 10 pixels. This can also diagnose pin holes and copper specks.
- After T3 has been used to check the line widths and line spacings to be smaller than 10 pixels, T4 is used to measure the actual line width or spacing.
- T5 is used to measure extensibility. To satisfy extensibility in a certain direction, all the pixels within a certain distance, from the center of the template T5, are checked for pixels of the same color. The small circle in the middle of the template T5 is used to prevent inspecting the line edges and making incorrect extensions.

The system detects open and short circuits, pin holes, overetch and underetch of the conductor patterns. It performs at a speed of $4 \times 10^6$ pixels/second at 0.5 *mil* resolution.

#### 4.3.4 Learning methods.

**Radial matching algorithm** The FVIS-110 system developed by Fujitsu [15, 32, 87] uses a radial code self-learning method. In this method the users input learning sample patterns from good PCB boards, and the system converts these patterns to characteristic features known as radial codes. Radial codes assume three concentric circles around the center of the PCB patterns; codes for the locations of the edges of each sub-pattern depend on which circular domain it falls within each of eight directions as shown in Figure 20. The pattern lengths are measured radially in four directions, 45 degrees apart. Each measuring line has a pair of sensors that measure the distance from the center to the pattern edges. The output of each sensor pair is then checked for equivalent lengths. The pattern center is defined where the number of equivalent sensor pairs exceed the predetermined number. The length is divided into four areas by the minimum width, the maximum width, and length of the measuring sensor. The system assigns codes consisting of S (shorter), C (correct), L (longer) and OV (over) for each point on the line. OV indicates the direction of the pattern line. The pattern width is perpendicular to the direction. When the pattern is normal, the width is within the C area. For example, for the line pattern in Figure 20(a), the 0-degree measurement is C, 45-degree measurement is L, 90-degree measurement is OV, and 135-degree measurement again is L. The radial code is (C, L, OV, L), and all of the sensor pairs have an equivalent length from the center.

Figure 20 shows the detection of short in a PCB sub-pattern. For a normal pattern the radial code is (C, L, OV, L). But if there is a short as shown in Figure 20(b), the 0-degree length is

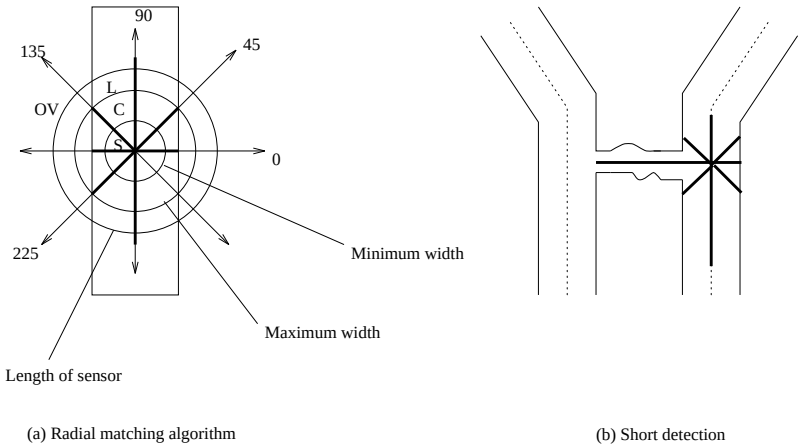



Figure 20: Radial matching algorithm (a) Perfect pattern (b) Short detection

OV, and the code changes to (OV, L, OV, L). These defective codes will be detected at many points, because inspection is performed at every center pixel. The system counts and memorizes the frequency with which each code occurs. Because the system assumes that defects tend to occur less frequently than correct points, it judges the items that occur infrequently as defects. Therefore, if the frequency of occurrence exceeds a set value, the product is good; if the frequency is greater than one and less than the set value, the system displays the components corresponding to the code as potentially defective points, asking the operator to determine whether or not the items are defective. Figure 21 shows how a partial open is detected by this method. The system detects open and short circuits, spur, narrow traces, and poor spacing between conductors. It performs at a speed of $40 \times 10^6$ pixels/second at 0.2 *mil* resolution.

**Shape comparison method** In the Ai-1029 system [32], Nikon employed a pattern comparison method based on automatic learning procedures. Figure 22 shows the steps involved in the training and testing of the system for fault identification. First the user inputs a learning sample and the system breaks the input image into small segments. Then it stores small patterns from each segment in a reference file. Next, the system repeats this process with the subject board, dividing the input image into small patterns with those in the reference files. If the subject board does not exhibit patterns that match those in the reference files, the system judges the product as defective. In this system, the allowance for pattern variation are the keys to accurate evaluation.

# 5 Commercial Systems

In order to make this survey complete, this section briefly surveys some of the currently available commercial PCB inspection systems. Many factors must be considered in designing a commercial inspection system: hardware, software, system throughput, versatility, and reliability. Versatility refers to the number of different inspections the system can perform. Some of the commercial

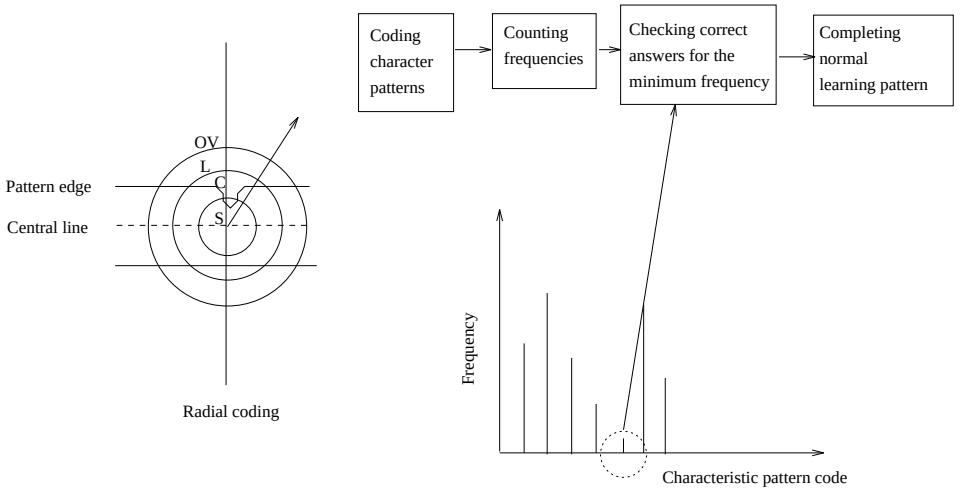



Figure 21: Fujitsu radial code self-learning method

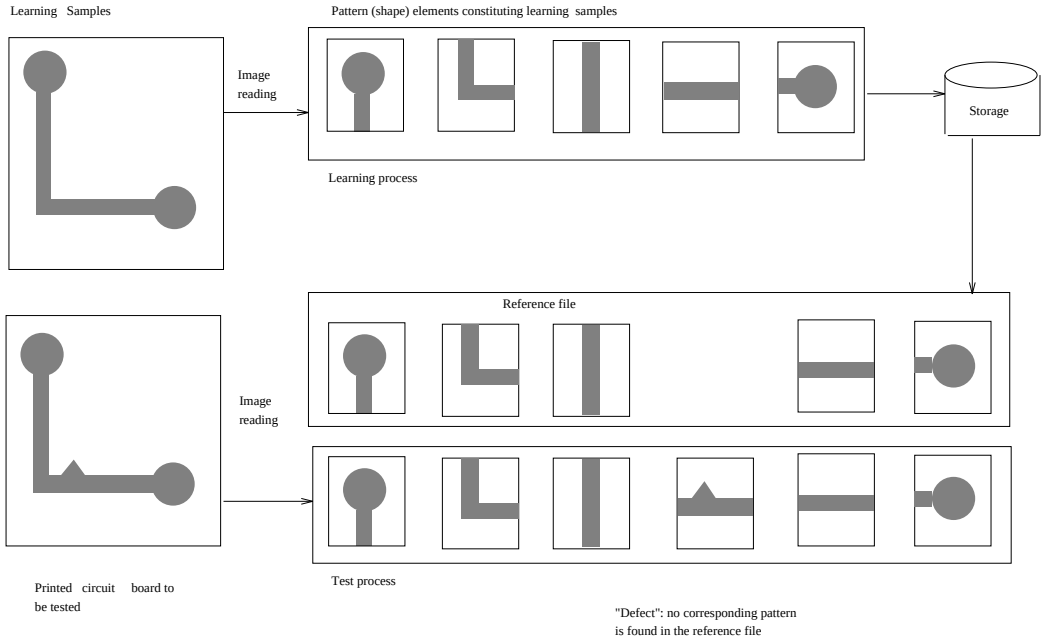



Figure 22: Nikon's shape comparison method

systems run the gamut from inspecting holes and measuring dimensions to inspecting complete bare-boards. Some can make exact measurement of board features or perform inspection in-line with the production process. For manufacturing, the most complete (and most expensive) systems can execute all these functions. The following is a list of capabilities and features a typical commercial PCB inspection system is expected to have:

- System capability:
  - Minimum flaw that can be repeatedly detected at the stated escape rate:- *2.0 mil.*
  - Scan rate:- *4.0 $ft^2$ / min.*
  - Panel through-put:- *inspect both sides of* $18 \times 24$ *inch panel (85% active) including setup, loading, scanning, and unloading at a rate of 40 panels/hour.*
  - Typical pixel size:- *1.0 mil.*
  - False alarm rate (fail good product):- *less than 2.0 per $ft^2$.*
  - Escape rate (pass bad product):- *less than 1.0 per 100 $ft^2$ (depends on defect criteria)* .
  - Gaging capability (where specified):- *measure feature size to $\pm$ 1.0 mil.*
- Typical dimensions of panels to be inspected:
  - Panel dimension:- 20" $\times$ 26".
  - Scan area:- 18" $\times$ 24".
  - Nominal conductor width:- *4 mil.*
  - Nominal conductor spacing:- *4 mil.*
  - Pad size:- *round or rectangular pads of dimension between 3 and 10 mil.*
  - Conductor via hole diameter size:- *5 mil or larger.*
- Types of panel to be inspected:
  - Conductor layout:- *all possible line orientations and power/ground layers.*
  - Photoprinted boards:- *all commercial photoresist types.*
  - Innerlayer metalization:- *drilled and undrilled PCBs in copper technology.*
  - Artwork:- *most forms including silver-halide and diazo on both mylar and glass substrate.*
  - Finished boards:- *without solder and prior to solder mask*
  - Substrates:- *FR4, polymide and other common substrate material*
- Types of defects to be inspected:
  - Voids:- *any void in a conductor that exposes bare substrate material and exceeds 5 % of the design width.*
  - Shorts:- *Any short with a width in access of 2 mil at any point*
  - Opens:- *Any conductor open exceeding 2 mils in width*

- Spacing:- *Any metalization that reduces the space between conductor by more than 5 % of design spacing*
- Extraneous metal:- *Any isolated spot whose area exceeds 2 mil*$^2$
- Artwork:- *Any defect violating the above rules for voids, spacing, or extraneous metal; as well as any pinhole in excess of 3 mil*

Table 1 presents a list of commercial PCB inspection systems currently available. The quoted throughputs in the table are estimated and may vary upon various inspection factors. It can be observed that most machines use the hybrid inspection techniques - design-rule checking and comparison methods jointly. These systems can inspect more items with greater accuracy than before. To improve image quality, makers applied different kinds of illumination from reflected light, transmitted light and fluorescent light from multiple light sources. Processing speeds continue to accelerate and some makers now adopt multi processing systems. AOI System Corp. developed the AOI-20 product, which employs as many as 20 CCD cameras and performs parallel processing. Even a slow system with a 1 *mil* resolution attains a processing speed of 6.00 $ft^2/min$; fast systems reach 33.33 $ft^2/min$. Converting this value to a pre-pixel speed reveals an astonishing speed of 10 $ns/pixel$. With progress in diminishing pattern thickness, developers improved resolution. The 1 *mil* resolution of the early days now has reached 0.2 *mil*. In addition to handling inspection processes, these systems now display defective locations, components, incorporate correction machines and accommodates computer-integrated manufacturing (CIM).

## 6 Summary

With the advances made over the last decade, machine vision may answer the manufacturing industry's need to improve product quality and increase productivity. This study presented a survey of algorithms for visual inspection of printed circuit boards. A classification tree of the algorithms is presented. The classification divides the techniques into three basic classes: *reference comparison* in which production boards are compared with a database or golden board patterns, *design rule checking* provides for making measurements that are checked against predetermined quality rules, *hybrid techniques* combine both in selectively performing pattern matches as well as design-rule measurements.

The major limitation of all the existing inspection systems is that all the algorithms need a special hardware platform in order to achieve the desired real-time speeds, which make the systems extremely expensive. Any improvements in speeding up the computation process algorithmically could reduce the cost of these systems drastically. However, they remain as a better option when deciding between increasingly error prone and slow manual inspection and higher productivity. Another major problem in automated inspection system design is the development of algorithms that will provide the sensitivity needed to find faults while ignoring 'noise' caused by acceptable imperfections. This problem becomes more difficult because the acceptability of an imperfection is a objective decision and will vary among different manufacturers. Also, forefront in the challenges confronting the automated visual inspection research is the development of generic inspection equipment, hardware and software, capable of handling a wide variety of inspection tasks. Many efforts are underway to improve flexibility in the field of visual inspection systems. Systems in the future will be easier to operate than those now available.

Table I. Commercially Available Bare PCB Inspection Systems

| System | Inspecion Methods | Image System | Resolution | Scan Rate | Features/Benefits |
|---|---|---|---|---|---|
| AOI System AOI-20 | Design Rule Checking (8 kinds of detection sensors) and Comparison method | 20 CCD Cameras Reflection/Transmission lighting | 1 mil | 6.00 sq. ft/min | Continuous operation is possible through the use of conveyor system |
| Mania MOP-5002 | Simultaneous use of Design Rule Checking and Image Comparison | Two CCD Cameras Halogen Lamp Lighting | 1 mil | 6.00 sq. ft/min | Menu driven user friendly software for easy and fast setup. Fast unit under test change over using patented vacuum adaptor system |
| Dai-Nippon Screen OPI-5220 | Design Rule Checking and Comparison method | LED light, CCD line sensor Reflection/Transmission lighting | 1 mil | 19.20 sq. ft/min | Complete Comparison Inspection Inspection function of product with special shape |
| Shin-Nippon Steel PT-2130 | Design Rule Checking and Comparison method | Halogen Lamp, Multi-Directional illumination Speedy CCD Camera | 1 mil | 33.33 sq. ft/min | Continuous Variable Resolution (0.2 to 1mil) Fastest Speed |
| Orbotech PC-1411 | Design Rule Checking and Comparison method (Golden Board or CAD download) | Reflective and Diffusive Omni lighting | Fixed resolution 0.5 mil | 18'' x 24 '' panels 45 sides / hour | Low cost startup, On-line verification |
| Orbotech PC-1450 | Design Rule Checking and Comparison method (Golden Board or CAD download) | Reflective and Diffusive Omni lighting | Variable resolution 0.25 - 0.9 mil | 18'' x 24 '' panels 38 - 160 sides / hour | 3 - 10 mil line width technology |
| Orbotech PC-1490 | Design Rule Checking and Comparison method (Golden Board or CAD download) | Reflective and Diffusive Omni lighting | Variable resolution 0.20 - 0.5 mil | 18'' x 24 '' panels 45 - 130 sides / hour | 3 - 6 mil line width technology for high volume PCB shops |
| Orbotech V-309i/x | Design Rule Checking and Comparison method (Golden Board or CAD download) | Fluorescent technology (Blue Laser) | Variable resolution 0.4 - 1.0 mil | 18'' x 24 '' panels 77 - 180 sides / hour | 3 - 10 mil line width technology for high volume PCB shops |
| Orbotech Vision Blaser | Design Rule Checking and Comparison method (Golden Board or CAD download) | Fluorescent technology (Blue Laser) | Variable resolution 0.25 - 0.5 mil | 12'' x 12 '' panels 80 - 180 sides / hour | 2 - 4 mil line width technology for high volume PCB shops |

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