

DFT for Digital Detection of Analog Parametric Faults in SC Filters

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Abstract—Parametric faults are a significant cause of incorrect operation in analog circuits. Many design for test techniques for analog circuits are ineffective at detecting multiple parametric faults because either their accuracy is poor, or the circuit is not tested in the configuration in which it is used. We present a design for test (DFT) scheme that offers the accuracy needed to test high-quality circuits. The DFT scheme is based on a circuit that digitally measures the ratio of a pair of capacitors. The circuit is used to characterize the transfer function of a switched capacitor circuit, which is usually determined by capacitor ratios. In our DFT scheme, capacitor ratios can be measured to within 0.01% accuracy and filter parameters can be shown to be satisfied to within 0.1% accuracy. With this characterization process, a filter can be directly shown to satisfy all specifications that depend on capacitor ratios. We believe the accuracy of our approach is at least an order of magnitude greater than that offered by any other DFT scheme reported in the literature.

I. INTRODUCTION

ON-CHIP design for test design for test (DFT) techniques have been suggested as one method to reduce test costs in analog and mixed-signal circuits [1]–[11]. A test process is judged by its cost and the quality of the product that passes the test process. Many DFT techniques suggested in the literature for analog circuits have been shown to be effective at detecting locally catastrophic faults. That is, faults which cause significant variations in the value of a single component. The validation has been both through circuit simulation and through the fabrication of test integrated circuits (IC's) with artificial fault injection.

In analog circuits, parametric or “soft” faults, that is minor component value variations, are as important as catastrophic faults. Parametric faults occur due to normal variations in the manufacturing process and cause the values of one or more circuit component to deviate from their expected values [12]–[14]. For minor single component deviations, the deviation in the output from its expected value (caused by the component variation) may be acceptable. Thus, only large single component deviations may cause output errors. It is possible that a collection of minor variations in multiple components may cumulatively cause the output to be erroneous. Unfortunately, not every possible set of variations is guaranteed to cause an output error. Not every multiple-component variation is a multiple parametric fault. Only those multiple deviations that actually cause output errors are parametric or soft faults. To further complicate matters, errors in the outputs are defined

by circuit specifications. A multiple-component variation that corresponds to a fault in one application may result in acceptable variations for another application. Since the number of potential parametric faults is infinite, the fault coverage for multiple parametric faults cannot be judged by fabricating a small number of IC's, or by simulating a small number of faults. To be considered as being effective, a test process has to offer high coverage for parametric faults. Conversely, in achieving this high fault coverage, the test process should not result in an inadvertent yield loss. The test process should not erroneously fail many fault-free circuits. A high yield loss will result in an unacceptable increase in test costs.

1) *Contributions:* Studies of the ability of DFT schemes to detect parametric faults have been very limited. With a statistical analysis tool, we show that most DFT schemes reported in the literature cannot offer an adequate coverage of multiple parametric faults. We demonstrate that adequate fault coverage can only be guaranteed with high accuracy signal measurement. We present a DFT scheme for switched-capacitor circuits that realizes the required high measurement accuracy. We develop a circuit, an *analog-to-digital capacitor ratio converter (ADCRC)* which given two capacitors C_1 and C_2 produces a digital estimate of the ratio C_1/C_2 . The accuracy of the digital estimate can be as high as 15 bits. In other words, the ratio can be estimated to an accuracy better than 0.01%. The functionality of a switched-capacitor filter is determined primarily by a number of capacitor ratios. The ADCRC circuit can be used to accurately compute *all* the capacitor ratios that determine the transfer function of the filter. The DFT scheme can characterize the functionality of the filter to an accuracy greater than 0.1% and consequently determine if the filter that has been realized satisfies the specifications that depend on capacitor ratios. In general, a majority of a filter's specifications depend on capacitor ratios. This approach offers a number of advantages.

- Each ratio is measured on-chip in the digital domain, with an accuracy at least an order of magnitude greater than that reported by previous on-chip test techniques.
- Functional test techniques can be used to directly verify that a circuit meets all of its specifications. Assume that a test process directly verifies only a subset of the functional specifications. In the absence of reliable system models, the results with this subset of tests cannot be used to deduce the ability of the system to meet the specifications that have not been directly verified. By characterizing the transfer function, we verify most specifications.
- The technique can be implemented in manner that is consistent with the design practices used for switched capacitor analog circuits and without a significant impact on circuit performance.

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II. PREVIOUS WORK

Many DFT schemes for analog circuits are extensions of techniques developed for digital circuits. They aim to reduce test generation difficulties and improve fault coverage. However, the test difficulties experienced with analog and mixed-signal circuits are significantly different from those experienced with digital circuits. For example, accurate signal measurement is far more difficult in analog circuits [1]. Thus, many DFT schemes exploit characteristics unique to analog circuits, such as regularity in circuit structure and/or relationships between on-chip signals, and target test problems unique to analog circuits. They are generally limited in their application to specific circuit macros such as data converters or filters. All DFT schemes require the addition of hardware for switching circuitry and functional elements. Macro-specific DFT techniques reported in the literature generally fall into one of the following categories:

1) *Reconfiguration for test*: Reconfiguration-based test methods require the addition of a switching network and the creation of a test mode in which the circuit is reconfigurable [2]–[5]. Reconfiguration has been used to improve testability in analog and mixed-signal circuits in two ways. We refer to one approach as reconfiguration for access. The basic approach is similar to one used for digital circuits. The circuit to be tested is partitioned into several blocks such that the inputs to and the outputs from each block can be directly controlled and observed. Reconfiguration simply increases access to the circuit components, without altering them. However, doing so without altering functionality is more difficult in analog circuits than in digital circuits. The details of the application of reconfiguration for access are circuit specific.

The second type of reconfiguration-based DFT technique is an indirect approach to testing that is unique to analog circuits. We refer to this technique as reconfiguration for redesign. Reconfiguration is used to rearrange the components to form an easily testable circuit. The response of the altered circuit, in its easily testable configuration, is used as a guide to determine if the original circuit, in its normal configuration, will work. Unlike circuit-specific reconfiguration for access techniques, almost all the reconfiguration for redesign techniques discussed in the literature have been macro-specific [2]–[5].

2) *Code-based test*: This approach is based on methods used to design on-line error detection schemes for fault-tolerant digital systems [7][8]–[11]. Code-based techniques target the difficulty encountered in measuring the values of on-chip signals. A redundant data code is used to encode on-chip data. On-chip code checkers, rather than off-chip instrumentation, are used to verify that the data code is not corrupted. Faults are detected indirectly in that those that corrupt the code are the only ones that are flagged by the checkers. To limit the number of faults that escape detection and to obtain a high fault coverage, the circuit can be redesigned to improve the number of faults that corrupt the data code. The code used most commonly is the data duplication code.

3) *Directly Relevant Research*: Two previous efforts are directly relevant to the DFT scheme developed in this paper. The reconfiguration for redesign technique in [5] measures individual

capacitor ratios to characterize the quality of a realized filter. It is based on the fact that the functionality of switched-capacitor circuits is largely determined by various capacitor ratios. Given a circuit to be tested, the capacitor ratios that determine its functionality are identified. The procedure to identify these ratios is circuit specific. Capacitor ratios are measured by configuring the pair of capacitors whose ratio is to be measured as a voltage divider. The power supply voltage is used as the input voltage to the voltage divider. The area overhead required for the technique was not discussed. However, this interesting technique suffers from four significant limitations.

- The variations in the supply voltage, which can be as high as 5%, limit the accuracy with which ratios can be measured.
- Reduced accuracy in ratio measurement results in looser bounds on the filter specifications and limits the method's utility.
- Fast accurate off-chip measurement techniques are needed to accurately measure the output of the voltage divider.
- The technique as implemented requires the addition of switches in the normal signal path which may affect performance.

A functional self-test technique based on using digital circuitry to generate functional test signals has been extensively investigated [19]. Tone inputs are digitally generated and the outputs of the circuit under test are digitized (if necessary). As many tones as are needed for functional test are generated. This technique also achieves substantial accuracy by moving analog signal measurement to the digital domain. As mentioned before, one limitation of functional test is that the test process is complete only if all the specifications of interest have been directly verified. In the absence of suitable models, one cannot make general deductions about the ability of a circuit to satisfy all its functional specifications by testing for only a few of them. The overhead of functional self-test will increase in proportion to the number of tests applied. Area estimates for individual components such as tone generators have been published. However, an estimate of the total overhead for a complete implementation has not been presented.

III. DFT SCHEME ANALYSIS

In this section, we examine the ability of the DFT techniques reported in the literature to detect multiple parametric faults. First, we discuss the impact of process variations on circuit elements and outputs.

A. Process Variations

With any process, the actual realized values of circuit components will differ from their expected or the desired values. Across several IC's, for the same design, the realized values will typically be both greater than and less than the expected nominal values. Process statistics can be used to estimate the expected range of variation in the value of each on-chip component. Random variables are commonly used to represent and analyze the impact of process variations. As do others, we use Gaussian distributions [17] to model the impact of process variations on component values.

1) *Components*: In IC's, though the absolute values of on-chip components can vary significantly from their expected values, relative matching between components is high [14], [15]. Thus, most analog IC's use the relative matching between physically similar components to set circuit parameters. When ratios are used to set transfer functions, output parameters are immune (as a first order approximation) to shifts in the mean values of components. Only relative shifts between components are of importance. Correspondingly, for our purposes, we will only model relative shifts in component values. On-chip components will be modeled by Gaussian variables centered around a fixed mean. The statistics of the distribution are determined by the fabrication process.

2) *Outputs*: In general, the output of an analog circuit is a nonlinear function of the component values. It would appear to be difficult to compute the output distribution from the component distributions. However, because the component variations of interest are small, at a given test point, the transfer function with respect to component values can be linearized using sensitivity analysis [16]. The linear sum of several Gaussian distributions is also a Gaussian distribution [15]. Thus, about each test point the variations in the output value can also be modeled as a Gaussian distribution. Without the loss of any generality, the mean of the distribution can be assumed to be zero.

3) *Signal Tolerances*: The value of an analog signal cannot be measured with complete precision. Hence, at each test point, a range of output values is defined as being acceptable. The output tolerance D_o is the accepted variation in the output at a test point. The output tolerance is defined by the specifications, measurement tolerances and the expected impact of process variations. We are only interested in the *differences* in the output from the expected value. The nominal value can be ignored without the loss of any generality. The output tolerance will be circuit and test-point specific. Thus, the value of signal x_1 is acceptable if $-D_o < x_1 < D_o$. Similar tolerances will have to be allowed in test points in a circuit reconfigured for redesign and in code checkers used to monitor on-chip signals.

B. Performance Metrics

Probabilistic or statistical analysis is the only practical method to assess the parametric fault coverage of a test process. In this section, we define some terms to enable us to quantify values of interest for such an analysis. A good IC is one for which all outputs are at their expected values within tolerances. Let P_G be the probability of manufacturing a good IC. $P_B = 1 - P_G$ is the probability of manufacturing a faulty IC. An ideal test process will pass all good IC's and fail all bad IC's. Some, but not all, of the following terms, or terms similar to those listed below, have been previously defined [14].

An ideal test process should fail all faulty units and pass all good units. In a real test process, some good units will fail the test, and some faulty units will pass the test. The following terms categorize good and faulty units with respect to their performance on the test process:

- 1) $P_{GP}(P_{GF})$ is the probability that a good IC will pass(fail) the test;

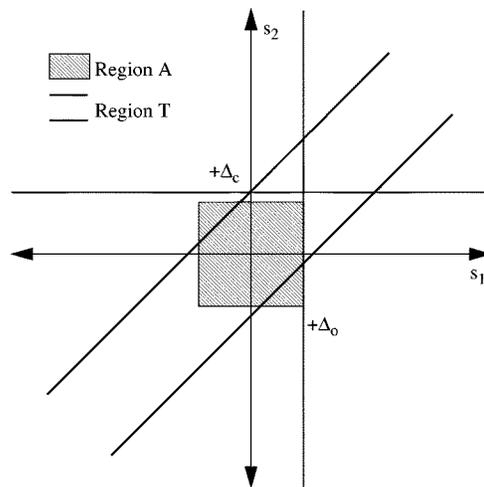


Fig. 1. Code-based DFT analysis.

- 2) $P_{BP}(P_{BF})$ is the probability that a bad IC will pass(fail) the test.

The fault coverage of the test process is $F = (P_{BF}/P_B)$. The yield is $Y = (P_{GP}/P_G)$. The confidence-level is the probability that a unit passed by the test process is good. The confidence level is $C = (P_{GP}/P_{GP} + P_{BP})$.

C. Fault Coverage Estimation

The goal of test is to cost-effectively improve a user's confidence in the shipped product. To assess the quality of the test process, we will have to compute the fault coverage and the yield. The primary costs of achieving the improvement are the costs of applying the tests and a drop in the yield. Ideally, we would like to maximize fault coverage and yield simultaneously. That is, we would like to discard all defective units while passing all defect-free units. Our analysis will demonstrate that this is usually not possible with most of the DFT schemes reported in the literature.

1) *Model-based Analysis*: The models developed below represent essential characteristics of simple, but representative, reconfiguration-based and code-based DFT schemes. They are not meant to represent all code- and reconfiguration-based DFT schemes in exact detail. However, as we show, even these simple models can provide substantial insight [1]. In what follows, recall that at each operating point, small changes in the output can be expressed as linear functions of component values.

a) *Code-based DFT*: Our model for code-based DFT is based on the most common code, data duplication. This model can be extended to other codes without significant difficulty. Assume that the duplication code is employed at the circuit outputs. Let s_1 and s_2 be the two signal outputs that are being compared. Typically, the two signals are produced by nearly-identical hardware which is completely or partially disjoint. Refer to the entire $s_1 s_2$ -plane shown in Fig. 1 as U. The plane represents the range of possible variations in the two signals. Since both signals are produced by the same hardware and are of the same tolerance they both have the same range of variations. Output values further away from the origin are less likely to occur than those closer to the origin.

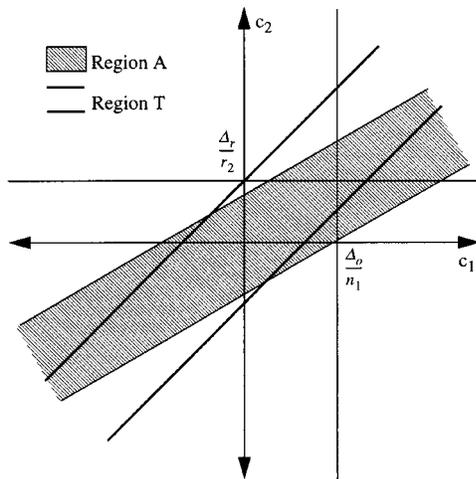


Fig. 2. Reconfiguration-based DFT analysis.

The circuit is acceptable only if both the outputs are at their expected values. Since the value of an analog signal cannot be defined or measured with complete precision, output values that are close to the expected values are also acceptable. The acceptable tolerance D_o in the output is defined by the specifications and process variations. This relationship is represented by the striped region inside the square in Fig. 1. Any parametric deviations that cause both the outputs to be in this region are not parametric faults since they do not cause output errors. Refer to this area as region A. The on-chip checker is triggered if the two signals being compared are not equal. Again, since the signals are analog, an exact comparison is not practically feasible. The checkers will only trigger if the difference is greater than a tolerance D_c defined by the test process and process variations. This relationship is represented by the area between the solid dark lines in Fig. 1. Refer to this area as region T. Any parametric variations which cause the outputs to be in this region, including those that correspond to faults, will not trigger the checker.

b) Reconfiguration-based DFT: A similar modeling technique can be used for reconfiguration-based DFT. Consider a circuit with two components c_1 and c_2 operated in one configuration and reconfigured during test. Refer to the entire c_1c_2 -plane, represented in Fig. 2, as U. Component values further away from the origin are less likely to occur than those close to the origin. Consider two test points, a *specification* test point in the original circuit and an *actual* test point in the reconfigured circuit. At each test point, the output o is a linear function of the two components of the form $o = k_1c_1 + k_2c_2$. However, the coefficient values at the test points for the original and reconfigured circuits will be different.

The *specification* test point determines whether the circuit is good or bad. The specifications, typically on circuit outputs, have a tolerance D_o defined by process variations and specifications. The acceptable range of linear functions is represented by the striped region in Fig. 2. Refer to this area as region A. Any set of parameter deviations that cause the outputs to lie in the striped region are not parametric faults. The *actual* test point determines whether the circuit passes or fails the test process.

The test will have a tolerance D_r , defined by process variations and the test process. The range of linear functions for which the circuit will pass the test is represented by the area between the solid dark lines in Fig. 2. Refer to this area as region T. Any parametric variations, including those corresponding to faults, which cause the output to lie in this region will pass the test process.

c) Analysis: The information in Figs. 1 and 2 demonstrates that with both types of DFT schemes, a test process may not function as desired. In the two figures, one may observe the following.

- A portion of the unstriped region lies outside the solid lines. This region corresponds to the set of faulty circuits which fail the test.
- A portion of the striped region lies within the solid lines. This region corresponds to the set of good circuits which pass the test.

These two outcomes are the only desirable ones. They correspond to the fault coverage and the yield of the test process respectively. However, the figures show that it is probable that the test process will have two more undesirable outcomes.

- A portion of the striped region lies outside the solid lines. This region corresponds to the set of good circuits which fail the test.
- A portion of the unstriped region lies between the solid lines. This region corresponds to the set of faulty circuits which pass the test.

The quality of the test process is determined by the probability of each of these events occurring. Event probabilities can be computed by integrating the probability density functions of the distribution of component and signal values over the appropriate regions. Recall that component and output variations can be modeled with the normal distribution. That is, smaller deviations in component or output values are more likely to occur than larger deviations. However, undesirable outcomes will still occur with a significant nonzero probability. The computation, through symbolic or numeric integration, even when the probability density function is modeled with the Normal distribution, is possible only for simple structures.

2) Simulation-Based Estimation: Large complex circuits require empirical analysis. Monte-Carlo simulation is commonly used to estimate the impact of random variations. In a Monte-Carlo analysis scheme, the target circuit is simulated a large number of times using a standard circuit simulator. Each component is modeled by a random variable. Process statistics are used to estimate the range of likely variations in component values for each of the components in the circuit. The pattern of variations is determined by the distribution, such as the Normal distribution, used to model the variation. On each iteration, the circuit is simulated with a different set of component values. The simulation is used to determine circuit quality and the result of the test process. That is, whether the circuit (realized in that iteration) is good or bad and whether it passes or fails the test process. Circuit quality is determined by the thresholds on the specifications. The pass/fail result is determined by the thresholds on the test process. The results of the simulation are used to estimate the fault coverage and the yield. We have developed a

TABLE I
PERFORMANCE COMPARISON

DFT Test Method	Authors	Type of circuit	Yield	Fault Coverage
Code-based	Direct duplication [11]	2nd order lowpass filter	0.916	0.566
	Pseudoduplication [9]	Lossy integrator	0.900	0.209
	Fully differential [6]	2nd order low pass filter	0.918	0.081
	Checksum coding [10]	2nd order low pass filter	0.900	0.350
Reconfiguration-based	TF re-evaluation [8]	2nd order low pass filter	0.911	0.659
	Signal propagation [7]	3rd order low pass	0.918	0.121
	Oscillation [2]	2nd order low pass filter	1.000	0.62

parametric fault-effect analysis tool (pFEAT) for switched-capacitor circuits. The pFEAT tool uses SWITCAP as the core circuit simulator. Our tool can be used to simulate the impact of process variations on the passive components, and estimate their consequent impact on circuit functionality. The tool can be used to evaluate both code-based and reconfiguration-based DFT schemes.

Statistical experiments using pFEAT were conducted for a wide range of analog DFT schemes reported in the literature. For brevity, we present only a summary in Table I. Intuitively, one may observe that for a specific probability of producing a good circuit (P_G) and for a given set of specifications, the yield and fault coverage of the test process will be determined by the test process thresholds. For each scheme, the threshold (for the checker or the test point in the reconfigured circuit) was set such that the yield of the test process would be approximately 90%. All the schemes were simulated assuming the probability of manufacturing a good unit, P_G was equal to 0.9. For each scheme, we report the best achieved combination of fault coverage and yield. As can be seen, some schemes are more effective than others. Yet, the fault coverage is generally unacceptable. In most cases, but not all, the yield is also unacceptable. None of the fault coverages listed in Table I would be acceptable for digital circuits.

IV. DIGITAL MEASUREMENT-BASED TEST

Both code-based and reconfiguration-based DFT are adversely affected by one significant factor: process variations have the same impact on signals in the test mode and during normal operation. In general, to measure a signal, the measuring instrument should be of greater accuracy than the signal being measured. The same should be true of a DFT scheme. Consider a code-based DFT scheme. Refer to one of the two signals as the *original* signal and the second as the *check* signal. To determine if the *original* signal is sufficiently accurate, we are using a *check* signal that is as inaccurate as the *original* signal. This leads to unsatisfactory results. To achieve a high fault coverage, any technique to measure signal values should use a check that is far more accurate than the target signal or parameter. We obtain the high measurement accuracy required by digitally estimating values of interest.

A. Digital Capacitor Ratio Estimation

We focus on switched-capacitor filters. To reduce the impact of process variations, filters are typically designed such that most output parameters of interest are determined by the values of a set of capacitor ratios. Given a circuit to be tested, if the

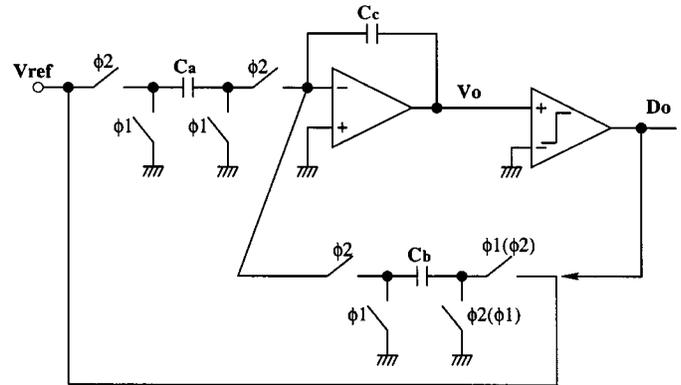


Fig. 3. Analog-to-digital capacitor ratio converter.

value of every capacitor ratio of interest could be measured with complete accuracy, the ratios could be used to characterize the transfer function of the circuit with great accuracy. We could then verify if the circuit meets the majority of its desired specifications. The set of specifications that we are unable to verify in this manner are noise and clock feed through related, and input and output impedances. All input-to-output transfer function specifications can be verified in this manner. Such a “constructive” test process would be useful practically only if output parameters of interest could be measured to the desired degree of accuracy. Many output parameters are actually determined by several ratios. Thus, this will require that capacitor ratios be measured with a much greater accuracy than that expected of the output parameters. For example, to obtain a tolerance of 0.1% in estimating output parameters, ratios may have to be measured to a tolerance of 0.01%.

The accuracy desired in ratio measurement is difficult to achieve with analog and/or off-chip measurement techniques. We achieve the accuracy desired in ratio estimation with an on-chip digital measurement technique. Fig. 3 shows the circuit diagram for an analog-to-digital capacitor ratio converter (ADCRC). This circuit is able to accurately convert a capacitor ratio into a digital value. It can be shown that the voltage at the output of the integrator, $V_o(n)$, after n clock cycles is given by (1) [18]. Note that the two values of the digital output D_o are $+1$ and -1 and n is the number of iterations for conversion

$$V_o(n) = \frac{C_a}{C_c} n V_{\text{ref}} - \frac{C_b}{C_c} \sum_{i=0}^{n-1} D_o(i) V_{\text{ref}} + V_o(0). \quad (1)$$

With appropriate algebraic manipulation it can be shown that the average digital value of the output is given by (2). Note that

the two values of the digital output are +1 and -1 and n is the number of iterations for conversion

$$V_{\text{digital-average}} = \frac{1}{n} \sum_{i=0}^{n-1} Do(i) = \frac{C_a}{C_b} - \epsilon_n \quad (2)$$

where

$$\epsilon_n = \frac{1}{n} \left[\frac{V_o(n) - V_o(0)}{V_{\text{ref}}} \right] \frac{C_c}{C_b}$$

Further, it can be shown that the worst case error is given by

$$\epsilon_{n\text{max}} = \frac{2}{n} \left[1 + \frac{C_a}{C_b} \right]$$

The set of equations above are valid for $C_a \leq C_b$, with the result the error can always be bounded by $4/n$ and can be made extremely small by increasing the value of n , i.e., the time spent on converting the capacitor ratio into a digital format. In theory, from (2) the capacitor ratio can be measured to arbitrary precision. However, this is limited by device noise, clock feedthrough, finite gain and bandwidth and other analog considerations. However, obtaining 12–15 bits of resolution in the ratio precision is definitely possible as this technique is identical to that used by conventional sigma-delta converters [20], [21] where 15–20 bit converters are regularly designed.

To measure a single ratio to n -bits, we require 2^n clock cycles using our first order sigma-delta converter based ADCRC. Therefore, to measure a ratio to 12 bits of accuracy, we need 4096 clock cycles. For the integrator, we measured two ratios. For the biquad we measured four ratios. The total number of cycles for these four ratios is 16,384. At a circuit speed of 100 MHz, this corresponds to a test time of 163.84 μs . If necessary the conversion time can be reduced significantly by using higher order ADCRC's. As with higher order sigma-delta converter the conversion time for a M th order ADCRC would be $2^{n/M}$ significantly reducing the test time. For example, for the same 12 bits of accuracy we would require 64 clock cycles and the overall test time would reduce to 2.56 μs .

To test the target circuit, the ADCRC must itself be defect-free. We briefly discuss how the ADCRC may itself be tested. The digital components, that is, the switches, the counter and the registers, can be tested using well-known digital test techniques. We focus on testing the sole analog component, the op amp. As with the circuit under test, two types of defects may occur in the op amp, hard defects and parametric defects. It has been shown that most hard defects cause the op amp output to saturate at one of the two rails. This type of an output error causes many errors in data conversion. While we do not have a detailed estimate of the fault coverage, it is reasonable to assume that such defects can be easily detected. As with the circuit under test, parametric faults in the op amp cause performance degradation. The sigma-delta conversion process, on which our ADCRC is based, is a very robust design. Small, parametric variations in the comparator, switches, clock period, reference voltage, finite opamp gain and bandwidth have minimal impact on sigma-delta based ADCRC [18]. We use the ADCRC to an accuracy of 12 bits of resolution. With careful design, the design is capable of a resolution of up to 20 bits. Thus, we are able to tolerate a wide range

of op amp parameter values. The design is capable of delivering 12 bits of resolution across the full range of normal process variations. For example, 12 bits of resolution can be obtained with op amp gains as low as 72 dB if a gain-squaring topology is used for the integrator in the ADCRC.

B. DFT Test Flow

Digital measurement of capacitor ratios enables the test process flow for a circuit to be greatly simplified. A circuit that incorporates the ADCRC would be tested as follows (in the following, the term "specification parameter" refers to a specification point on an output parameter):

- 1) the transfer function for the circuit under test is identified and expressed in terms of capacitor ratios. Currently, for most practical circuits, this can only be done manually;
- 2) each specification parameter of interest is processed as follows (all the steps are manual):
 - a) An acceptable range of values for the specification parameter is defined by the user;
 - b) the ratios that contribute to determining the value of the specification parameter produced by the circuit are identified;
 - c) an equation that expresses the value of the parameter in terms of the capacitor ratios is formed, usually derived from the transfer function.
- 3) Each die to be tested is processed as follows (all the steps can be automated):
 - a) the ADCRC circuit is used to measure each ratio of interest and the measured values are output from the circuit;
 - b) For each specification parameter, the numerical values for each of the ratios are inserted into the equations developed in Step 2;
 - c) If all the computed values lie within acceptable ranges, the die is declared as being good, else it is declared to be faulty.

C. System-Level Implementation

The ratio digitizer DFT scheme can be systematically implemented using a procedure compatible with design techniques for switched capacitor filter circuits. As mentioned earlier, most capacitors in a circuit are defined as multiples of a unit capacitor. In SC circuits, all the capacitors required for the design are realized together in a single two-dimensional physical array of unit capacitors. Each capacitor required in the design is formed by electrically connecting the appropriate number of unit capacitors. The array contains enough unit capacitors to form all the capacitors required by the design. The sizes of a few elements in the array may be a fraction of the unit size to accommodate noninteger ratios. There are two outputs (one for each terminal) for each capacitor realized.

At the system level, the DFT scheme can be realized as shown in Fig. 4. The test mode signal isolates the capacitor array from the active circuitry during the test process. The ratio measurement process is executed in several iterations. On each iteration, the digitizer (ADCRC) verifies the accuracy of one ratio, a process that requires multiple clock cycles. As shown in Fig. 4,

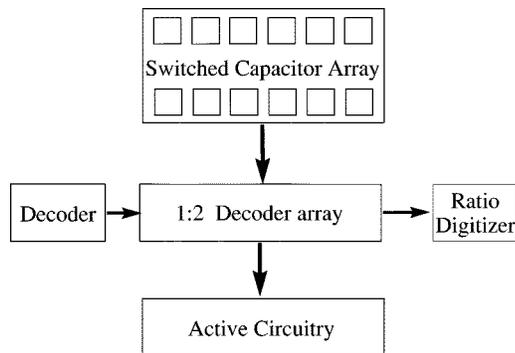


Fig. 4. Block diagram for proposed DFT scheme.

on each iteration a primary decoder (similar to a memory address row decoder), is used to select and drive a signal which drives a pair of 1:2 decoder structures. The outputs of the capacitor array are connected to the data input of the 1:2 decoder. Fig. 5 shows how, using two 1:2 decoders, the outputs of a pair of capacitors, whose ratio is to be measured, are directed to the inputs of the ratio digitizer. Recall that each capacitor has two terminals. Thus, a structure identical to Fig. 5 has to be used to direct the other terminals of the two capacitors in the ratio to the inputs to the ADCRC. No more than one output of the decoder is active at any instant. The system-level decoder has as many outputs as there are ratios to be measured. If a capacitor belongs to multiple ratios, it has to be connected to more than one output of the system-level decoder. These signals are ORed as shown in Fig. 5. In the figure capacitor $c1$ is used in two ratios, whereas capacitor $c2$ is used in only one ratio.

After each ratio is measured, the contents of the counter are unloaded and transported off the IC. The configuration shown in Figs. 4 and 5 offers several advantages.

- The test structure introduces additional parasitics at the outputs of the capacitors. We have attempted to minimize the additional capacitive load on all the capacitors. For example, let us assume that the 1:2 decoders are realized using two CMOS transmission gates. The data input to the decoder is connected to four transistor drains. Thus, the additional capacitive load on each terminal is 4 drains. (This is independent of the number of ratios to which a capacitor belongs.)
- All capacitors see the same type of load. Hence, the additional load can be systematically characterized without significant effort.
- The size of the load can also be tuned to each capacitor, by increasing transistor sizes in the 1:2 decoders, to make the additional parasitics proportional to the sizes of each of the capacitors.
- The design process for this DFT scheme is very simple. Methods to systematically design decoder structures are well-known.

The primary limitation of the DFT scheme is that it will result in area overhead for test. In a switched capacitor circuit, the passive components may occupy as much as 80% of circuit area. All the additional circuitry for the scheme consists of active elements, not passive components. It is reasonable to assume that the overhead incurred by this scheme will be limited.

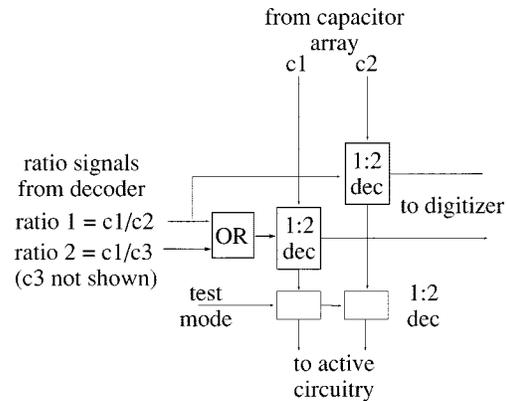


Fig. 5. Reconfiguration network for proposed DFT scheme.

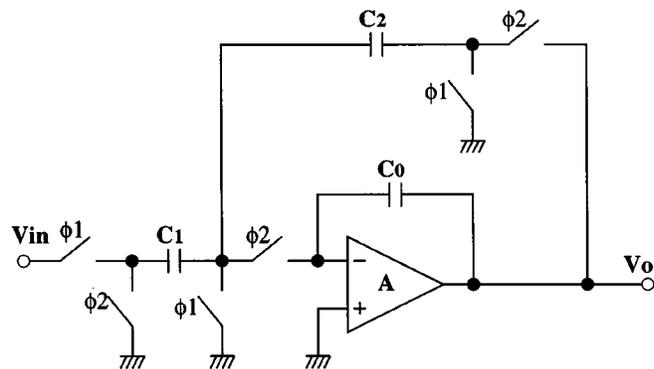


Fig. 6. Simple lossy integrator circuit diagram.

V. APPLICATION EXAMPLES

The increased accuracy in estimating capacitor ratios enables us to estimate output parameters with the accuracy desired in practice. We illustrate our methodology by way of a simple example followed by results for a more complex design. For each example, we assess the impact of process variations and the quality of the DFT technique.

A. Lossy integrator

Consider the SC lossy integrator circuit shown in Fig. 6. The transfer function for the filter is given by (3). For simplicity, we shall currently limit ourselves to ideal amplifiers

$$H(z) = \frac{C_1}{C_o + C_2} \frac{z^{-1}}{1 - \frac{C_o}{C_o + C_2} z^{-1}} = \frac{\alpha z^{-1}}{1 - \beta z^{-1}} \quad (3)$$

where $\beta = (1/(1 + (C_2/C_o)))$ provides the pole location on the z plane and $(\alpha/(1 - \beta)) = (C_1/C_2)$ provides the magnitude of the transfer function at dc. The transfer function for this circuit is plotted in Fig. 7

1) *Impact of Process Variations:* We note that both the pole location and the dc gain are a function of capacitor ratios. If these two ratios deviate from their expected value, the two parameters will shift correspondingly. Thus, the impact of process variations on capacitor values and consequently on output parameters can be gauged easily. Conversely, if

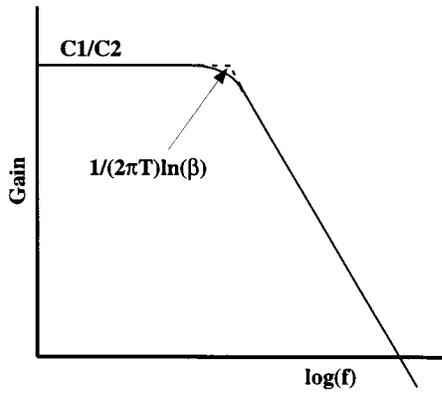
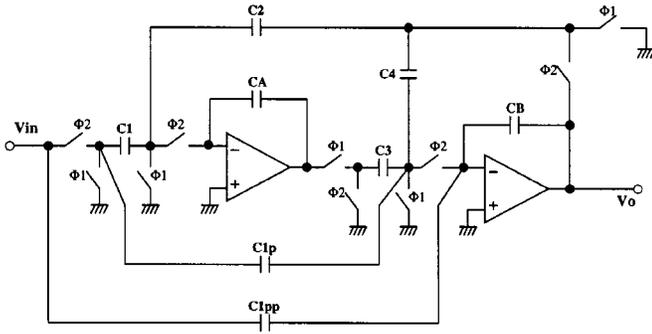


Fig. 7. Transfer function for lossy integrator.

Fig. 8. Low Q switched-capacitor biquad circuit.

we can accurately measure the ratio of capacitors we can provide information about the functional performance of the switched-capacitor filter. In particular, for our example if the capacitors ratios of interest are C_2/C_o and C_1/C_2 . We can obtain both these values by connecting the appropriate capacitors to our ADCRC circuit shown in Fig. 3. In our simple example the relationship between the functional performance and the capacitor ratios were fairly straightforward. However, as illustrated next the relationship is somewhat more complex for even moderately complex circuits. So, one has to resort to numerical techniques rather than closed form solutions.

B. Switched-Capacitor Biquad

Fig. 8 [17] shows the circuit diagram for a low Q switched-capacitor biquad filter section. The transfer function for a low-pass version of this circuit can be shown to be given by (4). We note that both the pole radius and angles are functions of capacitor ratios only

$$H(z) = \frac{\left[\frac{C_1 C_3}{C_a (C_b + C_4)} \right] z^{-1}}{1 - \left[\frac{2C_a C_b + C_a C_4 - C_2 C_3}{C_a (C_b + C_4)} \right] z^{-1} + \left[\frac{C_b}{C_b + C_4} \right] z^{-2}} \quad (4)$$

where the radius of the pole locations on z plane is given by (5) and the angle of the poles is given by (6)

$$r^2 = \frac{1}{1 + \frac{C_4}{C_b}} \quad (5)$$

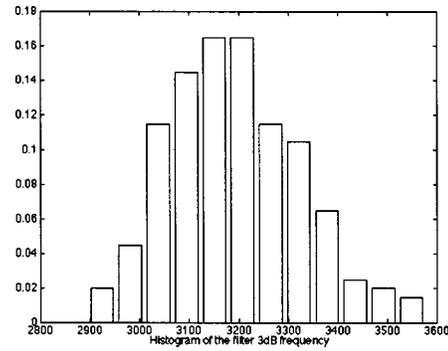
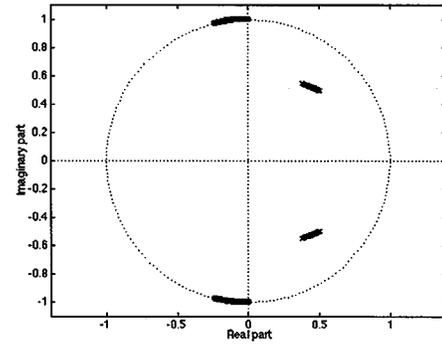


Fig. 9. Histogram of the variation in the 3-dB frequency of the SC low-pass filter.

Fig. 10. Variations in the pole and zero location in the z plane.

$$\theta = \cos^{-1} \left[1 + \frac{C_4}{2C_b} - \frac{C_2 C_3}{2C_a C_b} \right]. \quad (6)$$

1) *Impact of Process Variations:* In general, variations in the capacitor values and capacitor ratios causes the functional specifications to vary as well. For example, in the case of a SC low-pass filter the list of functional specifications that can be affected include the dc gain, the 3-dB bandwidth, the in-band ripple, the out-of-band attenuation, etc. For our simple lossy integrator the translation from parameter values to functional performance was relatively straight forward. A more complex circuit requires a simulation-based approach to assess the impact of process variations. As an example, Fig. 9 shows the variation in the 3-dB frequency of the SC low-pass filter due to variations in the capacitor ratios. The impact of capacitor variations on the pole-zero locations are shown in Fig. 10.

C. Results

We used simulation to verify the quality of the test process for each of the application examples. First, we discuss the experimental process used.

1) *Experimental Process:* The quality of a test process for the two example circuits based on the ratio-digitizer was verified with a Monte-Carlo simulation process. Each circuit was simulated for 2000 iterations. During the simulation, we maintain four counters corresponding to the following:

- i) number of good circuits that pass the test;
- ii) number of good circuits that fail the test;
- iii) number of faulty circuits that pass the test;
- iv) number of faulty circuits that fail the test;

Each iteration is conducted as follows:

- a) The capacitors in the circuit are given a new set of values. Each capacitor is assigned a random value that lies within a percentage Δ of its mean value. The value of Δ is a function of capacitor size that is determined by process variations. The values are specified to 64 bits of precision, the maximum allowed by the simulation tool.
- b) The values of all the output parameters of interest are computed from these “known” (double-precision) capacitor values. To limit computational effort, we only consider a small set of specifications. If the values are within acceptable ranges, the circuit formed on this iteration is declared to be a good circuit. Else, the circuit is declared to be a faulty circuit. The appropriate counter is incremented.
- c) The measurement with the ADCRC of each ratio of interest to a finite number of bits of precision is simulated.
- d) From the “estimated” (low-precision) ratios, the values for the output parameters considered in Step 2 are again computed. If these values are within acceptable ranges, the the circuit formed on this iteration is declared to have passed the test process. Else, the circuit is declared to have failed the test process. The appropriate counter is incremented.

The fault coverage of the test process is the percentage of faulty circuits that fail the test process. The yield is the percentage of good circuits that pass the test process. Ideally, both of these should be 100%.

Because the final limits of resolution are dependent on the fabrication process, they are not easily quantifiable, accuracy estimates from circuit simulation are not likely to prove too conclusive. To ensure the validity of our approach we run Monte-Carlo simulations on two sets of different circuits. Both simulations are done in Matlab. However, to confirm the validity of the Matlab simulations one complete circuit-level level simulation using SPICE was also done for each of the circuits.

2) *Lossy Integrator*: In the first experiment we used the lossy integrator shown in Fig. 6. As discussed earlier in this circuit the overall transfer function is determined by just two capacitor ratios. Two thousand simulation runs were repeated for this circuit. For each run the individual capacitors were varied and for this set of simulations the capacitor matching was assumed to be 1%, i.e., the capacitor ratios had a one sigma deviation of 1%. Each capacitor ratio was measured with a 12-bit accuracy (requiring 2^{12} clock cycles). For this simulation only dc gain for the filter was considered. The circuit was designed to have a dc gain of 0 dB. Additionally, a ± 2 percent variation in the dc gain was considered to be an acceptable design. *Starting with a initial yield of 86.6 the parametric fault coverage was 99.8% and the yield loss was 0.4%.*

3) *Switched-Capacitor Biquad*: For the next experiment we used the two stage biquad circuit shown in Fig. 8. The transfer function shown in (4) can be rewritten in terms of capacitor ratios as shown in (7), where $R_1 = C_1/C_a$, $R_2 = C_4/C_b$, $R_3 = C_2/C_a$ and $R_4 = C_3/C_b$. We note that all capacitor ratio dependent performance specifications are defined by these four ratios: R_1, R_2, R_3, R_4 . We are able to specify the passband gain, the 3-dB frequency, the passband ripple, and the stopband attenuation using just these four ratios. It should also be noted that

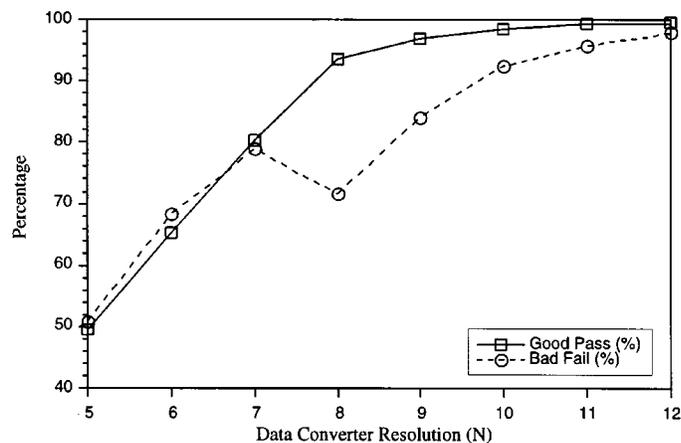


Fig. 11. Impact of capacitor ratio measurement accuracy on test method.

to measure these diverse performance specifications in using normal test techniques would require separate test setups and different sets of test equipment. Here, we are able to use a single test technique a number of times to evaluate all performance specifications

$$H(z) = \frac{\left(\frac{R_1 R_4}{1 + R_2}\right) z^{-1}}{1 - \left(1 + \frac{1 - R_3 R_4}{1 + R_2}\right) z^{-1} + \left(\frac{1}{1 + R_2}\right) z^{-2}}. \quad (7)$$

For this experiment a complete capacitor matching model that includes 1:1 and 1:N matching information was created [12]. This capacitor matching model assumed that two 1 pF capacitors can be fabricated such that the one sigma variation is 0.3%. This switched capacitor filter uses a 20 KHz and implements a low-pass Butterworth filter. It is designed to have a dc gain of 0 dB, a passband of 1 kHz, a stopband at 5 kHz with a stopband attenuation greater than 15 dB. Passband ripple and dc gain were used to verify operation. However, once the four capacitor ratios are known any and all performance specifications can be evaluated. In this experiment we have restricted ourselves to just these two specifications to reduce computation costs. Once again 2000 simulation runs were used for each individual result. However, in this case we varied the resolution of the data converter used to measure the capacitor ratios. As we are using a first order sigma-delta converter a higher resolution entails using more clock cycles to measure the result. For this set of results we varied the data converter resolution from 5 to 12 bits. To provide an additional measure of reality KT/C noise resulting from the input sampling capacitor were also added to the simulations. The starting yield for all these simulations varies between 88% and 90%. A one percentage variation in either specifications is considered to be acceptable. The results of the simulations is shown in Fig. 11. The solid line with the squares shows the percentage of good part that pass the test and the dashed line with the circles shows the percentage of bad circuits that fail the test. We note that the quality of the test procedure increases with data converter resolution. We note that there is lot of improvement for resolutions below 8 bits and progressively less as the number of bits increase. Additionally, there is not a lot of room

for improvement beyond 12 bits. In particular, at 12 bits the fault coverage is 98.1% and the yield loss is 0.39%

VI. CONCLUSION

In both code-based and reconfiguration-based DFT schemes, even if a circuit passes the test only conclusions of limited utility can be drawn about the quality of the original circuit. Code-based DFT schemes suffer from the limitation that the signals cannot be measured with an accuracy greater than the tolerance desired in the signal. Reconfiguration-based DFT schemes suffer from the limitation that the circuit tested is not the one used. The reconfigured circuits are not characterized completely but only tested to see if they meet a different set of specifications.

We present a DFT scheme for switched-capacitor circuits that realizes extremely high measurement accuracy. We test a filter by completely characterizing all capacitor ratios of interest. We are able to achieve accuracy far greater than previous efforts by moving ratio estimation to the digital domain. Further the accuracy of the estimate is not significantly influenced by the tolerance of any reference signal. By accurately characterizing all capacitor ratios of interest, we are able to characterize the transfer function of the filter. Therefore, we are able to verify the ability of the filter to satisfy its specifications, and the tolerance achieved in each of these specifications. We believe the accuracy of our technique is at least an order of magnitude greater, if not more, than that of any design for test scheme reported in the literature.

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