# Analog System Performance Estimation in the VASE (VHDL-AMS Synthesis Environment)

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# 1. INTRODUCTION

The VHDL-AMS Synthesis Environment (VASE) is a vertically integrated collection of software tools for synthesis of CMOS mixed signal systems from specifications written in VHDL-AMS. As discussed and demonstrated at the 1997 EETimes Analog and Mixed Signal Applications Conference [1], three successive generations of VASE systems are being developed.

Critical to the success of analog synthesis in VASE is the accuracy of analog performance estimation at various levels of abstraction. The analog performance estimator (APE) in VASE is used during mixed signal partitioning, analog behavior synthesis as well as analog circuit synthesis. APE is capable of accepting the design parameters (bias current) of an analog component as input and determines its performance parameters (UGF, slew rate, area) along with anticipated sizing for the circuit components.

VASE APE is structured as a hierarchical estimation engine and contains performance models of analog circuits at various levels of abstraction. The levels include the basic circuit elements (MOS transistors, resistors, capacitors), basic analog components (current mirrors, V-I converters), operational amplifiers (in various configurations), analog library cells (integrators, filters, amplifiers) and the user-level analog structures which include series and parallel combinations of the library cells with or without feedback connections. APE uses SPICE models of analog circuit elements and performance composition equations for determining circuit performance at other levels of abstraction.

APE provides fast and accurate estimates of analog system performance at various levels of abstraction. This presentation will focus on the analog performance estimator and how it is used by the constraint transformation and module selection tools in VASE. Specific emphasis will be placed on:

• The hierarchical estimation techniques used in the APE.

- Experimental results demonstrating the accuracy of the estimates provided by the APE.
- The impact on the speed and quality of analog circuit synthesis when the APE is used in analog design-space exploration.

## 2. Architecture of VASE

Figure 1 shows the architecture of VASE. The input is a VHDL-AMS description of the mixedsignal system and the constraints on the system. After partitioning and performing mixed-signal constraint allocation, the digital behavior is subjected to digital high-level synthesis. The analog behavior is taken through analog behavioral synthesis to generate an analog system-level net-list. The constraint transformation and module selection step allocates constraints to the individual components in the system, and selects a suitable topology for the component from the component library. Finally, each of the selected topologies along with the allocated constraints is sized by the circuit synthesis tool to generate a sized transistor net-list. This step is followed by layout synthesis and layout integration steps to generate the final layout of the system. In the Figure 1, the usage of the analog performance estimator in the various stages of VASE is highlighted. In the final section, we elaborate on the role of the estimator in the different stages of mixed-signal synthesis.

## 3. Analog Performance Estimator

Our performance estimation methodology is based on a hierarchical structure as shown in Figure 2. This methodology predicts the characteristics of an analog circuit and produces a roughly sized circuit. The inputs are a circuit topology and a set of constraints. The topology is a net-list of blocks selected from the analog component library, which behaves as the specification. The hierarchy goes from the CMOS Transistors to the User Application.

#### 3.1 CMOS Transistor Models

The transistor models are useful in predicting the performance of the devices before they are fabricated. There are several device models in the market to be used with different simulation tools. As SPICE has become the industrial standard for analog integrated circuits simulation, the SPICE models are one of the most used. SPICE and SPICE-like simulators implement various levels of device models [2]. The first generation comes from mathematical models. The second generation of models is based on the Berkeley Short-Channel IGFET Model (BSIM), which use empirical parameters instead of analytic equations.

A CMOS transistor's operating characteristic can be classified into three modes of operation: cutoff, non-saturation and saturation regions, where each is characterized by a DC and an AC model. The DC model describes the voltages and currents through the transistor ports. The current drain-source  $I_{ds}$  is a function of the voltage gate-source  $V_{gs}$ , voltage drain-source  $V_{ds}$ ,

voltage flat-band  $V_{fb}$ , and the fabrication process parameters. The small signal equivalent circuit characterizes the CMOS transistor behavior for AC, where the transconductance is a function of  $I_{ds}$  and the process parameters.

The transistor sizing process involves solving these equations such that the constraints are met. It should be noted that, the sizing process depends on the fabrication process parameters, and the sizing accuracy is directly proportional to the precision of the transistor models.

#### **3.2 Basic Analog Components**

A library of basic components is the next level in the estimator hierarchy. Some of these components are DC-bias voltages, current sources, gain amplifiers, output buffers, differential amplifiers and differential-to-single-ended converters. The symbolic equations of these elements are kept in memory. For example, a Differential CMOS amplifier can be characterized by the differential-mode gain  $A_{dm}$ , the common-mode gain  $A_{cm}$ , and the common-mode rejection-ratio CMRR. Each of these parameters depends on the topology of the basic component and the sizes of the transistors. When a component is required, the component elements are sized according to the specifications. A list of performance estimated parameters are attached as attributes to the sized component.

## 3.3 **Operational Amplifiers**

The third level of the hierarchy consists of a set of Operational Amplifier topologies. The general structure of an op-amp is represented by three stages: (1) Differential input amplifier; (2) Level shift, differential to single ended converter and gain stage; (3) Output buffer. Each of these stages can be implemented with elements from the library of basic components. The op-amp behavior depends on the topology selected, the behavior of the basic analog components and the sizes of the transistors. The differential gain, common gain, slew rate, common-mode rejection-ratio, unity gain frequency, input impedance and output impedance describe the performance of an op-amp. The op-amp estimation procedure uses the attributes of the basic components after being sized and the equations, which relate these attributes to the op-amp behavior. Then, the sized op-amp is marked with its performance attributes.

#### 3.4 Analog Modules

The library of components is the fourth level of the hierarchy. This library is constructed with opamps, resistors, capacitors and transistors. The library consists of circuits such as inverting amplifiers, integrators, comparators, analog-to-digital converters, digital-to-analog converters, filters and sample-and-hold circuits. The performance of each element depends on its topology and the sizes of the op-amp used. As each of the components describe different analog circuits, the performance parameters are specific for each analog module. The performance estimation of these components is done using the operational amplifier estimation attributes and the component library information.

#### **3.5** User Applications

The User Application is the highest level in the hierarchy. At this level, the specification is a structural definition of the analog system. The system is defined as a net-list of library components. The net-list is built with four configurations: serial, fork, join, and feedback. Each configuration consists of blocks, where the blocks are elements of the analog module library or one of the four configurations. In the serial configuration, the output of a block is the input of the next block. In the fork configuration, an input goes to two blocks, where each block has its own output. A block with two inputs and one output creates the split configuration. In the feedback configuration, the output of a block is fed-back through another block to the input of the first block. The performance estimator uses the library estimation and the relation of the four configurations to estimate a system net-list.

#### **3.6 APE Experimental Results**

To illustrate the effectiveness of APE, the performance of an Analog-to-Digital Acquisition System (see Figure 3) was estimated. For all components, the MOSIS HP 0.8µm CMOS26G n-well, triple metal, run N58A process was chosen. The input to the system is an analog signal, and the output is a 4-bit digital signal. The input is a sinusoidal signal with 10mV peak and a bandwidth of 300Hz to 3.3Khz (Telephone bandwidth). The first stage has a gain of 100, so that the output is a 1V peak. The sampling frequency used was 8KHz, with a 50% duty cycle TTL sampling signal. The ADC implemented was a 4-bit Flash Analog-To-Digital Converter.

ASTRX/OBLX [5] tool was used to perform the circuit synthesis. (ASTRX/OBLX is an automated synthesis tool developed at the Carnegie Mellon University, which can size a predefined circuit topology. The circuit topology is specified on a SPICE-deck format, where the transistor sizes and bias points are set as unknowns [6].) It was observed that ASTRX/OBLX was unable to converge when the input description did not have knowledge of the solution space. The input file was then modified such that the intervals were reduced and the starting points were set using the APE's estimated transistor-sizing information. A functional circuit was produced by ASTRX/OBLX using this modified input. Table 1 compares the estimation and SPICE simulation results after the circuit was synthesized.

#### 4 Analog Performance Estimator in the context of VASE

In this section, we discuss the analog performance estimator in the context of mixed-signal synthesis in VASE.

#### 4.1 Application of APE for Behavioral Synthesis of Mixed-Signal Systems

The VASE APE is used during solution space exploration for behavioral synthesis of mixedsignal systems. In our CAD environment, mixed-signal systems are specified in VHDL-AMS [9] by describing their behavior. The specification is compiled into an internal representation. After this, the exploration step for system-level topology selection is performed. This is done by extensively using information offered by APE. *Topology selection* explores possible component interconnections that realize the specified functionality. The topologies represent different "solvers" for the defined DAE. The solvers are ranked for synthesis according to the performance information provided by VASE-APE at the architectural level. For each topology that proves to be eligible for further analysis, a constraint transformation and component selection step follows.

#### 4.2 Analog System Level Constraint Transformation

The task of transforming the high-level specifications onto module level parameters is called constraint transformation. The constraint transformation and topology selection step in VASE takes as input the analog system level net-list and the constraints on the analog system. It generates the set of design/performance constraints on the individual modules in the system and selects a suitable topology for the module from the component library. The selected topology along with the constraints is used by the underlying circuit synthesis tool to generate a sized transistor net-list that is followed by the layout synthesis step. Typically, the circuit synthesis process involves searching the parameter space of the circuit in order to find the values of the widths and lengths of the transistors that satisfy the constraints. This search space is large because of the number of variables involved. The constraint transformation mechanism in VASE explores the parameter space at the system level to find ranges for the module design/performance parameters. During the exploration step, the performance estimator that is used by the constraint transformation engine generates approximate sizing solutions, which are used to limit the search space of the circuit synthesis tool. The constraint transformation method consists of an Interval Genetic Algorithm core interacting with the hierarchical performance estimator.

#### 4.2.1 Genetic Algorithms

Genetic Algorithms (GA) are stochastic search techniques based on the mechanism of natural selection and genetics [8]. They start with an initial set of random solutions called a *population*. Each individual solution being called a *chromosome*, which represents a candidate solution to the problem being solved. The chromosomes evolve through successive iterations, called *generations* by using genetic operators, like *crossover* and *mutation*. Each chromosome is evaluated using some measure of fitness, to determine which of them are used to form new ones.

#### 4.2.2 Constraint Transformation using Genetic Algorithms

Constraint transformation as mentioned earlier involves computing values for the component design parameters, while topology selection is the task of selecting a suitable implementation for

the component from the set of available components in the library. The solution encoding for the constraint transformation problem consists of a two dimensional array of real numbers. The first row represents the center of the interval being computed and the second row, a delta value that gives the width of the interval. The representation consists of two parts, the first part representing the values to be assumed by the design parameters and the second part represents the topology information. Figure 5 shows the fitness evaluation technique that uses the analog performance estimator (APE). In a solution, the design parameters and the topology information corresponding to each of the component in the system level net-list are used to evaluate the performance of the component by calling the performance estimator. The component performances corresponding to the current set of design parameters are stored in an intermediate performance array. With this set of performances, the APE is invoked at the user application level to evaluate the performance of the entire system. At the User Application level APE estimates the performance of the entire system, given the performances of the individual blocks constituting the system. The objective function is a two level one, the local objective function verifies whether all the constraints satisfy the user specified ones, and the global one checks whether all the solutions in the region are constraint satisfying. The GA works towards minimizing the objective function. The global objective function returns a value of zero only if all the points in the region are constraint satisfying. Uniform crossover and non-uniform mutation operators were defined for the representation. The GA generates a solution that best satisfies the user asserted constraints. The solution gives us the values for the design parameters and a topology for each of the component in the system level net-list.

## 4.3 Analog Circuit Synthesis

The analog circuit synthesis process typically consists of three steps: topology selection, circuit sizing and design verification [3],[4]. Topology selection is the process of choosing an architecture that performs the desired behavior. The circuit-sizing phase determines the physical dimensions, bias points, and element values to meet user constraints. Typically, the circuit sizing process employs an algorithm to search through the design-space until converges at a design that is likely to meet the user constraints. The speed of convergence and the quality of the design produced depend on the initial design point as well as the design-space exploration algorithm used. Finally, the design verification phase is typically performed by a circuit simulator such as SPICE.

Some of the analog circuit synthesis tools starts with a pre-selected topology and attempt to size it until the constraints are satisfied. Other tools try to select an architecture from a pre-defined database. The verification process involves many iterations through the design process, and a backtracking methodology is generally used. The circuit synthesis tool ASTRX/OBLX assumes a fixed topology and uses a simulating annealing process to size the analog cells.

ASTRX/OBLX requires several conditions to converge. The simulation is performed in two phases, the DC analysis, which evaluates the bias point, and the AC analysis, which evaluates the small signal behavior. The cost function is evaluated using these analyses and it is compared against the constraints, objectives and specifications. A proper test-bench becomes critical to find a functional design. However, it may take an expert analog designer to decide a proper test

bench. Besides, The convergence time and the accuracy of results are improved when the unknowns intervals are kept small and the number of unknowns, specifications, objectives and constraints are as minimum as possible. Therefore, an initial knowledge of the transistor sizes, operating points, and small signal characteristics can speed up the process of convergence successfully. The Analog Performance Estimator presented in this paper provides a way to generate such initial design conditions.

## 4.4 Analog Component Library

The analog cell library consists of a set of components such as current mirrors, opamps, differentiators, integrators, adders, multipliers, dividers, sample and hold circuits, analog to digital converters, and digital to analog converter. Each component describes just the circuit topology at the CMOS transistor level; no sizing information is obtained from the library. The goal is to have a retargetable library that doesn't depend on the fabrication process parameters and the functional constraints. However, having a library in this format requires extra information to guide the synthesis process. The performance of each library component depends on the fabrication process parameters, the sizes and the environment in which is used. The analog performance estimator presented in this paper can generate such information.

# 5. Conclusion and Future plans

The analog performance estimator (APE) presented in this paper uses a hierarchical approach to analog circuit performance and size estimation. These size estimates could be used effectively as a starting point for analog circuit synthesis. The APE was discussed in the context of a mixed-signal synthesis system (VASE). The application of APE in performing constraint transformation was also presented. Currently we are trying to characterize the error of the estimator and use this to improve the accuracy of the constraint transformation process. Work is also directed towards extending the estimator for use in analog behavioral synthesis.

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