An Analysis of Power and Stability in 6T, NC, Asymmetric, PP, and P3SRAM Bit-Cells Topologies in 45nm CMOS Technology

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ABSTRACT
In modern digital architectures, more and more emphasis has been laid on increasing the number of SRAMs in a SoC. However, with the increase in the number of SRAMs, the power requirement also increases, which is not desired. This calls for an urgent need for an SRAM with low dynamic and static power consumption and stability at the same time.The design and simulation work for 6T-SRAM, NC-SRAM, Asymmetric SRAM, PP-SRAM, and P3-SRAM topologies have been carried out to see their power consumption and performance at 45nm CMOS technology at 300^{o}K for V_{DD}=0.7V and 0.8V. At V_{DD}=0.8V, P3-SRAM consumes 69.069%, 13.61%, 82.03% and 86.11% less standby power than 6T-SRAM, NC-SRAM, Asymmetric SRAM and PP-SRAM, respectively.Similarly, the dynamic power consumed by P3-SRAM is 88.88%, 89.23%, 85.25% and 89.5% less than 6T-SRAM, NC-SRAM, Asymmetric SRAM and PP-SRAM, respectively at V_{DD}=0.8V.

General Terms
SRAM, VLSI, P3 SRAM

Keywords
Six-Transistor SRAM, NC-SRAM, Asymmetric-SRAM, PP-SRAM, P3-SRAM, Leakage Power, Stability.

1. INTRODUCTION
In modern day devices, more and more SRAM circuits are being fabricated on a single chip [1][2]. As a result, SRAMs occupy maximum areain a silicon die. Hence, they account for one of the major causes of power consumption on a silicon chip. This power consumption by SRAMs effects battery powered electronic devices adversely. The large power consumption of an SRAM affects other performance parameters like speed, stability and area of an SOC.

Two main factors that contribute to power dissipation in an SRAM are dynamic and static power dissipation.It has been observed that dynamic and static power dissipations account for 40% of the total power dissipation in an IC in active mode [3][4]. Dynamic power is the power that is dissipated when a device is switching states. On the other hand, static power is the power that is dissipated when a device is in idle/standby state.

The leakage current, which leads to power dissipation, constitutes three main components, i.e., gate leakage currents because of small gate oxide thickness, sub-threshold current which flows at low threshold voltages, and band-to-band leakage because of heavily doped halo doping profile[5]. In state of the art SRAM cells, a channel length as low as 45nm is being used. This scaling leads to a reduction in gate-oxide thickness, and therefore leakage current is largely contributed by gate-oxide leakage [5].

With tremendously increasing static and dynamic power dissipation because of increasing number of transistors on a chip, there is a serious need for a low power SRAM cell which is stable and maintains high speed of operation at the same time.

The leakage current can be controlled by controlling its three main components. One way to reduce the tunnelling currents is touse pMOS instead of nMOS [5]. Thebarrier height for hole tunnelling (4.5ev) is higher compared to barrier height for electron tunnelling [5], whichleads to significantly lower tunnelling currents in pMOSas compared to nMOS[5].

In this paper, the introduction has been discussed in section 1 which is followed by the operation of Conventional 6T-SRAM Bit-Cell in section 2. SRAM power consumption consisting of static and dynamic power has been discussed in section 3. Then, the related work is reviewed in section 4 which is followed by section 5 comprising the design and simulation work. Lastly, the work has been concluded in section 6.

2. THE CONVENTIONAL 6T-SRAM BIT-CELL
An SRAM bit-cell can store one bit of binary data.The Conventional 6T SRAM Bit-Cell has large noise immunity and data stability independent of leakage currents in micrometer and sub-micrometer CMOS technologies. It comprises of two CMOS inverters (M1, M3 and M2, M4) and two pass transistors (M5 and M6). The pass transistors act as the input/output ports of the internal inverters and are controlled by the Word Line (WL). The input/output ports of the SRAM bit-cell are Bit Line (BL) and Bit Line-bar (BLB) [6].

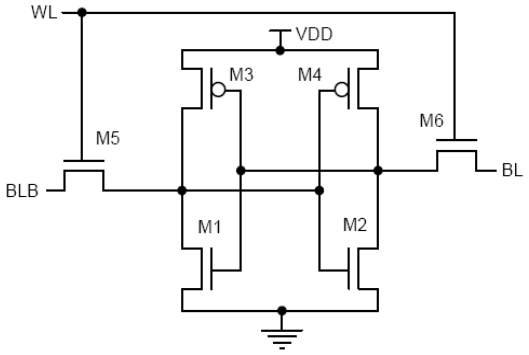

Fig 1: Conventional 6T SRAM Bit-Cell [6]

2.1. The Operation of Conventional 6T SRAM Bit-Cell

There are three types of data operations in an SRAM Bit-Cell: Data Read Operation, Data Write Operation and Data Hold Operation.

2.1.1 Data Read Operation

During the data read operation, the word line is at logic '1' (WL='1') which turns on the pass transistors M5 and M6. BL and BLB are pre-charged to '1', i.e., V_{DD}. The transistors M1 and M4 are ON. The pass transistors transfer the values of Q and QB to BL and BLB. BLB discharges through M1 and M5 and M4 and M6 pull BL to V_{DD}, i.e., BL='1'. This voltage difference is sensed and amplified to logic levels by sense amplifiers.

2.1.2 Data Write Operation

During the data write operation, the values to be written in the memory cell are given to BL and BLB. Word line is set to logic '1' (WL='1') due to which the pass transistors M5 and M6 are turned ON and the data is written into the cell. After the data write operation, word line is set to V_{SS} level and the bit lines to V_{DD} level.

2.1.3 Data Hold Operation

When the SRAM cell is powered up and the Word Line is at logic '0' (WL='0'), the SRAM cell is said to be in Data Hold Mode. When WL='0', the pass transistors - M5 and M6 are turned off. The two cross-coupled inverters reinforce each other without being affected by BL and BLB. The current drawn from the power supply in the data hold operation is known as Standby Current.

3. SRAM POWER CONSUMPTION

The total power consumption in a SRAM bit-cell consists of Static and Dynamic Power, as shown in eq(1) [10].

$$P_{total} = P_{static} + P_{dynamic} \quad \text{eq(1)}$$

3.1 Static Power

Static Power is the amount of power dissipated when data is held in an SRAM bit-cell because it needs power supply to retain the data stored in it. Stand-by power dissipation in a single cell is small but it adds up to a very large value in a multiple cell array. Static power dissipation is because of leakage current, hence, it is also known as leakage power. This power is described mathematically in eq(2) [10].

$$P_{static} = P_{leakage} = I_{leakage} \times V_{DD} \quad \text{eq(2)}$$

3.2 Dynamic Power

Dynamic power is the power dissipated when an SRAM is switching states while drawing energy from the supply voltage. Almost half the power required in the charge-up mode of operation is dissipated in the form of dynamic power. During the charge-up state, voltage at output node changes from 0 to V_{DD} which results in dissipation of heat in the conducting pMOS transistors. During the charge-down state, power stored in output capacitor is dissipated, heating up the nMOS transistors. This power which is dissipated heats up the transistors in the SRAM. Dynamic power can be expressed mathematically as shown in eq(3) [10].

$$P_{dynamic} = C_{load} \times V_{DD}^2 \times f_{clk} \quad \text{eq(3)}$$

where,
C_{load} is the capacitive load,
V_{DD} is the voltage swing, and
f_{clk} is the number of logic-state transitions

4. A REVIEW OF RELATED WORK

In this section, some previously proposed SRAM designs are discussed. The first among them is [7] Asymmetric SRAM cell design .In this design, an nMOS is added to SRAM design. The advantage of inclusion of an nMOS is reduction in gate leakage when '0' is stored. However, the gate leakage current increases when '1' is stored. This is achieved at the cost of increased SRAM cell area and longer read, write and access times. DC noise margin remains the same [7].

It is seen that an asymmetric SRAM gives good performance at data state '0' but the area increases due to the inclusion of an extra nMOS per bit-cell.

The Self Controlled Voltage Levels (SVL) technique uses full supply voltage in the active mode and a reduced supply voltage in the stand-by mode in order to reduce the leakage power.
During the read/write operation, the WL and BL's must be active, i.e., for any read/write operation, all the cells in the memory core need to wake up even if the read/write operation has to be performed in one cell.

Another previously proposed design is [8] NC SRAM design. This design implements dynamic voltage scaling. It uses two additional pass transistors to provide different ground levels for active and idle states. The new virtual ground formed at node A reduces gate leakage and sub-threshold currents, but read,write and access performances are degraded [8].

Yet another approach [9] to reduce the gate leakage is to increase the gate oxide thicknesses of the nMOS pass transistors and the nMOS pull down transistors. Here, a dual threshold voltage technique is used in which cell evaluation is performed at a high threshold voltage for different transistors. The proposal discussed above gives low power consumption and high stability, but read access time is prolonged.

Another design approach is a nine-transistor SRAM. In this approach three nMOS transistors are used to separate read and write circuits. This approach results into a higher stability, but at the same time cell area increases.

5. DESIGN AND SIMULATION WORK

The design and simulation work for 6T-SRAM, NC-SRAM, Asymmetric-SRAM, PP-SRAM, and P3 SRAM topologies have been carried-out to see their power consumption and performance at 45nm CMOS technology at 300^{o}K for V_{DD}=0.7V and 0.8V.

5.1. Standby Leakage Power

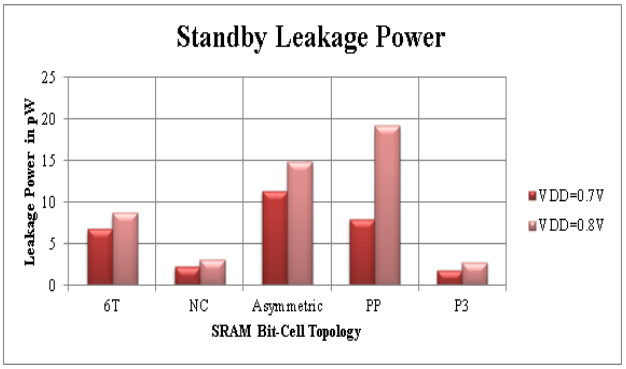

Fig 2: Standby Leakage Power

The standby leakage power analysis carried out on 6T SRAM, NC SRAM, Asymmetric SRAM, P3 SRAM and PP SRAM

yields the result shown in figure 2. It can be seen from the figure that P3 SRAM consumes least power when compared to the others with NC SRAM consuming slightly more power than P3 SRAM, whereas the rest consume significantly more power.

5.2. Dynamic Power

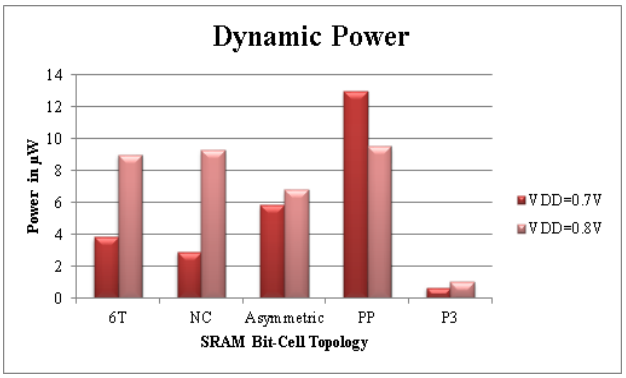

Fig 3: Dynamic Power

From the dynamic power analysis carried out on 6T SRAM, NC SRAM, Asymmetric SRAM, P3 SRAM and PP SRAM shown in figure 3, it can be seen that P3 SRAM consumes considerably less dynamic power than the rest. However, PP SRAM consumes the maximum amount of dynamic power.

5.3. Stability

The stability analysis carried out on 6T SRAM, NC SRAM, Asymmetric SRAM, P3 SRAM and PP SRAM gives the result shown in figure 4and figure 5.

5.3.1 Static Voltage Noise Margin

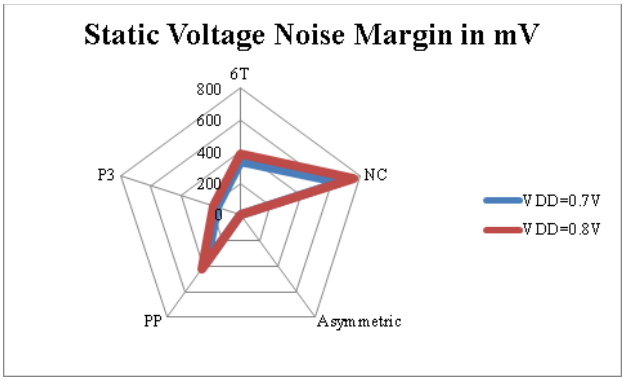

Fig 4: Static Voltage Noise Margin analysis

From figure 4, it becomes clear that the static voltage noise margin of P3 SRAM is higher than Asymmetric SRAM. However, it is low when compared to NC, 6T and PP SRAM.

5.3.2 Write Trip Voltage

From figure 5, it can be observed that the write trip voltage of Asymmetric SRAM is least among all five SRAMs. The write trip voltage of P3 SRAM is higher than NC and Asymmetric SRAM, but significantly less when compared to 6T and PP SRAM.

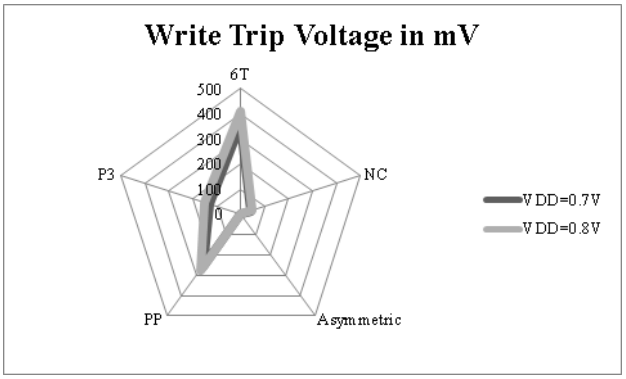

Fig 5: Write Trip Voltage Analysis

6. CONCLUSIONS

In this paper we have analysed 6T-SRAM, NC-SRAM, Asymmetric SRAM, PP-SRAM and P3- SRAM. The analysis has been based upon Power and Stability parameters of SRAM, such as Standby power, Dynamic power, Static Voltage Noise Margin(SVNM) and Write trip Voltage(WTV). With the help of these parameters, the power consumption and stability of each SRAM has been compared.

At V_{DD}=0.7V, P3-SRAM consumes 73.07%, 16.789%, 84.05% and 77.16% less standby power than 6T-SRAM, NC-SRAM, Asymmetric SRAM and PP-SRAM, respectively. Furthermore, at V_{DD}=0.8V, P3-SRAM consumes 69.069%, 13.61%, 82.03% and 86.11% less standby power than 6T-SRAM, NC-SRAM, Asymmetric SRAM and PP-SRAM, respectively.

At V_{DD}=0.7V, the dynamic power consumed by P3-SRAM is 82.77%, 77.158%, 88.72% and 94.95% less than 6T-SRAM, NC-SRAM, Asymmetric SRAM and PP-SRAM, respectively. Additionally, at V_{DD}=0.8V, the dynamic power consumed by P3-SRAM is 88.88%, 89.23%, 85.25% and 89.5% less than 6T-SRAM, NC-SRAM, Asymmetric SRAM and PP-SRAM, respectively.

Therefore, it has been observed that the P3-SRAM consumes less power compared to 6T-SRAM, NC-SRAM, Asymmetric SRAM and PP-SRAM. It has also been observed that the stability of P3-SRAM is poor as compared to 6T-SRAM and PP-SRAM.

7. ACKNOWLEDGEMENTS

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