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A High-Speed, Low-Power Phase Frequency Detector and Charge-Pump Circuits for High Frequency Phase-Locked Loops*

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SUMMARY In this paper, we introduce a high-speed and low-power Phase-Frequency Detector (PFD) that is designed using a modified TSPC (True Single-Phase Clock) positive edge triggered D flip-flop . The proposed PFD has a simple structure with using only 19 transistors. The operation range of this PFD is over 1.4 GHz without using additional prescaler circuits. Furthermore, the PFD has a dead zone less than 0.01ns in the phase characteristics and has low phase sensitivity errors. The phase and frequency error detection range is not limited as in the case of the pt-type and nc-type PFDs [3]. Also, the PFD is independent of the duty cycle of input signals. Also, a new charge-pump circuit is presented that is based on a charge-amplifier. A stand-by current of the proposed charge-pump circuit enhances the speed of charge-pump and removes the charge sharing which causes a phase noise in the charge pump PLL. Furthermore, the effect of clock feedthrough is reduced by separating the output stage from up and down signal. The simulation results base on a third order PLL are presented to verify the lock in process with the proposed PFD and charge pump circuits. The proposed PFD and charge-pump circuits are designed using 0.8 μm CMOS technology with 5 V supply voltage.

key words: *PFD, charge-pump, low-power, PLL, high-speed, D flip-flop, error detection range*

1. Introduction

The input phase errors are detected by Phase - Detector (PD) or Phase Frequency Detector (PFD). These errors, phase or frequency errors, are converted into current or voltage to control the output frequency of Voltage Controlled Oscillator (VCO) by charge pump in a charge pump PLL. PD detects a phase error between the reference signal and the output signal of PLL. Thus, the error detection range can be extended with PFD. A conventional CMOS PFD [1] is shown in Fig. 1. The PFD has a large dead zone in phase characteristics at the steady state which generates a large jitter in locked state in PLL. Furthermore, a large amount of power consumption cannot be avoided in high frequency operations because internal nodes of PFD are not completely pull up or pull down. An additional prescaler circuits can be added to lower frequency of the input signals. However, as the division ratio increases, the steady state phase error will be increased. The pt-type [2],[8] and the nc-type PFDs [3] are shown in Fig. 2. The pt-type PFD (Fig. 2 (b)) has a very high speed, but dead zone exists. A nc-type PFD (Fig. 2 (a)) has no dead-zone. The capture range of PLL is determined by the error detection range of PFD. A conventional CMOS PFD [1] has no limit to the error detection range. Therefore, the capture range of PLL is only limited by the Voltage Controlled Oscillator (VCO) output frequency range [5].

However, the error detection ranges of pt-type and nc-type PFDs are limited to $-\pi$ - $+\pi$. So the capture range of PLL with these PFDs is only limited by input

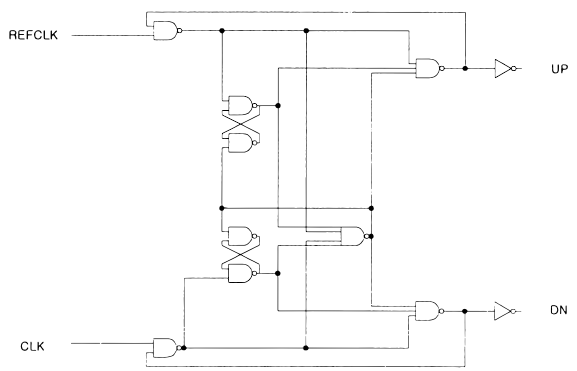

Fig. 1 A conventional CMOS PFD [1].

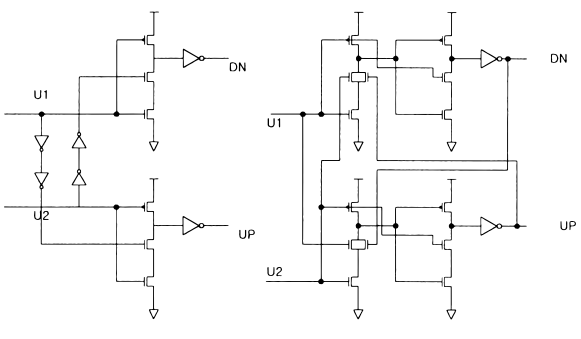

Fig. 2 Circuit schematic of dynamic PFDs [2],[3].

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reference signals.

In [4], the PFD and charge-pump circuits provide a transfer function of input phase error to the output charge per clock cycle. Whenever UP and DOWN signals are switching, a conventional tri-state charge-pump [1] has problems such as charge sharing in high-impedance state, charge injection and clock feedthrough [5]. The clock feedthrough and charge-sharing introduce a step phase noise to a charge pump PLL.

We propose a high-speed and low-power sequential type high speed and low power PFD circuit based on a modified TSPC positive edge triggered D flip-flop whose phase and frequency error detection range is not limited. Furthermore, we present a new charge-pump circuit which is designed using a current-amplifier. The proposed charge-pump not only reduces the effects of clock feedthrough and a charge-sharing but also the response speed is enhanced by the stand-by current.

This paper is organized as follows. The proposed high speed and low power positive edge triggered D flip-flops are presented in Sect. 2. In Sects. 3 and 4, two types of PFD circuits and current amplifier type charge-pump circuit are proposed. The phase and frequency characteristics of proposed PFDs and charge-pump circuit are presented, and comparisons are made in Sect. 5. In Sect. 6, a third-order PLL is designed to verify the lock-in properties of the proposed PFD and charge-pump circuits. Section 7 will draw a conclusion.

2. Design of Positive Edge Triggered D Flip-Flop for High Speed PFD Circuit

Circuit schematic of the proposed D flip-flops are shown in Fig. 3. These flip-flops modify the TSPC flip-flop [7] to satisfy the required function of D flip-flop for PFD. The operation of the proposed D flip flop is as follows. When input clock and reset signals are low, node A is connected to VDD through m1, mr1 and charges the node A to VDD. At the rising edge of the clock signal, node B is connected to ground through m3 and m4. Once the node A is charged to VDD, the node B is not affected by input clock signal. Because the charges at node the A turn off the m3 and this prevents the node B from being pulled up. Therefore, the node B is disconnected from input node. When the reset signal is applied, node A is disconnected from VDD by mr1 and is connected to ground by mr2. As soon as the node A is discharged, the node B is pulled up through m2. The mr1 is added to prevent the short circuit that occurrs whenever the reset signal is applied. When the clock signal is low while the reset signal is high, a current path is made from VDD to ground if mr1 is not provided. This increases the short circuit power consumption. Moreover, the reset time is increased because m1 charges the node A to VDD while the mr2 discharges node A to ground. Discharging node A quickly means the fast reset operation. The operation of D flip-flop in Fig. 3a is same as one of the D flip-flops in Fig. 3b, but their connection is different. Therefore, the transitoin delay of the two types of D flip-flops are almost same. Dynamic power consumption can be reduced by lowering the internal switching and speed is increased by shortening the input to output path.

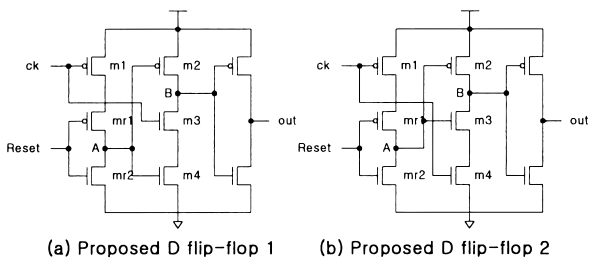


Fig. 3 A circuit schematic of the proposed D flip-flops.

3. Design of Phase Frequency Detector Circuits

Full schematics of the proposed PFDs are shown in Fig. 4. In Fig. 4., the proposed D flip-flops are used as a positive edge triggered D flip-flop. The proposed PFD type 1(Fig. 4 (a)) has a same phase error detection range as pt-type and nc-type PFDs. This structure detects phase errors within $-\pi$ - $+\pi$ between the input signals. The operation of the PFD is shown in Fig. 5 using input clock signals.

If the U1(resp. U2) signal makes transition from low to high, UP(resp. DOWN) signal goes to high. As soon as the U2(resp. U1) signal goes to high, the U2 reset the F/F 1[resp. F/F 2]. The output of the other flip-flop cannot make transition to high state because U1 signal is asserted to reset input. The high speed operation is accomplished with the proposed PFD because the proposed PFD structure has no feedback network to reset the flip-flops in PFD. Moreover, the power consumption is reduced half from the dynamic PFDs such as pt-type or nc-type because the switching of the PFD is occurred only in one flip-flop.

In order to extend the phase error detection range,

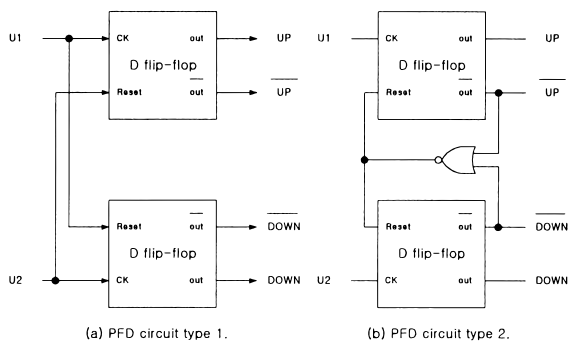


Fig. 4 Schematics of the proposed PFDs.

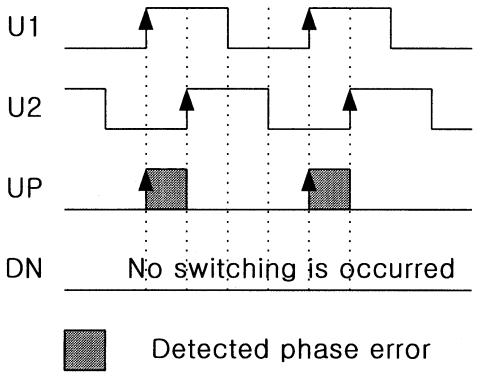


Fig. 5 The operation of the proposed PFD.

Table 1 Comparison of PFDs.

PFD type	Dynamic power	Number of Transistors	Detection range	Dead zone
Proposed type 1	3.6 mW	16	$-\pi$ -$+\pi$	< 20ps
Proposed type 2	7.8 mW	19	-2π- $+2\pi$	< 50ps
pt-type 1	10.8 mW	18	$-\pi$-$+\pi$	< 200ps
nc-type 1	11 mW	19	$-\pi$-$+\pi$	-
Static CMOS PFD	15 mW	48	-2π-$+2\pi$	< 400ps

the proposed PFD type 2 (Fig. 4 (b)) uses a conventional sequential type PFD structure. For the purpose of high-speed operation, a small size of PMOS pseudo-NOR gate can be used at the feedback network. The comparisons of PFDs are shown in Table 1.

The dynamic power consumption and the number of transistors of the proposed PFD type 2 are similar to the high speed dynamic PFDs. However, since the proposed PFD uses the pseudo-NOR gate at the feedback network, a little more input dependent power consumes than the dynamic PFD circuists.

4. Design of the Charge-Pump Circuit

The block diagram of the proposed charge-pump circuit is shown in Fig. 6. The charge pump consists of current amplifier with stand-by current and switched current sources. The operation of the proposed charge-pump is similar to the conventional tri-state charge-pump [2]. No output current is generated when the input signals are in the same state. The output current is generated only when the input signals are in different state. However, the current control switch is not connected directly to the output stage in order to reduce the effect of clock feedthrough which causes the step phase-jump error whenever the UP/DN signals make transition. The stand-by current sources are added to the input of the charge-pump to enhance the response speed of charge-pump, because the transistors at output stage are always turn on and passes the little current from VDD to ground. This makes the charge-pump possible to operate more higher speed. Also, the stand-by current eliminates high impedance state in the tri-state charge-

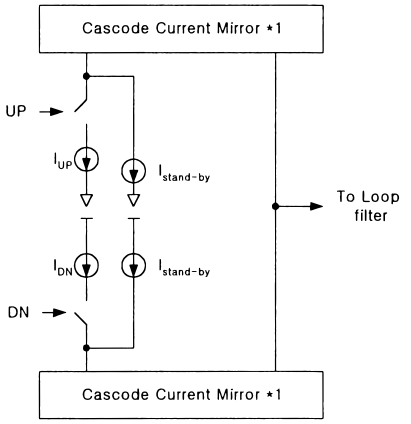


Fig. 6 Block diagram of our charge-pump.

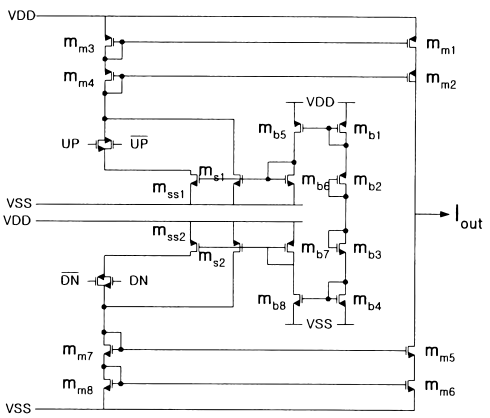


Fig. 7 Detailed circuit schematic of our charge-pump.

Table 2 Characteristics of the proposed charge-pump.

Input condition UP — DN	Output current	Power consumption
0 — 0	-70nA	0.198 mW
0 — 1	-157.05uA	1.376 mW
1 — 0	157uA	1.3801 mW
1 — 1	45nA	2.55 mW

pump which causes a charge sharing problem. The output current of the proposed charge-pump is same as the conventional tri-state charge-pump. The stand-by current does not affect the output current, but enhances the speed of charge-pump.

The detailed circuit schematic of the proposed charge-pump is shown in Fig. 7. The transistors, mb1-mb8, are the bias circuit for stand-by current sources (ms1,ms2) and switched-current sources (mss1,mss2). The switch is implemented using transmission gate to reduce clock feedthrough. And the current mismatch caused by path delay mismatch between UP and DOWN signal can be reduced. The cascode current sources are used to increase the output impedance.

To concern with the power consumption, an additional stand-by current consumes more static power

than the conventional tri-state charge-pump circuit at off-state about 112.5uW with 5 V supply voltage. The output currents, stand-by currents and dynamic power consumptions of the proposed charge-pump (as a function of input conditions) are shown in Table 2.

5. Phase Characteristics of the Proposed PFD and Charge-Pump Circuit

Figure 8 shows the phase characteristics of our PFD (type-2) compared with the other dynamic PFDs. The pt-type PFD has a 0.18ns dead zone. In case of nc-type PFD, it has no dead zone but the phase characteristics of PFD depends on the duty cycle of the input signals. Also, the nc-type PFD has a constant offset in phase characteristics. The nc-block of the nc-type PFD and D flip-flop of the pt-type PFD are controlled by both input signals while the proposed PFD does not depend on other input signals. Therefore, the phase sensitivity error caused by input signal dependence is reduced.

Phase sensitivity errors of pt-type PFD, nc-type PFD and our PFD are shown in Fig. 9. Phase sensitivity errors are reduced to less than 0.02ns using our PFD.

The nc-type PFD has various phase offsets caused by the duty cycle of input signals. The pt-type PFD has similar phase characteristic to the proposed PFD. However, since the flip-flops are controlled by both input signals, the output signal is dependent on the state of input signals. This increases the phase sensitivity error.

Setup and reset delay of the proposed PFDs as a function of supply voltage are shown in Fig. 10. The setup delay of proposed PFDs are same, because setup time is same as one of the D flip-flop. The setup delay varies from 0.1ns up to 0.25ns when supply voltage decreases from 5 V to 2 V. In case of the reset delay, there is a slight difference between two type of PFDs. The reset delay of the PFD type-1 is same as the reset time of D flip-flop. However, the reset delay of the proposed PFD type-2 reset two flip-flops via the feedback network. The speed of PMOS pseudo-NOR gate decreases significantly as the supply voltage decreases. This makes the reset time of PFD type-2 much longer than that of the PFD type-1. The reset delay of the PFD type-1 is 0.479ns while the PFD type-2 is 1.45ns with 2 V supply voltage.

Figure 11 shows the simulated transfer function of the PFD and charge-pump as a function of input phase difference. The input phase difference is applied to the

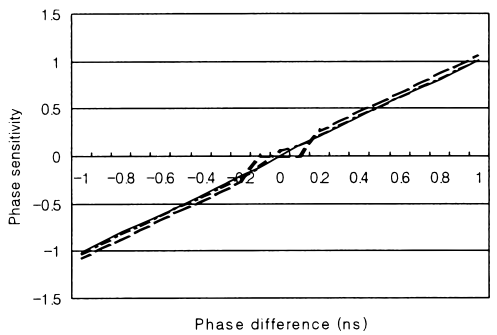


Fig. 8 Phase characteristics of the pt-type PFD (long dashed-line), and nc-type PFD (short dashed-line), and our PFD (type-2) (solid line).

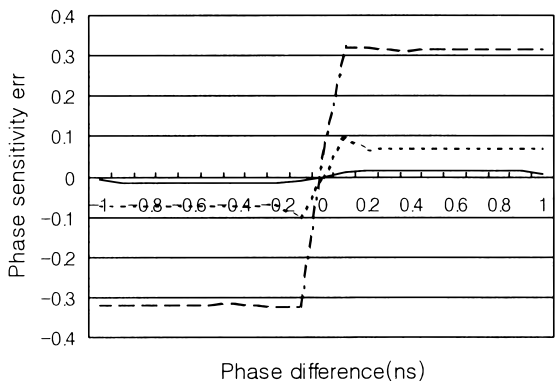


Fig. 9 Phase sensitivity error of the pt-type PFD (short dashed-line), and nc-type PFD (long dashed-line), and proposed PFD (solid line).

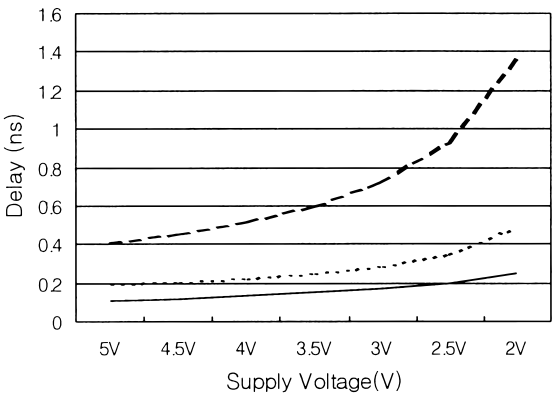


Fig. 10 Setup delay (solid line PFD type 1 and type 2) and reset delay of proposed PFD (PFD type 1 : short dashed line, PFD type 2 : short dashed line) as a function of supply voltage.

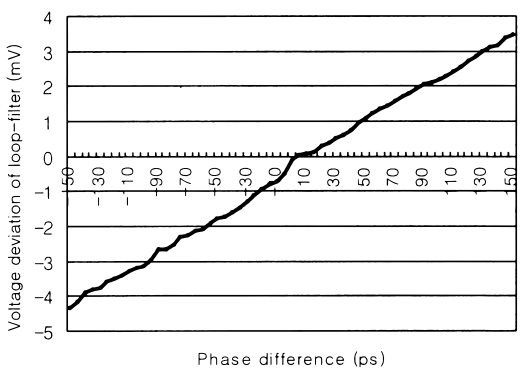


Fig. 11 PFD and charge-pump gain.

PFD with a 5ps step. The output voltage diviations of the loop-filter are measured. The gain of PFD and charge-pump is 150uA/ps and the gain from PFD to loop-filter is 0.0232 mV/ps.

6. Verification of PFD and Charge-Pump with a Third-Order PLL

In order to verify the lock in properties of the proposed PFD and charge pump, a complete third-order charge-pump PLL was designed. Figure 12 shows the block diagram of a third-order PLL. The PLL block is composed of PFD, charge-pump, loop-filter and VCO.

As an external reference clock generator circuit, the same VCO circuit as is in the PLL core is used. And this method makes it easy to apply step input frequency to the PLL. Also, in order to verify the speed of the proposed PFD and charge-pump circuits, high frequency input and output of the VCO is applied to the PFD circuit without additional prescaler circuits. A simple 2-pole and 1-zero RC loop filter is used to reduce the steady state phase error in locked state when the step input is applied to the PLL [2].

The circuit schematic of VCO [6] is shown in Fig. 13. The VCO circuit is composed of 5 stage delay-cell and voltage level shifter to control the output frequency of VCO circuit. However, because of the negative Vc-Fo characteristics of the VCO, the connection of the output signals of the PFD(UP and DOWN signal) to charge-pump has been changed to compensate the negative gain of VCO.

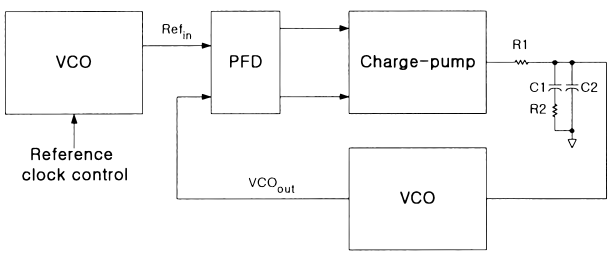


Fig. 12 Block diagram of a third-order PLL.

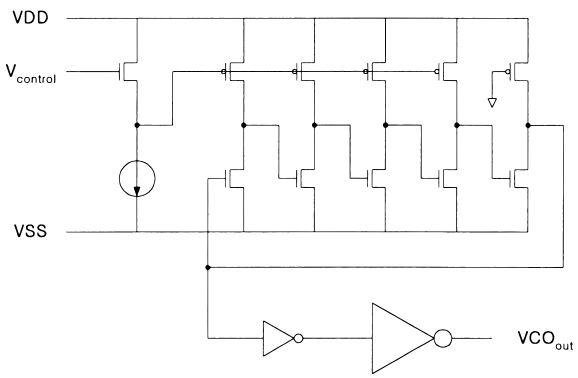


Fig. 13 Circuit schematic of VCO [6].

The key parameters of PLL block is summarized in Table 3.

A third-order PLL based simulation results are shown in Fig. 14. The reference clock generator is controlled by the external voltage(Vref, dashed straight line). Various frequency steps are applied to the PLL to verify the lock in properties of a third-order PLL. At the initial state, the VCO in PLL core is tuned to oscillated at 1.05 GHz, then 855 MHz input reference is applied to PLL. When the external clock signal is applied to the PLL, the PLL is locked at 855 MHz after 240ns. After the output frequency of PLL is settled at 855 MHz, then 155 MHz, 305 MHz, 442 MHz and 571 MHz frequency step is applied to the PLL respec-

Table 3 Characteristics of the proposed charge-pump.

Key parameters	Values
VCO output range	Max : 1.62\,GHz @ 2\,V Min : 497\,MHz @ 4\,V
VCO gain	-561.5\,MHz / V
R1	8K
R2	1K
C1	10pF
C2	2pF

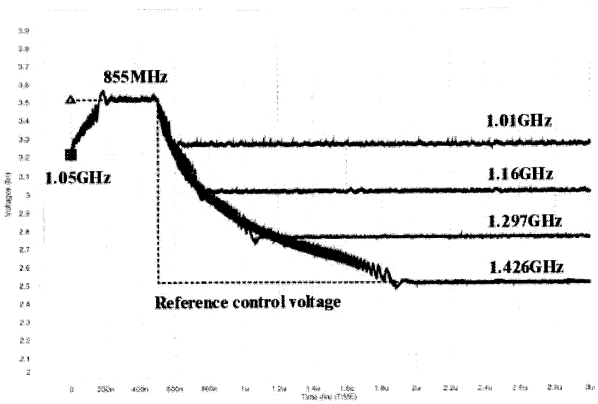


Fig. 14 Response of a third-order PLL for various input reference step variation.

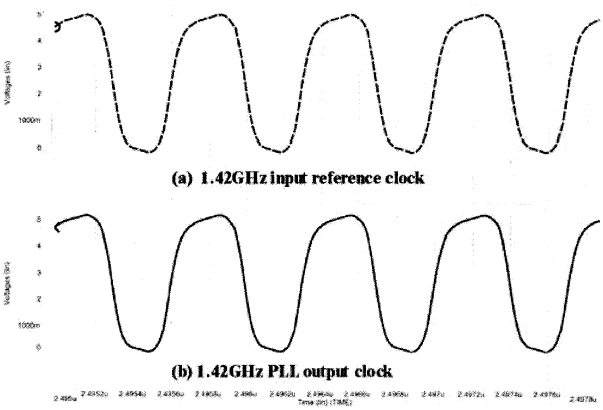


Fig. 15 1.426 GHz input reference and PLL output clocks.

Table 4 Final state phase error and lock-time.

Frequency step	Max. phase error	operating frequency	lock-time
155Mhz	+38ps	1.01 GHz	250ns
305Mhz	+11.4ps	1.16 GHz	420ns
422Mhz	+28.1ps	1.297 GHz	780ns
571Mhz	+11.5ps	1.426 GHz	1.65us

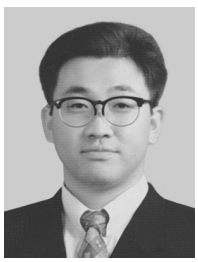
tively. The 1.426 GHz Input reference and PLL output clocks are shown in Fig. 15. Also, the final state conditions are summarized in Table 4.

7. Conclusions

For designing high-speed and low-power CMOS PLL, we proposed a new dynamic CMOS positive edge triggered D flip-flop for PFD and current amplifier charge-pump circuit. Two types of PFD circuits are presented. The proposed half range PFD (type-1) circuit, whose phase error detection range is $-\pi$ - $+\pi$, is surperior to dynamic PFD circuits such as pt-type and nc-type PFD in power consumption and speed. Whereas, the proposed full range PFD (type-2) circuit extends its phase error detection range just modifying the structure as conventional sequential type PFD. Dead zone of the proposed PFD is less than 0.01ns and error detection range is not limited as in PFD type 2. The speed of the charge-pump is enhanced by adding standby current. A spice simulation results based on a third-order PLL indicates that the proposed PFD and charge-pump circuits operate over 1.426 GHz without additional prescaler circuits in 0.8 μm CMOS with 5 V supply voltage. The steady state phase errors are measured less than 12ps and jitter is reduced to 15ps at 1.426 GHz input reference. The proposed dynamic CMOS PFD and charge amplifier type charge pump circuits can be used in high frequency region over 1.4 GHz with precise and fast lock in process.

References

[1] R.E. Best, Phase Locked Loops, 2nd ed., McGraw Hill, New York, 1993.
[2] H. Kondoh, H. Notani, T. Yoshimura, and Y. Matsuda, "A 1.5-V 250-MHz to 3.3-V 622Mhz CMOS phase locked loop with precharge type CMOS phase detector," IEICE Trans. Electron., vol.E78-C, no.4, pp.381–338, April 1995.
[3] H.O. Johansson, "A simple precharged CMOS phase frequency detector," IEEE J. Solid State Circuits, vol.33, no.2, pp.295–259, Feb. 1998.
[4] I.A. Young, J.K. Greason, and K.L. Wong, "A PLL clock generator with 5 to 110 MHz of lock range for microprocessors," IEEE J. Solid State Circuits, vol.SC 27, pp.1559–1607, Nov. 1992.
[5] B. Razavi, "Monolithic phase-locked loops and clock recovery circuits," Theory and Design, IEEE Press.
[6] M. Banu and A. Dunlop, "A 660 Mb/s CMOS clock recovery circuit with instantaneous locking for NRZ data and burst mode transmission," ISSCC Dig. Tech. Papers, pp.102–103, Feb. 1993.
[7] J.M. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice Hall, 1993.
[8] H. Yoshizawa, K. Taniguchi, H. Shirahama, and K. Nakashi, "A low power 622 MHz CMOS phase locked loop with source coupled VCO and dynamic PFD," IEICE Trans. Fundamentals, vol.E80-A, no.6, pp.1015–1020, June 1997.



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