FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm

Digh Hisamoto, *Member, IEEE*, Wen-Chin Lee, Jakub Kedzierski, Hideki Takeuchi, Kazuya Asano, *Member, IEEE*, Charles Kuo, Erik Anderson, Tsu-Jae King, Jeffrey Bokor, *Fellow, IEEE*, and Chenming Hu, *Fellow, IEEE*

***Abstract*—MOSFETs with gate length down to 17 nm are reported. To suppress the short channel effect, a novel self-aligned double-gate MOSFET, FinFET, is proposed. By using boron-doped $Si_{0.4}Ge_{0.6}$ as a gate material, the desired threshold voltage was achieved for the ultrathin body device. The quasiplanar nature of this new variant of the vertical double-gate MOSFETs can be fabricated relatively easily using the conventional planar MOSFET process technologies.**

***Index Terms*—Fully depleted SOI, MOSFET, poly SiGe, short-channel effect.**

I. Introduction

TO DEVELOP sub-50-nm MOSFETs, the double-gate structure has been widely studied. This is because for conventional bulk MOSFETs, the high concentration punch-through stopper ($>10^{18}$ cm^{-3}) is indispensable but results in severe drivability and leakage degradation. For the double-gate SOI-MOSFETs, the gates control the energy barrier between the source and drain effectively. Therefore, the short channel effects can be suppressed without increasing the channel impurity concentration [1]–[5].

However, former studies found that the ultrathin body devices have peculiar problems, such as parasitic resistance or threshold voltage controllability [6]–[8]. Furthermore, the complexity of the fabrication process has been a severe problem of double-gate structures. This is because the Si-planar technology is not suitable to form the gate-channel-gate stacked structure that the double-gate device demands. New ideas are sorely needed.

In view of the above problems, we recently proposed a new self-aligned double-gate MOSFET structure. Based on the DELTA structure [10], after reduction of the vertical feature height, the gate-channel-gate stacked structure is realized by a quasi planar technology. In this paper, the fabrication process and the device characteristics in the sub-50 nm gate-length region are presented. We demonstrate the feasibility of the new device structure named FinFET.

Manuscript received June 28, 1999; revised February 1, 2000. This work was sponsored by DARPA AME Program under Contract N66001-97-1-8910. The review of this paper was arranged by Editor C. Y. Yang.

D. Hisamoto is with the Central Research Laboratory, Hitachi Ltd., Tokyo 185-8601, Japan (e-mail: hisamoto@crl.hitachi.co.jp).

W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, T.-J. King, J. Bokor, and C. Hu are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA.

E. Anderson is with the X-ray Optics, Lawrence Berkeley National Laboratory, Berkeley, CA USA.

Publisher Item Identifier S 0018-9383(00)10393-4.

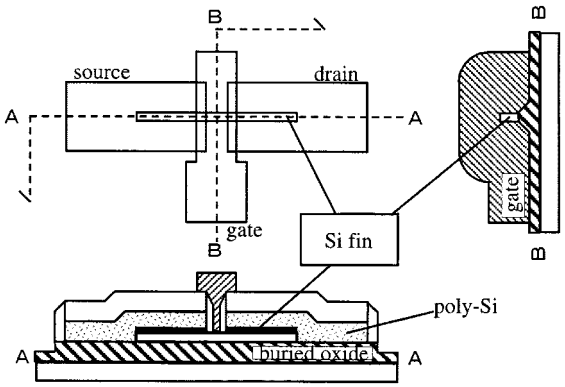

Fig. 1. FinFET typical layout and schematic cross sectional structures.

II. Device Fabrication

The device structure of the FinFET is shown in Fig. 1. As DELTA, the channel was formed on the side "vertical" surface of the Si-fin, and the current flows in parallel to the wafer surface. The device used the elevated S/D process first applied on DELTA [11]. The heart of the FinFET is a thin ($\sim$10 nm) Si fin, which serves as body of the MOSFET. A heavily-doped poly-Si film wraps around the fin and makes electrical contact to the vertical faces of the fin. The poly-Si film greatly reduces the S/D series resistance and provide a convenient means for local interconnect and making connections to the metal. A gap is etched through the poly-Si film to separate the source and drain. The width of this gap, further reduced by the dielectric spacers determines the gate length. The channel width is basically twice the fin height (plus the fin width). The conducting channel is wrapped around the surface of the fin. Hence the name—FinFET. Because the S/D and gate are much thicker (taller) than the fin, the device structure is quasiplanar.

Fig. 2 shows the process flow and Fig. 3 shows the SEM pictures at two fabrication step 2 and step 4. The starting material is a SOI wafer with a 400-nm thick buried oxide layer and 50-nm thick silicon film. The measured standard deviation of the silicon film thickness is around 20 A. Although the silicon film thickness determines the channel width, the variation is acceptable for the device uniformity. The variation in the gate length will be a larger source of process variation.

The CVD Si_3N_4 and SiO_2 stack layer is deposited on the silicon film to make a hard mask or cover layer. The cover layer will protect the Si-fin through the fabrication process steps. The fine Si-fin is patterned by electron beam (EB) lithography with 100 keV acceleration energy. The resist pattern is slightly ashed at 5 W and 30 sec to reduce the Si-fin width. Then, using top

0018–9383/00$10.00 © 2000 IEEE

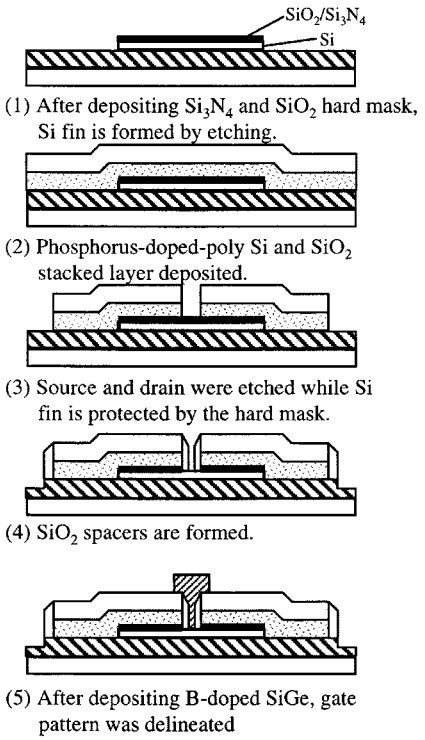

Fig. 2. FinFET fabrication process flow.

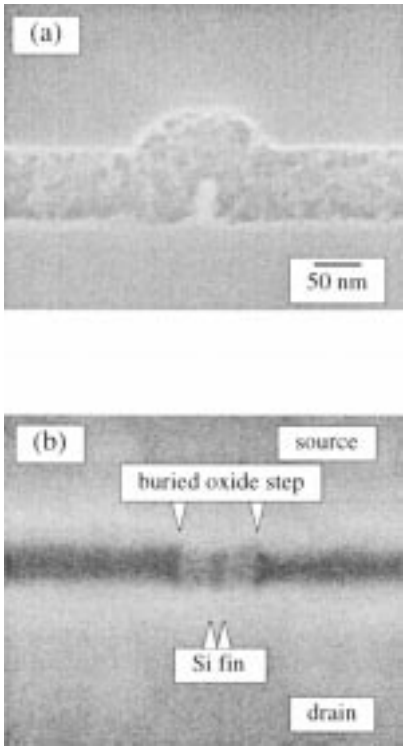

Fig. 3. (a) Cross-sectional SEM picture of 15-nm Si vertical fin. The height is 50 nm. (b) Top view of channel region after spacer etching. The spacer gap between source and drain is 50 nm.

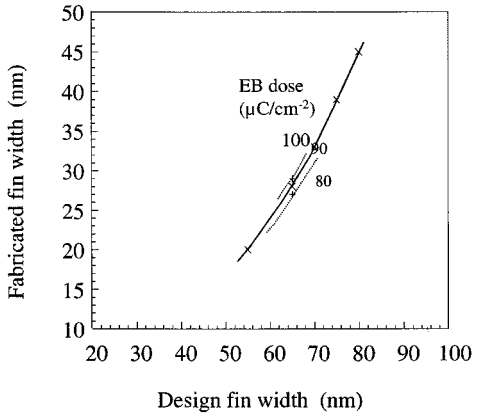

Fig. 4. Relationship between design Si-fin width practical size with EB dose as a parameter.

SiO_2 layer as a hard etching mask, the SOI layer is etched. The Si is exposed only at the sides of the Si-fin as shown in Fig. 2(1). Fig. 4 shows the fabricated Si-fin width versus the design size with the EB dose as a parameter. Fine Si-fins down to 20 nm are obtained. The final Si-fin ($\sim$10 nm) width are smaller than the value in Fig. 4 because of thinning during later dry etching and gate oxidation processes.

In-situ phosphorus-doped-amorphous Si (for S/D pads) is deposited at 480 °C. To suppress the native oxide growth on the Si-fin side surfaces, the wafers are loaded at 300 °C. After α-Si deposition, SiO_2 is deposited at 450 °C. The process temperatures are low enough to suppress impurity diffusion into the Si-fin. The cross sectional SEM picture of Fig. 3(a) shows that the 15-nm width and 50-nm height of a Si-fin, which is covered by phosphorus-doped Si.

Using EB lithography, the S/D pads with a narrow gap in between them are delineated. The SiO_2 and amorphous Si layers are etched and the gap between the S/D pads is formed [Fig. 2(3)]. While the cover layer protects the Si-fin, the amorphous Si is completely removed from the side of the Si-fin. The amorphous Si in contact to with the Si-fin at its side surfaces becomes the impurity diffusion source that forms the transistor S/D later. Fig. 5 shows the simulated current density distribution in the Si-fin and pad region of FinFET. By using the two-dimensional (2-D) device simulator, the behavior of electrons and holes was calculated. The current density contour shows that the current quickly spreads into the pads. This suggests that the parasitic resistance is reduced.

CVD SiO_2 is deposited to make spacers around the S/D pads. The height of the Si fin is 50 nm, and the total S/D pads thickness is 400 nm. Making use of the difference in the heights, the SiO_2 spacer on the sides of the Si-fin is completely removed by sufficient over etching of SiO_2 while the cover layer protects the Si-fin. The Si surface is exposed on the sides of the Si-fin again [Fig. 2(4)]. During this over etching, SiO_2 on the S/D pads and the buried oxide are etched. By measuring the buried oxide thickness, we confirmed the amount of the etched SiO_2. The top-view SEM picture of Fig. 3(b) shows a 15-nm thin Si fin located in a 50-nm gap between the light oxide spaces. This gap determines the gate length. A brief summary of the typical sizes: 100 nm gap between the S/D pads, 40 nm spacer length, and 20 nm gate length. From the top-view SEM picture at this process step, the gate length and Si-fin width are measured and they are the values reported in this paper. Because 1:20 HF and 7 sec dip is used to clean the Si surface before gate oxidation, the gate length is slightly ($\sim$1 nm) larger than the measured gap width.

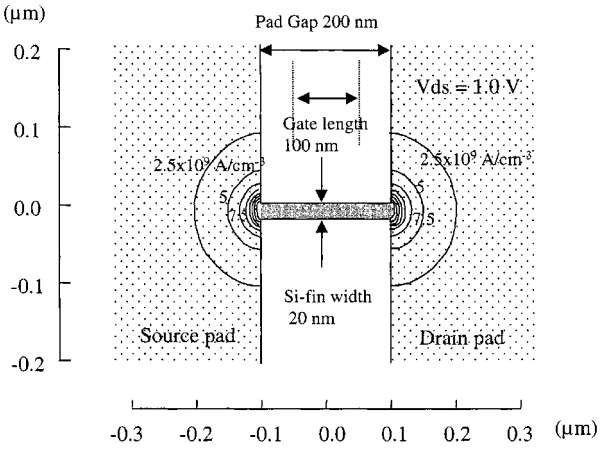

Fig. 5. Simulated current density contours in the poly-Si S/D pads. The fast spread of the current indicate effective reduction of the series resistance.

Also, the gate oxidation should thin the Si-fin width slightly. Notice that the channel width of the devices is twice the height of the Si-fins or approximately 100 nm.

By oxidizing the Si surface, gate oxide as thin as 2.5 nm is grown. Because the area of Si-fin side surface is too small, we use dummy wafers to measure the oxide thickness with ellipsometry. During gate oxidation, the amorphous Si of the S/D pads is crystallized. Also, phosphorus diffuses from the S/D pads into the Si-fin and forms the S/D extensions under the oxide spacers. Then, boron-doped $Si_{0.4}Ge_{0.6}$ is deposited at 475 °C as the gate material. Because the source and drain extension is already formed and covered by thick SiO_2 layer, no high temperature steps are required after gate deposition. Therefore, the structure is suitable to use with new high k gate dielectric and metal gates that are not compatible with each other under high temperature.

After delineating the gate electrode [Fig. 2(5)], the probing windows are etched through the oxide. We directly probe on the poly-Si and poly-SiGe pads, with no metallization used in this experiment. The total parasitic resistance due to probing is about 3000 Ω.

III. Experimental Results and Discussion

A. Device Characteristics with Sub-30-nm Gate Length

The typical current–voltage (*I–V*) characteristics of a 30-nm gate length device are shown in Fig. 6. In spite of the low channel impurity concentration (2×10^{16}cm^{-3}), the subthreshold leakage current is well suppressed. In the saturation region, no kink effect due to the floating body effect is observed. This is as expected for a device having an ultrathin floating body. The small saturation current was observed. We considered that the bad Si-SiO_2 interface condition resulted in the value because sacrificial gate oxidation was not used after the dry etching. To study the DIBL effect, the channel current dependence on the drain bias is measured for the 30-nm gate length device with the Si-fin width as a parameter (Fig. 7). V_{gs} values are chosen so that of $I_{ds} = 10^{-11}, 10^{-10}, 10^{-9}$, and 10^{-8} A at $V_{ds} = 0.05$ V. Device with a larger Si-fin width show a larger rise of I_{ds} or decrease of V_t with rising V_{ds}, i.e., a stronger DIBL effect. It appears that a Si-fin width just smaller than the gate length may be sufficiently small to suppress DIBL.

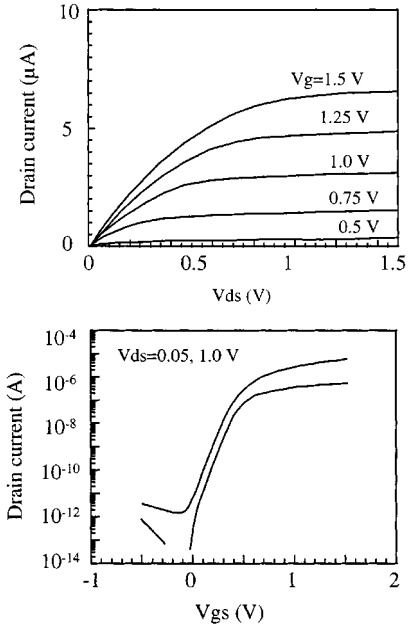

Fig. 6. Device characteristics of FinFET with 30-nm gate length and 20-nm Si-fin width, (a) I_d–V_{ds} and (b) I_d–V_{gs}.

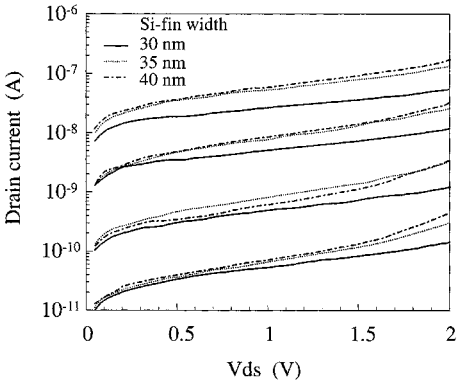

Fig. 7. Drain bias dependence of subthreshold current for gate length of 30 nm with the Si-fin width as a parameter. V_{gs} are chosen so that $I_{ds} \sim 10^{-8}, 10^{-9}, 10^{-10}$, and 10^{-11} A at $V_{ds} = 0.05$ V.

The roll-off characteristics of a 20-nm Si-fin width device are shown in Fig. 8. V_t is defined as the gate voltage when $I_{ds} = 10^{-10}$ A. Good roll-off characteristics are observed for the FinFET structure. The characteristics of the smallest device fabricated have a gate length of 17 nm. To our knowledge, this is the smallest gate length ever demonstrated for a MOSFET. The Si-fin width is 15 nm, and the channel doping is 10^{15} cm^{-3}. Fig. 9 shows the characteristics of this device. The subthreshold swing is relatively large due to the short channel effect. However, in spite of the very low channel concentration, the subthreshold leakage is effectively suppressed. Fig. 10 shows the subthreshold-swing dependence on the Si-fin width. Because the thin body of the double-gate device successfully prevents punch-through, the FinFETs show small swings even in 30 nm MOSFETs.

In Fig. 11, the transconductance (G_m) are plotted with the Si-fin width as a parameter. Interestingly, G_m peaks at 30-nm of

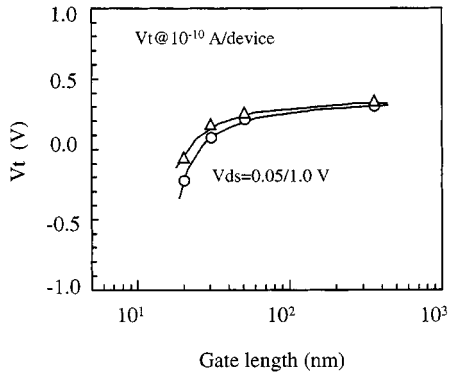

Fig. 8. Threshold voltage dependence on the gate length for Si-fin width of 20 nm.

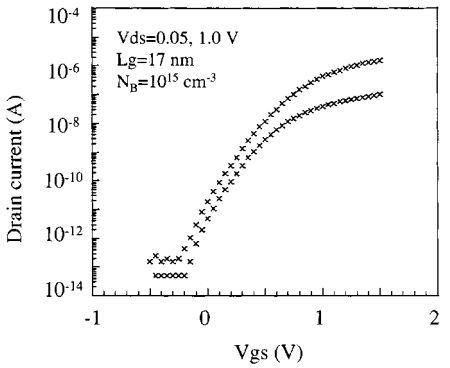

Fig. 9. Subthreshold leakage for the gate length of 17 nm is low even though the body doping density is only 10^{15} cm^{-3}.

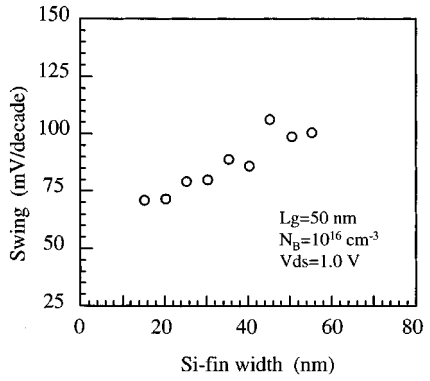

Fig. 10. Swing dependence on the Si-fin width and can be quite small.

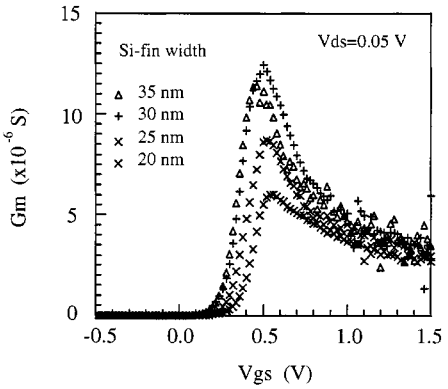

Fig. 11. Transconductance peaks when the Si-fin width is 30 nm.

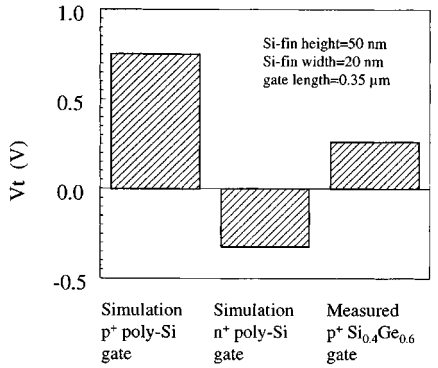

Fig. 12. Comparison of simulated device V_t with the measured V_t. Si-fin width is 20 nm, fin height is 50 nm, fin doping is 10^{16} cm^{-3}, and gate length is 350 nm.

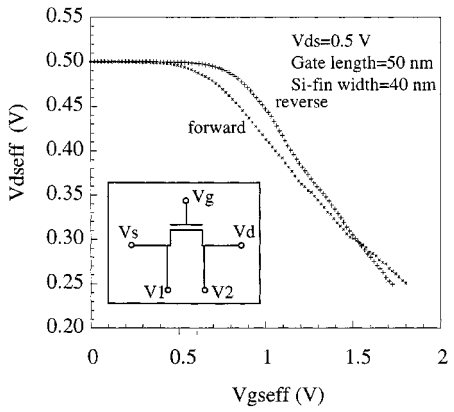

Fig. 13. Effective drain bias and gate bias dependence for gate length of 100 nm and Si-fin width of 30 nm.

Si-fin width. This is because that while a thinner body increases the parasitic resistance, it also can increase the mobility and reduce the charge centroid, resulting in an optimum Si fin width or body thickness.

B. Gate Engineering

To control the threshold voltage of ultrathin SOI-MOSFETs, the gate work function control is essential. This is because heavy body doping is not compatible with the fully-depleted body design which suppresses the floating body effect, improves mobility, and suppresses the dopant fluctuation effect. So far, many kinds of metal gate, such as TiN and Ta [8], [12] have been reported. However, because of the instability of metals, metal gate processes are not straightforward. FinFET uses SiGe with 60% Ge mole fraction as a gate material. The advantages of SiGe are the compatibility with poly-Si gate process and the continuous variability of the work function controlled with the Ge concentration [13].

The work function was confirmed by comparing the threshold voltage with the simulated V_t (Fig. 12). The quantum effect was taken into account in the simulations. A uniform channel impurity profile was assumed. Because the measured data is almost at the middle of the simulated V_t's, the work function of the gate is around mid-gap.

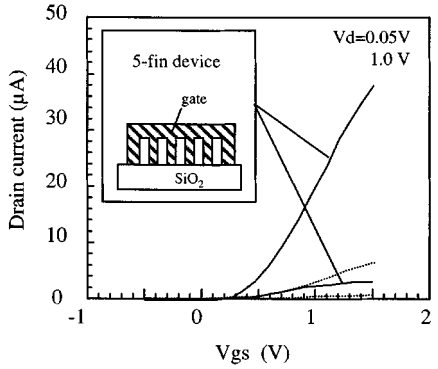

Fig. 14. Current drivability is proportional to the number of fins. The MOSFET channel width can be varied by increments of 0.1 μm.

C. Self-Aligned Gate to S/D

The double-gates of the FinFET are self-aligned to each other and to the S/D. Self-alignment is good for reducing the parasitic capacitance and resistance and for control of the channel length. To evaluate the self-alignment process, four terminal "Kelvin-type" devices as shown in the inset of Fig. 13 are formed. This is because the direct probing onto the poly-Si pads leads to large asymmetric parasitic resistances. The effective drain bias $(V_{\mathrm{ds\,eff}})$ and the effective gate bias $(V_{\mathrm{gs\,eff}})$ are

$$V_{\mathrm{ds\,eff}} = V_2 - V_1$$
$$V_{\mathrm{ds\,eff}} = V_g - V_1.$$

We measure the device characteristics at forward and reverse S/D setting. Fig. 13 shows the relationship between $V_{\mathrm{ds\,eff}}$ and $V_{\mathrm{gs\,eff}}$ for V_{gs} =0 to 2.0 V and $V_{\mathrm{ds}} = 0.5$ V. In spite of the reasonable sheet resistance (82 to 114 $\Omega/\square$) of the S/D pads, large bias degradations are observed. This means that the contact between the measuring probe and poly-Si pads has a large parasitic resistance. However, a good symmetry current drive with 6% difference between forward and reverse operations was observed, which indicates the good symmetry of the self-aligned source and drain.

The self-aligned process and the quasiplanar structure of the FinFETs are suitable to construct multifin transistor for larger channel width. This is because the S/D pads directly connect the adjacent fins. Multiple fin devices are fabricated and presented as shown in Fig. 14. The five-fin device conducts five times larger current than the single fin device. Although the channel width can be varied only by integer number of fins, the discrete increment is small (0.1 μm) in our design.

IV. Conclusion

A novel self-aligned double-gate SOI structure (FinFET) is proposed as a nanoCMOS device. In spite of its double-gate structure, FinFET is close to its root, the conventional MOSFET in terms of layout and fabrication. The result is a quasiplanar device. We experimentally demonstrated the following key features.

1) Self-aligned double-gate effectively suppresses short channel effects, even with 17-nm gate length.
2) $Si_{0.4}Ge_{0.6}$ gate provides a proper threshold voltage for ultrathin body MOSFET.
3) Gate is self-aligned to the S/D, which is raised to reduce the parasitic resistance.

This structure uses a S/D first, gate last process flow that may be needed for future high-k gate dielectric and metal gate. FinFET can be suitable integration of Si-ULSIs.

Acknowledgment

The authors wish to thank the staffs of the Microfabrication Laboratory, University of California, Berkeley, for their support in device fabrication.

References

[1] D. J. Frank, S. E. Laux, and M. V. Fischetti, "Monte carlo simulation of a 30 nm dual-gate MOSFET: How short can Si go?," in *IEDM Tech. Dig.*, 1992, pp. 553–556.
[2] C. Fiegna *et al.*, "A new scaling methodology for the 0.1–0.025 um MOSFET," in *VLSI Symp. Tech. Dig.*, 1993, pp. 33–34.
[3] K. Suzuki *et al.*, "Scaling theory for double-gate SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 40, pp. 2326–2329, 1993.
[4] H. S. Wong, D. J. Frank, Y. Taur, and J. M. C. Stork, "Design and performance considerations for sub-0.1 um double-gate SOI MOSFET's," in *IEDM Tech. Dig.*, 1994, pp. 747–750.
[5] B. Majkusiak, T. Janik, and J. Walczak, "Semiconductor thickness effects in the double-gate SOI MOSFET," *IEEE Trans. Electron Devices*, vol. 45, pp. 1127–1134, May 1998.
[6] L. T. Su, M. J. Sherony, H. Hu, J. E. Chung, and D. A. Antoniadis, "Optimization of series resistance in sub-0.2 um SOI MOSFETs," in *IEDM Tech. Dig.*, 1993, pp. 723–726.
[7] D. Hisamoto *et al.*, "Metallized ultra-shallow-junction device technology for sub-0.1 um gate MOSFET's," *IEEE Trans. Electron Devices*, vol. 41, pp. 745–750, May 1994.
[8] J. Hwang and G. Pollack, "Novel polysilicon/TiN stacked-gate structure for fully-depleted SOI/CMOS," *IEDM Tech. Dig.*, pp. 345–348, 1992.
[9] D. Hisamoto *et al.*, "A folded-channel MOSFET for deep-sub-tenth micron era," *IEDM Tech. Dig.*, pp. 1032–1034, 1998.
[10] D. Hisamoto, T. Kaga, and E. Takeda, "Impact of the vertical SOI 'Delta' structure on planar device technology," *IEEE Trans. Electron Devices*, vol. 38, pp. 1419–1424, 1991.
[11] S. Kimura, H. Noda, D. Hisamoto, and E. Takeda, "A 0.1 μm-gate elevated source and drain MOSFET fabricated by phase-shifted lithography," in *IEDM Tech. Dig.*, 1991, pp. 950–952.
[12] T. Ushiki *et al.*, "Reliable tantalum gate fully-depleted-SOI MOSFET's with 0.15 μm gate length by low-temperature processing below 500 C," in *IEDM Tech. Dig.*, 1996, pp. 117–120.
[13] T.-J. King, J. P. McVittie, K. C. Saraswat, and J. R. Pfiester, "Electrical properties of heavily doped polycrystalline silicon-germanium films," *IEEE Trans. Electron Devices*, vol. 41, pp. 228–232, Feb. 1994.

Digh Hisamoto (M'94) received the B.S. and M.S. degrees in reaction chemistry from the University of Tokyo, Tokyo, Japan, in 1984 and 1986, respectively.

In 1986, he joined Central Research Laboratory, Hitachi Ltd., Tokyo, where he has been working on ULSI device physics and process technologies. From 1997 to 1998, he was a Visiting Industrial Fellow at the University of California, Berkeley. His current research interests include thin-film SOI materials, short-channel MOSFETs, semiconductor memories, and Si RF devices.

Mr. Hisamoto is a member of the Japan Society of Applied Physics and the Institute of Electronics and Communication Engineers of Japan.

Wen-Chin Lee received the B.S. degree in electrical engineering from National Tsing-Hua University, Hsinchu, Taiwan, R.O.C., in 1993, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1997 and 1999, respectively. His research involved poly-SiGe gate for dual-gate CMOS application and other advanced deep-submicron technologies.

He joined Intel Corp., Hillsboro, OR, in 2000, as a Senior Process Engineer, and is currently involved with the development of 0.1-μm CMOS technology and novel process modules.

Jakub Kedzierski recived the B.S. in electrical engineering in 1995 from The Ohio State University. Currently, he is pursuing the Ph.D. degree in semiconductor device design at the University of California, Berkeley.

His research interests include wrap-around gate transistors, electron beam lithography, and ultrathin body devices. He is involved in the 25-nm device project, which aims to extend CMOS scaling down to 20-nm gate-lengths.

Hideki Takeuchi received the B.E. and M.E. degrees from the University of Tokyo, Tokyo, Japan, in 1988 and 1990, respectively.

He joined the ULSI Development Center, Nippon Steel Corporation, Sagamihara, Japan, in 1990, where he was engaged in the development of DRAM processes. From 1997 to 1999, he was a Visiting Industrial Fellow at the University of California, Berkeley (UCB). He is currently a Research Associate at UCB. His current research interest is in gate stack engineering and ultrashallow junction formation.

Kazuya Asano (S'98-M'00) received the B.S. and M.S. degrees in applied physics from the University of Tokyo, Tokyo, Japan, in 1990 and 1992, respectively, and the M.S. degree in electrical engineering from the University of California, Berkeley, in 1999.

In 1992, he joined NKK Corporation, working on photolithography technologies. In 1997, he went to the University of California, Berkeley, to study ultrasmall transistors on the NKK scholarship program. In 1999, he returned to NKK Corporation, where he is now working as a Circuit Designer for VLSI. His present research interest includes network security, data compression, and circuit design for network devices.

Charles Kuo received the B.S. degree in electrical engineering and computer sciences from the University of California, Berkeley (UCB) in 1996. He is currently pursuing the Ph.D. degree at UCB, with an interest in the characterization and reliability of sub-100 nm MOSFETs and novel semiconductor memory technologies.

He has been with Intel and Altera in the areas of ESD reliability and PLDs, respectively.

Erik Anderson, photograph and biography not available at the time of publication.

Tsu-Jae King, photograph and biography not available at the time of publication.

Jeffrey Bokor (F'00) received the B.S.E.E. degree from the Massachusetts Institute of Technology, Cambridge, in 1975, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1976 and 1980.

From 1980 to 1993, he was with AT&T Bell Laboratories, where he was involved in research on a variety of subjects in optics, microelectronics, and semiconductor physics. He was appointed Professor of electrical engineering and computer science at the University of California, Berkeley, in 1993. His current research activities include extreme ultraviolet projection lithography, nanoelectronics, and ultrafast phenomena in electronic materials.

Prof. Bokor is a Fellow of the American Physical Society and the Optical Society of America.

Chenming Hu (F'90) received the B.S. degree from Taiwan University, Taipei, Taiwan, R.O.C., and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley.

He is TSMC Distinguished Professor of Microelectronics and Professor of electrical engineering and computer sciences at the University of California, Berkeley. His research areas include microelectronic devices, thin dielectrics, nonvolatile memories, and device modeling. He leads the development of the MOSFET model BSIM that has been chosen as the first international standard for IC simulation by Electronics Industry Alliance. He leads the Berkeley team that set the transistor gate-length record with a 18-nm double-gate transistor in 1999. He has authored or co-authored five books and over 600 papers.

He is a member of the National Academy of Engineering, a Fellow of the Institute of Physics, and a life honorary professor of the Chinese Academy of Science. He received the 1997 IEEE Jack A. Morton Award for Solid State Electronics for his contributions to the physics and modeling of MOSFET reliability. In 1997, he received the UC Berkeley Distinguished Teaching Award, and from 1997 to 2000, he held Chancellor's Professor Chair. In 1998, he received the Monie A. Ferst Award of Sogma Xi for encouragement of research through eduation. In 1999, he received W.Y. Pan Foundation Award for Distingushed Research in Electronics and Information Technology.