

A Unity Gain Fully-Differential 10bit and 40MSps Sample-And-Hold Amplifier in 0.18 μ m CMOS

Sanaz Haddadian, and Rahele Hedayati

Abstract—A 10bit, 40 MSps, sample and hold, implemented in 0.18- μ m CMOS technology with 3.3V supply, is presented for application in the front-end stage of an analog-to-digital converter. Topology selection, biasing, compensation and common mode feedback are discussed. Cascode technique has been used to increase the dc gain. The proposed opamp provides 149MHz unity-gain bandwidth (ω_u), 80 degree phase margin and a differential peak to peak output swing more than 2.5v. The circuit has 55db Total Harmonic Distortion (THD), using the improved fully differential two stage operational amplifier of 91.7dB gain. The power dissipation of the designed sample and hold is 4.7mw. The designed system demonstrates relatively suitable response in different process, temperature and supply corners (PVT corners).

Keywords—Analog Integrated Circuit Design, Sample & Hold Amplifier and CMOS Technology.

I. INTRODUCTION

AN important analog building block, especially in data converter systems, is the sample-and-hold circuit.

The Sample and Hold circuit is a main part of most discrete-time systems such as ADCs. In many cases, use of an S&H (at the front of the data converter) can greatly minimize errors due to slightly different delay times in the internal operation of the converter. At first it is necessary to mention some factors which affect the performance of the SHA circuit.

1. Sampling pedestal (hold step): this error occurs when the circuit switches from sampling mode to the holding mode. It is important to know that this error must be independent from input signal. This error may cause nonlinear distortion.

2. The speed at which a sample and hold can track an input signal in sample mode. This parameter is limited by the slew rate and the -3db bandwidth in both small signals and large signals. It is necessary to maximize SR and ω_{3db} for high speed performance.

3. Aperture jitter (aperture uncertainty): this error is the result of effective sampling time changing from one sampling instance to the next and becomes more pronounced for high

speed signals. Specifically, when high speed signals are being sampled, the input signal changes rapidly, resulting in small amounts of aperture uncertainty causing the held voltage to be significantly different from the ideal held voltage[2].

There are also other factors such as dynamic range, linearity, gain, noise, and offset error. There have been different structures for sample and hold circuits. Some examples of these circuits are shown in Fig. 1 (a),(b),(c). In Fig. 1(a) which is titled Flip Around SHA, the input independent nature of the charge injected by the reset switch allows complete cancellation by differential operation. The FA is also a low power structure. But the operation of the circuit depends on the input and output common mode voltage. Specially, in low voltage operations it causes perceptible variations for input voltage.

Illustrated in Fig. 1(a) such an approach employs a differential opamp along with two sampling capacitors so that the charge injected by S_2 appears as a common-mode disturbance at nodes X and Y. In reality, S_2 exhibits a finite charge injection mismatch, an issue resolved by adding another switch, S_{eq} , that turns off slightly after S_2 (and before S_1), thereby equalizing the charge at nodes X and Y [3].

Fig. 1(b) shows another sample and hold circuit used in the paper. In the first phase, ch_1 and ch_2 charged up to $V_{in}-V_{cm}$ and in the second phase $(V_{in}-V_{cm}) + V_{cm}$ appear on output capacitors. Three different phases can be used in order to reduce the charge injection effects.

Another kind of sample and hold is the Charge Redistribution SHA that its operation does not change with the input common-mode voltage (Fig. 1(c)).

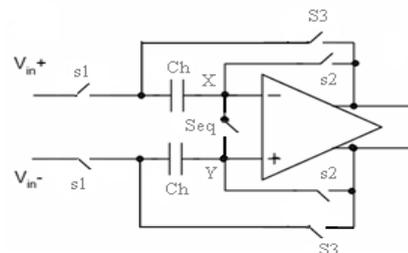


Fig. 1 (a) Circuit of Flip around SHA [3]

S. Haddadian is with Electrical Engineering Department, Sadjad Institute of Higher Education, Mashhad, Iran (phone: +98-915-5077423; e-mail: s.haddadian@ieec.org).

R. Hedayati is with Electrical Engineering Department, Sadjad Institute of Higher Education, Mashhad, Iran (e-mail: rahele.hedayati@yahoo.com).

III. DESIGN PROCEDURE AND CALCULATIONS

For designing a 10bit resolution sample & Hold, total settling error (including both gain and bandwidth errors) of the system would be less than 2^{-11} . The error is obtained from equation (1):

$$e_{tot} = \frac{1}{A\beta} + e^{-\frac{t_s}{\tau}} \tag{1}$$

Where A and β are the open loop gain and the feedback gain respectively, t_s and τ are defined using the following equations:

$$\tau = \frac{1}{\beta \cdot \omega_u}, \quad t_s = \frac{T_{Sample}}{2} \tag{2}$$

These errors are the result of the limited gain and bandwidth which cause limited speed of opamp to settle on its final value. Assuming that both errors have equal portion in the total error of the system, the error due to each factor would be less than 2^{-12} .

To obtain enough gain and bandwidth in the simulations, A and ω_u are assumed more than 80db and 150MHz in the design procedure. For two stage fully differential opamps, unity-gain frequency can be achieved from equation (3). Compensation capacitors are assumed to be in order of 1pf.

$$\omega_u = \frac{g_m}{C_c} \tag{3}$$

Slew Rate is another parameter of the opamp that introduced with equation (4):

$$SR = \frac{dV_o}{\Delta t} = \frac{I_{tail}}{C_c} \tag{4}$$

So I_{tail} would be around 620 μ A.

In SHA circuits, since the output of the opamp changes from V_{CM0} (output common-mode voltage) to V_{dd} or 0 in different phases, dV_o would be $2V_{p-p}$ fully differential output swing or swing/2:

$$V_{effn} = \sqrt{\frac{2I_i}{\mu_n C_{ox} \left(\frac{W}{L}\right)_{in}}} \tag{5}$$

The current of the second stage can be calculated using equation (6):

$$I_{2p} = I_{tail} + I_{2n} + C_l \frac{dv_o}{dt} \tag{6}$$

Considering equation (6) and with the assumption of $\mu_n C_{ox} = 3\mu_p C_{ox} = 270 \frac{\mu A}{V^2}$, V_{effn} & V_{effp} and also the determined currents, the aspect ratios of the transistors will be calculated (it should be mentioned that $V_{effn} \leq V_{effp}$ because of the same current and different mobility).

In calculating the aspect ratios of the transistors the required output swing should be considered. Furthermore, the effective voltages should be considered in amount that variations in different PVT corners wouldn't cause the transistors to enter in linear or cutoff regions. The Nmos and Pmos threshold voltages vary in different corners. Thus the following ranges should be considered.

TABLE I
THRESHOLD VOLTAGE

Voltages/Corners	TT	SS	FF
V_{thn} (v)	0.8	0.9	0.7
V_{thp} (v)	0.7	0.8	0.6

Table II and III exhibit the results of the calculation for the aspect ratios in the first and second stages, respectively.

TABLE II
ASPECT RATIO OF FIRST STAGE

Cascode Transistors	W(μ m)	L(μ m)	V_{dsat} (v)	V_{th} (v)
M_{tail}	10	0.35	0.3065	0.7924
$M_{1,2}$	25	0.35	0.1748	0.7918
$M_{3,4}$	5	0.35	0.3030	0.7913
$M_{5,6}$	8	0.35	-0.6517	-0.6672
$M_{7,8}$	13	0.35	-0.5099	-0.6725

TABLE III
ASPECT RATIO OF SECOND STAGE

Common Source	W(μ m)	L(μ m)	V_{dsat} (v)	V_{th} (v)
$M_{9,11}(m=3)$	96.1	1.5	-0.4662	-0.7075
$M_{10,12}(m=2)$	18.99	1.5	0.5983	0.7819
$M13(R_c)$	1.92	0.35	0.5337	0.7947
$M14(R_c)$	1.92	0.35	0.5337	0.7947

A. Designing Common Mode Feedback

In single ended amplifiers, the feedback circuit set both the common-mode and the differential mode; but since the general feedback circuit just set the differential mode, the fully differential amplifiers require a common mode feedback circuit to set the output common mode. Generally, the differential-mode feedback has not sufficient gain for holding the CM. Even in some cases -such as the two stages fully differential opamps- the negative feedback plays the role of the positive feedback for common mode.

There are key architectures for CMFB circuits such as *Continuous time* approach and *Switched Cap*. The former approach is the limiting factor on maximizing the swing of signals, and the CMFB loop must be stable. The latter approach is useful for the switched capacitor circuits that require high speed for settling output.

In this paper a switched capacitor (C_s) common mode feedback (CMFB) circuit used for each stage that holds the output common-mode on 1.5v. As shown in Fig. 3, C_c generates the average of the output voltages, which is used to create control voltages for the opamp current source. The DC voltage across C_c is determined by C_s which switches between bias voltages and being in parallel with C_c . It acts like a simple switched-cap low pass filter having a DC input signal. The

CMFB circuits with switched cap create large swing signal.

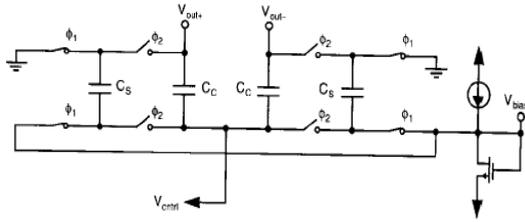


Fig. 3 Switched Cap. CMFB [2]

Table IV shows the aspect ratio and capacitance of the common mode feedback circuits in the paper.

TABLE IV
ASPECT RATIO AND CAPACITANCE OF CMFB

SCCMFB,2	W(μm)/C(PF)	L (μm)
M _{s1,5}	5	0.35
M _{s2,6}	5	0.35
M _{s3,7}	15	0.35
M _{s4,8}	5	0.35
C _{s1,2}	5.3	-----
C _{b1,2}	0.64	-----
M _{s11,55}	2	0.35
M _{s22,66}	2	0.35
M _{s33,77}	2	0.35
M _{s44,88}	2	0.35
C _{s11,22}	0.2	-----
C _{b11,22}	2	-----

Fig. 4(a) illustrates Nmos switch which is selected for the circuit and Fig. 4(b) shows the output common mode voltage.

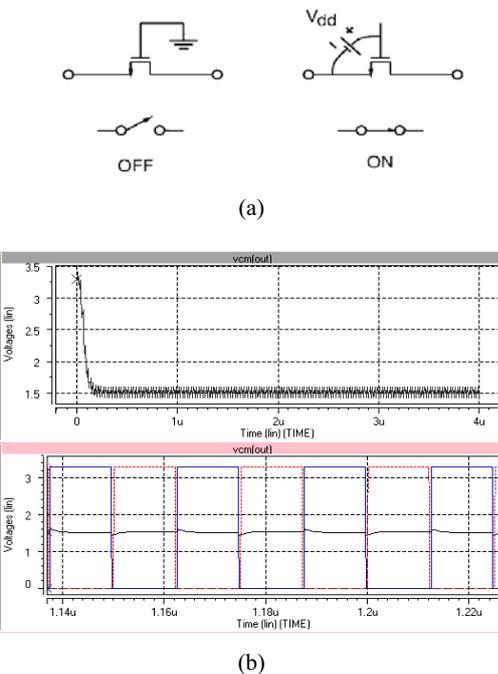


Fig. 4(a) on & off states of a MOS Switch [4]
(b) Output Common Mode (simple and zoomed views)

B. Opamp Compensation

This part discusses how to compensate an opamp to ensure that the closed loop configuration is not only stable but also has good settling characteristics.

Optimum compensation of opamps is typically considered to be one of the most difficult parts of the opamp design procedure. As mentioned in part II, miller compensation has been used in this opamp. The capacitor C_c realizes what is commonly called dominate-pole compensation. It controls dominate first pole, ω_{p1} , and thereby the frequency ω_u . Since:

$$\omega_u = A_0 \omega_{p1} \quad (7)$$

Transistors M_{13} and M_{14} has $V_{ds}=0$, since no DC bias current follow through it, and therefore, $M_{13,14}$ are used in the triode region. Thus, these transistors operate as resistor, R_c , of value given by:

$$R_c = r_{ds13} = \frac{1}{\mu_n c_{ox} \left(\frac{W}{L}\right)_{13} V_{eff13}} \quad (8)$$

This transistor is included in order to realize a left-half-plane zero at frequencies around or slightly above ω_t . Without M_{13} , the circuit will have a right-half-plane zero which makes compensation much more difficult [2].

In this circuit the ω_z is calculated considering equation (9):

$$\omega_z = \frac{-1}{C_c \left(\frac{1}{g_{m9}} - R_c \right)} \quad (9)$$

In order to reduce the effect of the zero frequency, one could take $R_c = \frac{1}{g_{m9}}$ to eliminate the right-half-plane zero.

The second possibility is to choose R_c even larger yet to move the now left-half-plane zero to a frequency slightly greater than the unity-gain frequency that would result if the lead resistor were not present_ say, 20 percent larger [2]. For this case, one should satisfy the following equation:

$$\omega_z = 1.2\omega_t \Rightarrow R_c \cong \frac{1}{1.2g_{m1}} \quad (10)$$

C. Biasing

Fig. 5 shows the bias circuit used in this paper which has been designed based on the required voltages.

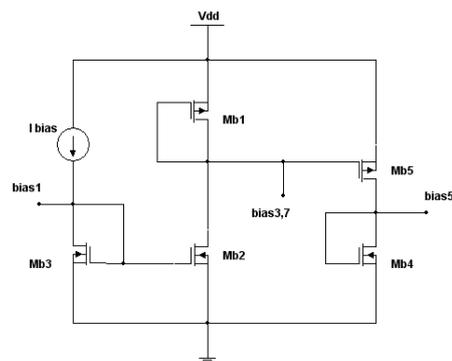


Fig. 5 The bias circuit

D. Simulation Results

The performance of the opamp is analyzed using Hspice.2006.03. Fig. 6 shows the frequency response of the opamp. As it can be seen, in TT process corner with nominal temperature, the opamp has 91.7 dB gain, with 149MHz unity-gain frequency. In order to check the output voltage swing, one approach is to add differentially the amount of the output swing divided by the gain to the input common mode range, so the gain shouldn't vary so much. The simulation results showed 2.6v fully differential output swing for the output voltage.

To make sure that the settling behavior of the opamp satisfies the requirement of the opamp, a pulse voltage of 1v is applied to the feedback system of the sample and hold which will be explained later. The results of simulation are shown in Fig. 6. The output reaches the input pulse after about 10ns which is in good agreement with the required aspect (<10ns).

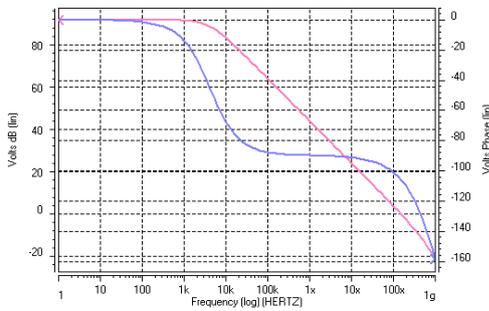


Fig. 6 Frequency Response of Opamp with CMFB

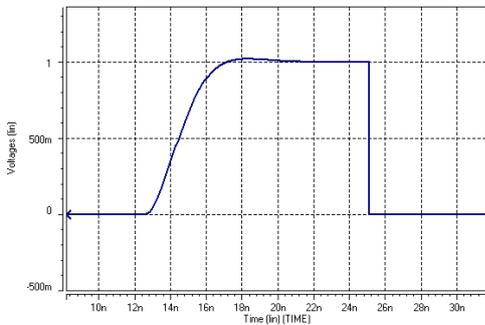


Fig. 7 Settling Behavior of the Opamp

E. PVT Corners Simulation Results

The designed opamp behavior in different process and temperature corners has been mentioned in Table V.

TABLE V
PVT CORNERS

PVT Corners	Gain(dB)	F _u (MHz)	PHM
TT/30°	91.7	149	75
TT/ 0°	99.4	134	56°
SS/ 30°	72	152	+
SS/ 85°	83	122	+
FS/ 30°	65.5	43.3	60
FS/ 0°	88.75	125	+
SF/ 30°	90.2	80	+
SF/ 0°	88.67	114	85
FF/ 30°	93.46	104	42
FF/ 0°	57.97	124	53
V _{dd} =3 v	86	24	+
V _{dd} =3.6 v	93.46	53.7	+

F. Sample & Hold Simulation Results

In this part, the simulation results of the total circuit will be analyzed. Fig. 8 illustrates the waveform of the output of sample and hold while the input frequency is 31/64 of sampling frequency; so the sampling rate will be the Nyquist rate (19.35MHz).

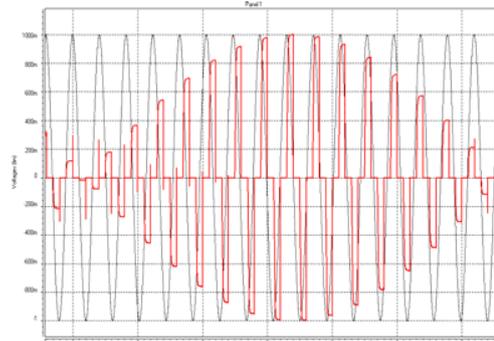
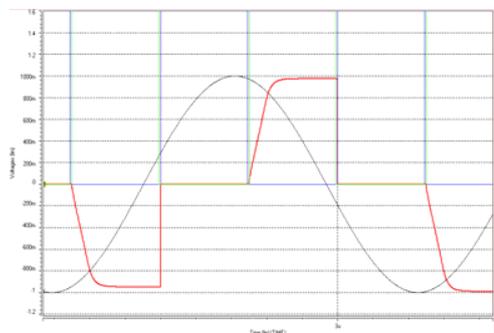


Fig. 8 Waveforms of the input signal and the output of SHA

In order to analyze the error of sampling, Fig. 9 shows the closed view of one sample in the Nyquist rate. The measurements show that there is about 0.5m error which would be attributed to the gain or bandwidth.



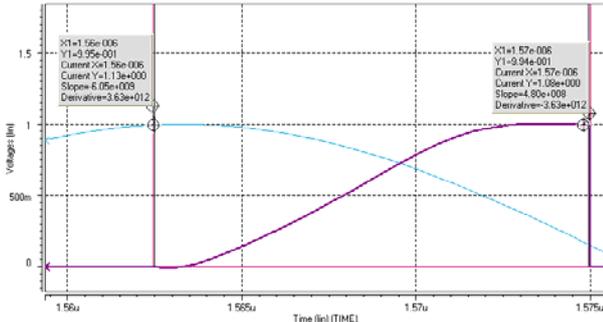


Fig. 9 Zoomed View of the Waveforms

G. The Monte-Carlo and THD Simulations

Fig. 10 shows the frequency response of opamp with Monte-Carlo simulation.

The Equations below have been used for this reason.

$$\sigma = \frac{0.02e - 6}{\sqrt{WL}} \tag{11}$$

This simulation has been applied to 100 points for input transistors. As shown in Fig. 10, for about 30% of the points gain is less than 70db.

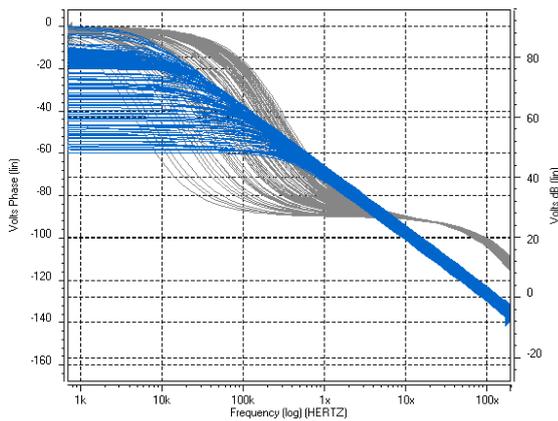


Fig. 10 Monte-Carlo

The Total Harmonic Distortion (THD) of the designed circuit has been estimated. This job has been done through Matlab, with transient step of 0.1n.

$$THD = \frac{\sqrt{V_f^2 + V_{n2}^2 + V_{n3}^2 + \dots}}{V_f} \tag{12}$$

Total Harmonic Distortion has been calculated according to equation 14 with two approaches.

THD1 = 0.95547163395720

THD2 = 0.95594409374826

With this definition, THD must be around 1 (or %100.)

IV. CONCLUSION

Due to the importance of sample and hold amplifiers in discrete-time systems, in this paper, a 10bit 40Msps sample and Hold circuit was designed and simulated to achieve specific aspects. Simulation results illustrate the total system

performance and accuracy. The challenges of design of the operational amplifier and the CMFB have been discussed in detail.

REFERENCES

- [1] P.R. Gray, J. Hursr, S.H Lewis, R.G Meyer, "Analysis and design of analog integrated circuit", John Wiley & sons, 2001.
- [2] d. Johns, K. Martin, "Analog integrated circuit design", 1997.
- [3] B. Razavi, "Design of Analog CMOS Integrated Circuits", MacGrewHil, 2001.
- [4] A. Loloee, A. Zanchi, H. Jin, S. Shehata, E. Bartolome, "A 12b 80Msps Pipelined ADC Core with 190mV Consumption from 3 V in 0.18um Digital CMOS", *ESSCIRC*, 2002.
- [5] O. Choksi, L.Richard Carley, "Analysis of Switched-capacitor Common-Mode Feedback Circuit" *IEEE*, 2003.
- [6] M. Dessouky, M. Louerat, A. Kaiser "Switch Sizing for Very Low-Voltage Switched Capacitor Circuits", *IEEE*, 2001.
- [7] Dessouky, Kaiser " Input Switch Configuration Suitable for rail to rail operation of switched opamp circuits" *IEEE, Electronics letter*, 1999.
- [8] R. Lotfi, "Design of High speed, High resolution and low power Analog-to-Digital Converters" PhD dissertation, 2005.
- [9] R.Van de Plassche, "CMOS Integrated Analog-to-Digital and Digital to Analog Converters, 2nd Edition, 2003.
- [10] Abo, Gray "A 1.5V, 10b 14.3MSpsCMOS Pipeline Analog-to-Digital Converter", *IEEE, Solid State circuits*, 1999.
- [11] P.E Allen, D.R Holberg, "CMOS Analog Circuit Design", OXFORD University Press, 2002.