

# Dual Voltage Design for Minimum Energy Using Gate Slack

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**Abstract**—This paper presents a new slack-time based algorithm for dual  $V_{dd}$  design to achieve maximum energy saving. Although a global optimum is sought computation time is kept low. The slack of a gate is defined as the difference between the critical path delay for the circuit and the delay of the longest path through that gate. A linear-time algorithm is used for computing slacks for all gates of the circuit. Positive non-zero slack gates are classified into two groups, one in which all gates can be unconditionally assigned low voltage and the other where only a selected subset can be assigned low voltage without violating the positive non-zero slack requirement. Multiple voltage boundaries are given special consideration. The overall complexity of this power optimization algorithm is linear in number of gates as compared to a previously published exponential-time exact algorithm using mixed integer linear program (MILP). We apply the new algorithm to optimize ISCAS’85 benchmark circuits and compare the results with those from MILP. We avoid the use of level converters at multiple voltage boundaries. Energy savings from the new slack-time based algorithm is very closed to those from MILP. For c880, the energy saving is 22% for subthreshold voltage operation and 50% for nominal operation in PTM CMOS 90nm. For c2670 nominal voltage design, time of dual voltage optimization is reduced 44X compared to the MILP method. This new algorithm is beneficial for a large circuits with many large positive slack paths that would require enormous time for optimization by the MILP approach.

## I. INTRODUCTION

Scaling power supply voltage ( $V_{dd}$ ) is widely used as a technique for reducing both dynamic power and static leakage power. This degrades the performance. To scale the power supply voltage of a circuit without degrading the performance, a dual  $V_{dd}$  technique exploits time slacks in the circuit by assigning a lower supply voltage ( $V_{DDL}$ ) to gates on non-critical paths and a higher supply voltage ( $V_{DDH}=V_{dd}$ ) to gates on critical paths [2], [10], [13], [14]. For maximizing power saving, an optimal lower supply voltage is determined such that it can be assigned to as many positive slack gates as possible without exceeding the critical path delay. However, signal levels at multiple voltage boundaries require special attention.

The literature gives two main algorithms for dual  $V_{dd}$  design, namely, *clustered voltage scaling* (CVS) [13] and *extended clustered voltage scaling* (ECVS) [14]. To insure correct logic function of gates across multiple voltage bound-

aries without a level converter (LC), the CVS algorithm does not allow the  $V_{DDL}$  cells to feed directly into  $V_{DDH}$  cells and level converting is only implemented within special level conversion flip-flops (LCFF). This topological constraint limits the use of the full slack available to reduce power consumption. The ECVS algorithm eliminates this constraint using a level converter that is inserted when a  $V_{DDL}$  cell drives a  $V_{DDH}$  cell. More power saving is achievable than CVS algorithm. Both algorithms use the backward traversal heuristic traversing the circuit from primary outputs in level order.

Most researches have focused on improving power saving implementing their own greedy algorithms [2], [3], [10]. These are still heuristic approaches and provide a suboptimal solution for dual  $V_{dd}$  assignment. Mixed integer linear programs (MILP) [5] are widely used to optimize a circuit for minimizing power or energy consumption using sizing, multiple  $V_{dd}$ , multiple threshold voltage ( $V_{th}$ ) and combinations of those [4], [9], [12]. MILP searches global optimal solution for an objective function, minimize power, considering the entire design space. Thus, it may take huge time to optimize large circuits used in modern VLSI systems. Time complexity of MILP optimization may not be acceptable in practice.

For dual  $V_{dd}$  design, we need to find the optimal  $V_{DDL}$  and its assignments to positive slack gates in a circuit for minimum power. If we can quickly find all positive slack gates that can be assigned to  $V_{DDL}$ , it reduces much optimization work of dual  $V_{dd}$  design and saves computation time. We propose a new slack-time based algorithm to save computation time and obtain a nearly global solution similar to that obtained by an MILP. The new technique is highly efficient and gives a quality of solution very close to the MILP.

The paper is organized as follows. Section II gives recent background on MILP models [9] for comparison purpose with a proposed algorithm. In Section III, we propose the new slack-time based algorithm for dual  $V_{dd}$  design. Section IV reports SPICE simulation results of our algorithm and MILP to validate results. Finally, a conclusion of this work is given in Section V.

## II. MILP FOR OPTIMAL $V_{DDL}$ AND ASSIGNMENTS OF DUAL $V_{dd}$

There are two ways to find the optimal lower supply voltage  $V_{DDL}$  and its assignments for dual voltage design in the literature. First, the optimal  $V_{DDL}$  is simultaneously searched by applying  $V_{DDL}$  assignment algorithm to a circuit with different  $V_{DDL}$  values, then it selects a pair of the optimal  $V_{DDL}$  and its assignments for minimum power consumption [3], [13], [14]. Otherwise, theoretical path delay model to power supply voltage  $V_{dd}$  is developed to determine the optimal  $V_{DDL}$  for maximum power saving, then  $V_{DDL}$  assignments are executed to achieve lowest power consumption considering multiple voltage boundaries [6], [10]. Most of dual  $V_{dd}$  techniques are based on heuristic greedy algorithms and applied to nominal operating circuits for lowering power consumption.

For energy constrained applications, dual  $V_{dd}$  technique is applied to a subthreshold logic circuit for further reducing minimum energy operating point [9]. In this paper, MILP models similar to CVS are formulated to find the best optimal  $V_{DDL}$  and its assignments for dual  $V_{dd}$  design. This global optimum algorithm is applicable to a circuit operating in both subthreshold and nominal supply voltage, but is needed to multiple runs considering all available  $V_{DDL}$  to given  $V_{DDH}$ . Now, we extend this MILP models to select automatically the optimal  $V_{DDL}$  and its assignments by introducing new variables for one-time run. We briefly explain new variables and parameters here before presenting MILP models.

- $X_{i,v}$ : supply voltage assignment integer variable that is 1 for a gate  $i$  with power supply voltage  $v$ .
- $V_v$ : supply voltage integer variable that is 1 for two selected  $V_{DDH}$  and  $V_{DDL}$  in available power supply voltage  $v$ .
- $td_{i,v}$ : gate delay for a gate  $i$  with supply voltage  $v$ .
- $V_{dd,v}$ : power supply voltage value for  $v$ .
- $G_{tot}$ : total number of gates in a circuit.

MILP models are reformulated from [9]:

$$\text{Minimize } \sum_i \sum_v E_{tot,i,v} \cdot X_{i,v}$$

$$\forall i \in \text{all gates and } \forall v \in \text{power supply voltage domain } V \quad (1)$$

$$E_{tot,i,v} = \alpha_i \cdot C_{L,i,v} \cdot V_{dd,v}^2 + P_{leak,i,v} \cdot T_c \quad (2)$$

Subject to timing constraints:

$$T_i \geq T_j + td_{i,v} \cdot X_{i,v} \quad \forall j \in \text{all fanin gates of gate } i \quad (3)$$

$$T_i \leq T_c \quad \forall i \in \text{all primary output gates} \quad (4)$$

Subject to topological constraints:

$$\sum_{v \in V} V_{dd,v} \cdot X_{i,v} \leq \sum_{v \in V} V_{dd,v} \cdot X_{j,v} \quad (5)$$

$$\forall j \in \text{all fanin gates of gate } i$$

Subject to dual supply voltages selection:

$$\sum_{v \in V} V_v = 2 \quad (6)$$

$$V_{V_{DDH}} = 1 \quad (7)$$

$$\sum_{v \in V} X_{i,v} = 1 \quad \forall i \in \text{all gates} \quad (8)$$

$$\sum_i X_{i,v} \leq G_{tot} \cdot V_v \quad \forall i \in \text{all gates}, \forall v \in V \quad (9)$$

Main difference of MILP models from [9] is dual  $V_{dd}$  selection conditions.  $T_c$  is critical path delay and given by the performance requirement, thus  $V_{DDH}$  is selected from (7) in power supply domain  $V$ . Using a bin-packing technique [1] all gates must be assigned to one of power supply voltage in  $V$  from (8) and (9).

MILP always guarantees that a dual  $V_{dd}$  circuit with the optimal  $V_{DDL}$  and its assignments achieve minimum energy consumption at same performance. We use absolute results of MILP as a reference to check accuracy of our slack-time based algorithm that is presented in next section.

## III. NEW SLACK-TIME BASED ALGORITHM FOR DUAL $V_{dd}$ DESIGN

In this section, we propose a new slack-time based algorithm that finds the optimal  $V_{DDL}$  and its assignments for dual  $V_{dd}$  design as much close as global optimization from MILP solution for minimum energy consumption.

First, Our algorithm generates slack time distribution of a given circuit. We have developed an expanded version of static timing analysis (STA) [7]. For the output of gate  $i$ , let  $T_{PI}(i)$  be the longest time for an event to arrive from a PI and  $T_{PO}(i)$  be the longest time for an event to reach a PO. The delay of the longest path through gate  $i$  is given by,

$$D_{p,i} = T_{PI}(i) + T_{PO}(i) \quad (10)$$

The critical path delay for the circuit is,

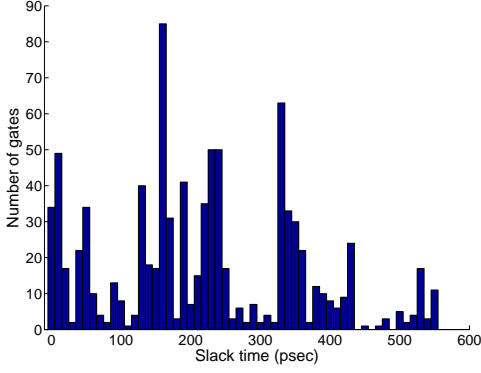
$$T_c = \text{Max}\{D_{p,j}\} \quad \forall \text{ gates } j \quad (11)$$

Slack time for gate  $i$  is found as follows:

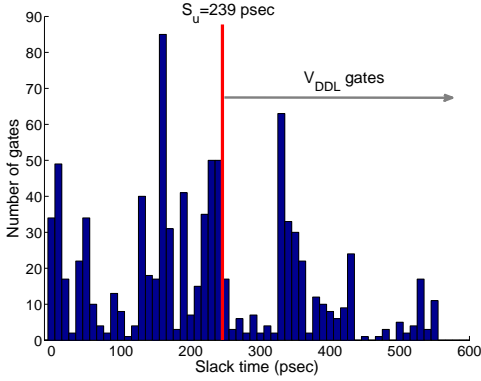
$$S_i = T_c - D_{p,i} \quad (12)$$

The time for calculating slack time for all gates of a circuit is  $O(n)$ , where  $n$  is total number of gates. Figure 1(a) shows the slack time distribution for c2670 ISCAS'85 benchmark circuit in PTM 90nm CMOS technology [16].

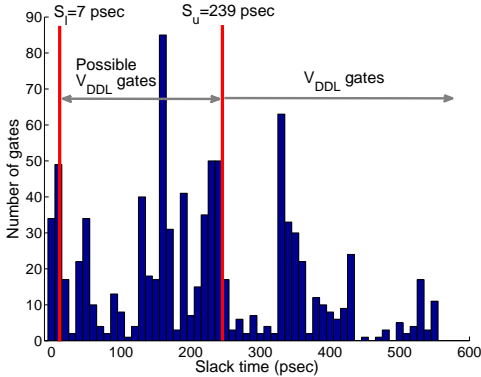
To quickly identify the possible  $V_{DDL}$  gates on non-critical paths, we introduce an upper slack time ( $S_u$ ) that guarantees that any gate with slack time larger than  $S_u$  will be free from timing violation, i.e., *negative slack*, irrespective of the voltage assignment for other gates. The slack time of a  $V_{DDH}$  gate that is equal to  $S_u$  becomes zero after assigning  $V_{DDL}$  to all gates on the longest path through it. We find  $S_u$  using (12).



(a) Slack time distribution for a single nominal  $V_{dd} = 1.2V$ .



(b) Upper slack time  $S_u$  at  $V_{DDH}=1.2V$  and  $V_{DDL} = 0.69V$ .



(c) Lower slack time  $S_l$  at  $V_{DDH} = 1.2V$  and  $V_{DDL} = 0.69V$ .

Fig. 1. Procedure of slack-time based algorithm for c2670 in ISCAS'85 benchmark circuits in PTM 90nm CMOS.

Let  $S'_i$  be the slack time of gate  $i$  after assigning  $V_{DDL}$  to all gates on the longest path through it. Now,  $D'_{p,i}$  is the longest path delay through the gate  $i$ .

$$\begin{aligned}
 S'_i &= T_c - D'_{p,i} \\
 &= T_c - \beta \cdot D_{p,i} \\
 &= T_c - \beta \cdot (T_c - S_i)
 \end{aligned} \tag{13}$$

Where  $\beta$  is the ratio of  $D_{p,i}$  to  $D'_{p,i}$ . It is approximated by

$$\beta = \frac{D'_{p,i}}{D_{p,i}} \approx \frac{T'_c}{T_c} \tag{14}$$

$T'_c$  is the critical path delay when  $V_{DDL}$  is supplied to the entire circuit. It is determined by a modified STA algorithm in the same way as  $T_c$ . By substituting  $S_u$  for  $S_i$  in (13),  $S'_i$  become zero. Thus,  $S_u$  is obtained as:

$$S_u = \frac{\beta - 1}{\beta} \cdot T_c \tag{15}$$

In Figure 1(b), any gate that has a positive slack time larger than  $S_u$ , a right arrow, is safe to be assigned to  $V_{DDL}$  without timing violation.  $S_u$  is used to select the portion of positive slack gates that can be assigned to  $V_{DDL}$ , because it is introduced to differentiate quickly positive slack gates that can be independently assigned to  $V_{DDL}$  without considering others assignments on paths.

The slack time of a gate on critical paths is zero, thus all gates on critical paths have zero slack time. There is no room to assign  $V_{DDL}$  to the gates on it. But, if there is a gate with positive slack time close to zero, it is possible to assign  $V_{DDL}$  to the gate within  $T_c$ . In this case, all gates on paths through it remain with  $V_{DDH}$ , while only the gate is assigned to  $V_{DDL}$ .

Let  $t_d$  be a gate delay in a circuit. After assigning  $V_{DDL}$ ,  $t_d$  is increased by lowering supply voltage. Now, it becomes  $t'_d$ . The amount of  $t'_d - t_d$  is increment of path delay through a gate. Therefore, a gate that has the slack time larger than  $t'_d - t_d$  can be assigned to  $V_{DDL}$ . Let us call this slack time the lower slack time ( $S_l$ ). Because each logic gate has the different value of  $t'_d - t_d$ , we assume the minimum value of  $t'_d - t_d$  is used to define  $S_l$ . It means that any possible  $V_{DDL}$  gates inside a circuit are not missed. Timing violation from this assumption is checked later when  $V_{DDL}$  gates is chosen finally. For simplicity, we assume a path delay is proportion to a gate delay on it.

$$\begin{aligned}
 S_l &= \text{Min} [(t'_d - t_d)_{\text{gates } j}] \\
 &= \text{Min} [(\beta - 1) \cdot t_{d \text{ gates } j}] \quad \forall j \in \text{all gates} \\
 \text{assume } \frac{t'_{d,j}}{t_{d,j}} &\approx \frac{D'_{p,j}}{D_{p,j}} = \beta
 \end{aligned} \tag{16}$$

As shown in Figure 1(c),  $S_l$  can be used to search more possible  $V_{DDL}$  gates between  $S_l$  and  $S_u$ , a double arrow. The gates with positive slack time less than  $S_l$  is always assigned to  $V_{DDH}$  and are located near or on critical paths.

Until now, we demonstrate how to select the gates that can be assigned to  $V_{DDL}$  using simple two slack times,  $S_u$  and  $S_l$ . A gate with slack time larger than  $S_u$  is assigned to  $V_{DDL}$ , while a gate with slack time less than  $S_l$  is assigned to  $V_{DDH}$ . For a gate with slack time between  $S_l$  and  $S_u$ , we need to select carefully its power supply voltage.  $V_{DDL}$  assignment for these gates affects the assignment of other gates on paths to keep any path delays within  $T_c$ . The order of  $V_{DDL}$

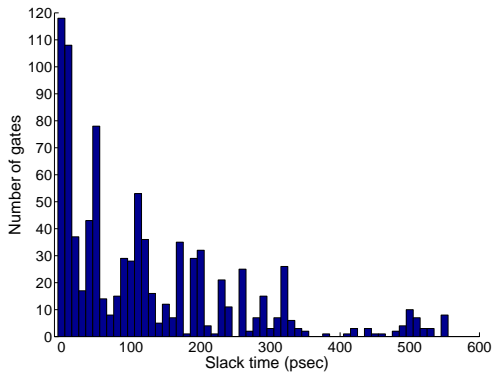


Fig. 2. Slack time distribution of an optimized c2670 with  $V_{DDH} = 1.2V$  and  $V_{DDL} = 0.69V$ .

assignment in these gates affect the energy saving of dual  $V_{dd}$  design, when we consider multiple voltage boundaries. Thus, we need to use greedy approach depending on the type of dual  $V_{dd}$  design. If we allow  $V_{DDL}$  gates to drive  $V_{DDH}$  gates like ECVS, the selection order should consider minimum use of level converters to maximize energy saving. Adversely, CVS does not need level converters, but there exist topological constraints that  $V_{DDL}$  gates can not drive  $V_{DDH}$  gates. Therefore, the selection order is chosen to keep these constraints with as many as  $V_{DDL}$  assignment to gates.

In this paper, we use the slack time distribution to implement dual  $V_{dd}$  algorithm like CVS, then the result of the algorithm is compared to MILP solution in terms of energy saving and run time. To maximize  $V_{DDL}$  assignment in topological constraints, first, higher logic level gates between  $S_l$  and  $S_u$  should be assigned to  $V_{DDL}$ . This priority reflects the fact that  $V_{DDL}$  gates do not feed into  $V_{DDH}$  gates directly. The timing violation should be checked when a gate between  $S_l$  and  $S_u$  is assigned to  $V_{DDL}$ . Now, we finish to find all  $V_{DDL}$  gates, which do not violate the timing constraint by  $T_c$ . After checking topological constraints from these  $V_{DDL}$  gates, all  $V_{DDL}$  gates satisfy the timing and topological constraints according to available  $V_{DDL}$ .

Final stage of the algorithm is searching for the optimal  $V_{DDL}$  value to give maximum energy saving. We already know all  $V_{DDL}$  gates for each available  $V_{DDL}$  value from previous procedures. Thus, we simply calculate the energy saving from  $V_{DDL}$  gates, then select the optimal  $V_{DDL}$  to meet best energy saving. Figure 2 shows that the slack time distribution of an optimized c2670 circuit that has the optimal  $V_{DDL}=0.69V$  from our algorithm. In next section, we shows the results of optimization from slack-time based algorithm for ISCAS'85 benchmark circuits, which operate in either subthreshold or nominal supply voltage.

#### IV. RESULTS

As example circuits, ISCAS'85 benchmark circuits are synthesized with four types of basic standard cells, namely,

INV, NAND2, NAND3, and NOR2. Average activity of a synthesized circuit is found from logic simulation with randomly generated input vectors. We extract gate delay, capacitance and leakage power of basic standard cells in SPICE simulation varying power supply voltage from 0.1V to 1.2V by a 10mV step. All SPICE simulations run at room temperature (300K) using PTM 90nm CMOS, where CMOS device threshold voltages are  $V_{th,pmos} = 0.21V$  and  $V_{th,nmos} = 0.29V$  at nominal  $V_{dd} = 1.2V$ .

For comparing our algorithm in Section III and MILP in Section II, we measure energy consumption of benchmark circuits in SPICE simulation for a single  $V_{dd}$  as a reference. Random input vectors for each circuit in SPICE simulation are same as those in logic simulation to measure the average activity. To find the optimal  $V_{DDL}$  and its assignments for maximum energy saving, MILP algorithm is applied for a synthesized circuit. With MILP solutions, the SPICE netlist of a optimized circuit is generated, where each gate is supplied by its voltage assignment from either given  $V_{DDH}$  or optimal  $V_{DDL}$ . SPICE simulation runs with this nestlist to measure energy consumption of a optimized dual  $V_{dd}$  circuit. Same procedure is done with the results of our slack-time based algorithm.

First, we apply both algorithms for benchmark circuits operating in subthreshold region.  $V_{DDH}$  is given with performance for each benchmark circuit. Table I shows SPICE simulation results from two algorithms. The results of two algorithm exactly match each other, thus we present it once here. Using dual  $V_{dd}$  design, c880 (8-bit ALU) shows 22.2% reduction of its total energy as the best case. In Table II, both algorithm are applied to optimize benchmark circuits operating in nominal supply voltage. We set 1.2V as a nominal power supply voltage for PTM 90nm CMOS by referring to industrial standard 90nm CMOS technologies. The results from both algorithms are not matched for c880 and c6288, but energy savings of two algorithms are very close. From the results, we guarantee our slack-time based algorithm is very close to global optimization results, even it still uses heuristic greedy method to select best  $V_{DDL}$  gates from all  $V_{DDL}$  gates that pass timing constraint for maximum energy saving. For c880, energy savings from MILP and our algorithm are 51.0% and 50.8%, respectively. Compared to the energy savings in the subthreshold region, these energy savings are greater. This is because the supply voltage increases the gate delay exponentially in the subthreshold region, while the gate delay increase for the nominal voltage operation is polynomial following the alpha-power law model [11], [15]. It means that positive slack inside a circuit is reduced quickly by assigning  $V_{DDL}$  in subthreshold region. Thus, we can obtain the optimal  $V_{DDL}$  close to  $V_{DDH}$  and less  $V_{DDL}$  gates from dual  $V_{dd}$  scheme. Figure 3 shows slack time distribution after and before optimization of our algorithm applied to c880 for

TABLE I

ENERGY SAVING AND OPTIMAL  $V_{DDL}$  FROM MILP [9] AND SLACK-TIME BASED ALGORITHM FOR GIVEN  $V_{DDH}$  IN ISCAS'85 BENCHMARK CIRCUITS IN SUBTHRESHOLD REGION IN PTM 90NM CMOS.

Benchmark circuit	Total gates	Activity $\alpha$	$V_{DDH}$ (V)	$V_{DDL}$ (V)	$V_{DDL}$ gates (%)	$E_{single}$ (fJ)	$E_{dual}$ (fJ)	$E_{reduc.}$ (%)	Freq. (MHz)	MILP CPU time(s)*	Slack CPU time(s)*
c432	154	0.19	0.25	0.23	5.2	7.9	7.8	1.1	14.4	0.6	3.0
c499	493	0.21	0.22	0.18	9.7	20.2	19.8	2.0	11.9	0.5	23.2
c880	360	0.18	0.24	0.18	46.4	14.4	11.2	22.2	13.6	8.5	21.2
c1355	469	0.21	0.21	0.18	10.2	19.5	19.0	2.5	9.8	0.3	15.7
c1908	584	0.20	0.24	0.21	24.3	26.5	25.0	5.8	11.8	4.6	57.2
c2670	901	0.16	0.25	0.21	46.4	32.8	28.0	14.8	17.4	51.7	160.3
c3540	1270	0.33	0.23	0.14	7.0	88.0	84.6	3.8	7.2	4.8	306.5
c5315	2077	0.26	0.24	0.19	47.1	116.8	98.0	16.1	9.8	1129.7	801.2
c6288	2407	0.28	0.29	0.18	2.7	165.4	162.0	2.1	9.4	3.7	1531.9
c7552	2823	0.20	0.25	0.21	42.3	131.7	117.1	11.1	13.6	1784.4	1657.8
Average					24.1			8.2			

\*Intel Core 2 Duo 2GHz, 2GB RAM.

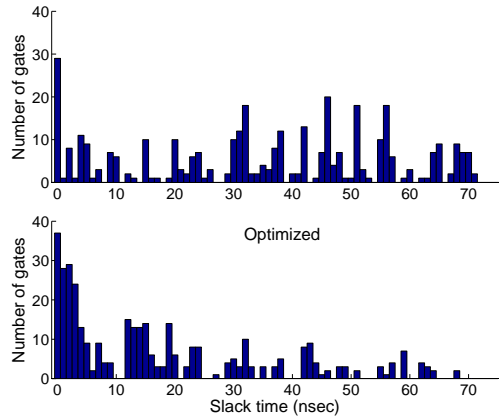
both subthreshold and nominal operation. Before optimization for c880, slack time distribution of two operations are little different. The reason is that the delay of each logic gate has slightly different increment from voltage scaling. It causes little change of slack time distribution inside a circuit.

We measure the run time of two algorithms based on CPU time in second. Our algorithm is written by Perl script language, thus it has inherently slower execution than binary program like C language. The solve time of MILP depends on numbers of integer variables and complexity of inequality equations by linear constraints, and size of optimization space. From Table I, MILP is mostly more fast than our algorithm except for c5315 and c7552. Both circuits has large slack and more optimization space to be searched. Also, available  $V_{DDL}$  as an integer variable in MILP is limited by minimum operating voltage that guarantees correct logic function in lower supply voltage. It is 0.1V from lowest one in power supply domain. This limitation reduces size of optimization space for MILP algorithm to search the optimal  $V_{DDL}$  in subthreshold region.

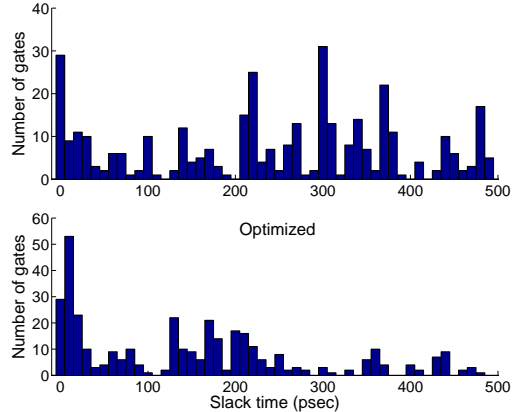
In Table II, the solve time of our algorithm is  $\sim 44X$  faster than MILP for c2670, because more available  $V_{DDL}$  in nominal operation needs to be searched for MILP optimal solutions compared to subthreshold region. For available  $V_{DDL}$  from power supply domain, our algorithm has linear time complexity  $O(n)$  to find best energy saving by reducing time of searching  $V_{DDL}$  gates using  $S_l$  and  $S_u$ , while MILP searches recursively  $V_{DDL}$  gates from all gates inside a circuit to meet best energy saving. From this, MILP shows exponential time complexity for some benchmark circuits. Therefore, we can use our algorithm to optimize large circuits for dual  $V_{dd}$  design within reasonable time instead of MILP.

## V. CONCLUSION

This paper presents a new slack-time based algorithm for dual  $V_{dd}$  design to save computation time and effort for maximizing energy saving to a given circuit. In dual  $V_{dd}$



(a) Subthreshold:  $V_{DDH} = 0.24V$  and  $V_{DDL} = 0.18V$ .



(b) Nominal:  $V_{DDH} = 1.2V$  and  $V_{DDL} = 0.60V$ .

Fig. 3. Slack time distribution before and after optimization of slack-time based algorithm for c880.

design, given performance to a circuit determines higher supply voltage  $V_{DDH}$ . Thus, the selection of lower supply voltage  $V_{DDL}$  and positive slack gates supplied by it is a main problem to optimize a circuit for lowering energy con-

TABLE II  
ENERGY SAVING AND OPTIMAL  $V_{DDL}$  FROM MILP [9] AND SLACK-TIME BASED ALGORITHM FOR ISCAS'85 BENCHMARK CIRCUIT OPERATING IN NOMINAL  $V_{dd}$  IN PTM 90NM CMOS.

Benchmark circuit	Single $V_{dd}$			Dual $V_{dd}$									
	$V_{DDH}$ (V)	$E_{single}$ (fJ)	Freq. (GHz)	MILP					Slack-time based algorithm				
				$V_{DDL}$ (V)	$V_{DDL}$ gate (%)	$E_{dual}$ (fJ)	$E_{reduc.}$ (%)	CPU (s)*	$V_{DDL}$ (V)	$V_{DDL}$ gate(%)	$E_{dual}$ (fJ)	$E_{reduc.}$ (%)	CPU (s)*
c432	1.20	160.1	1.7	0.75	5.2	153.9	3.9	1.0	0.75	5.2	153.9	3.9	18.6
c499	1.20	460.6	2.3	0.79	19.5	433.4	5.9	568.8	0.79	19.5	433.4	5.9	236.3
c880	1.20	277.6	2.0	0.59	56.9	136.1	51.0	583.1	0.60	57.5	136.6	50.8	75.8
c1355	1.20	453.0	2.3	0.69	13.6	433.6	4.3	446.7	0.69	13.6	433.6	4.3	159.9
c1908	1.20	496.5	1.5	0.67	26.9	402.4	19.0	2697.9	0.67	26.9	402.4	19.0	308.2
c2670	1.20	647.6	1.8	0.69	57.9	337.9	47.8	28024.4	0.69	57.9	337.9	47.8	628.3
c3540	1.20	1844.0	1.1	0.70	11.6	1667.0	9.6	770.4	0.70	11.6	1667.0	9.6	1727.9
c6288	1.20	3066.0	0.5	1.18	53.1	2976.0	2.9	15053.8	0.47	2.9	2985.0	2.6	7438.7
Average					30.6		18.0			24.4		18.0	

\*Intel Core 2 Duo 2GHz, 2GB RAM.

sumption. A proposed algorithm is devised to classify simply all positive slack gates to  $V_{DDH}$ , possible  $V_{DDL}$ , and  $V_{DDL}$ , respectively, based on slack time of a gate. After classification, the algorithm only investigates the “possible  $V_{DDL}$  gates” for available  $V_{DDL}$  considering multiple voltage boundaries in energy optimization procedure. This reduces complexity of energy optimization process and the computation time remains tolerable for large size and slack circuits compared to the other available MILP methods. SPICE simulation for ISCAS'85 benchmark circuits shows energy saving up to 22.2% in subthreshold operation and 50.8% in nominal operation, which are the same as were obtained by the higher-complexity MILP method [8], [9]. Computation time is reduced up to 44X compared to MILP. Our proposed algorithm has linear time complexity  $O(n)$  with total  $n$  number of gates of a circuit. A new slack-time based algorithm is useful, when MILP is limited by its exponential time cost for a specific circuit design.

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