

A Design Scheme for Sampling Switch in Active Matrix LCD

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Abstract – In the design of a source driver in an active matrix LCD, of primal importance is the issue of how to restrict the admissible allowance of the RPV (i.e. the ratio of the pixel voltage to the video voltage) of a pixel within a specified narrow range, which determines the transmitted luminance of the pixel. This constraint on the RPV is analyzed in terms of parameters associated with the sampling switch and the sampling pulse, and then by using a minimal number of these parameters a design scheme is described dedicatedly for the sampling switch. Experimental results show that an optimal sampling switch can be attained by the proposed scheme, which gives rise to a source driver with almost 50% less power consumption than the one by manual design.

1 INTRODUCTION

LCDs (Liquid Crystal Displays) have established a firm foothold on the market as flat panel displays, first for calculators, subsequently for personal computers, mobile appliances, digital cameras, etc., and at present with increasing importance for TVs. Thus, development is continuing further on the picture quality as well as the picture function of LCDs, and hence the design automation has to be enhanced more and more for drivers which affect most the performance of LCDs[1].

In the TFT(Thin Film Transistor)-addressed LCD, usually called *active matrix LCD*, as illustrated in Fig.1, the grey shade is controlled individually in each pixel by applying an appropriate pixel voltage. In each column of the matrix, a pair of nMOS and pMOS TFTs connected in parallel operates as a sampling switch which is to sample the video signal and to transmit the signal to the source line. During the period when a row of pixels are activated by the gate line in the row, the video information (i.e. video voltage) corresponding to a desired gray shade is fed into each pixel in the row, from column to column, whereas all pixels in other rows are blocked by grounding their gate lines.

Thus, during this period the source drivers have to activate all pixels in the row, and hence the operation

speed of the source driver in each column, henceforth designated as *column driver*, is far greater than that of the gate driver in each row, henceforth referred to as *row driver*. This implies that the column driver acts a principal role to determine the RPV (Ratio of Pixel voltage to Video voltage) of each pixel.

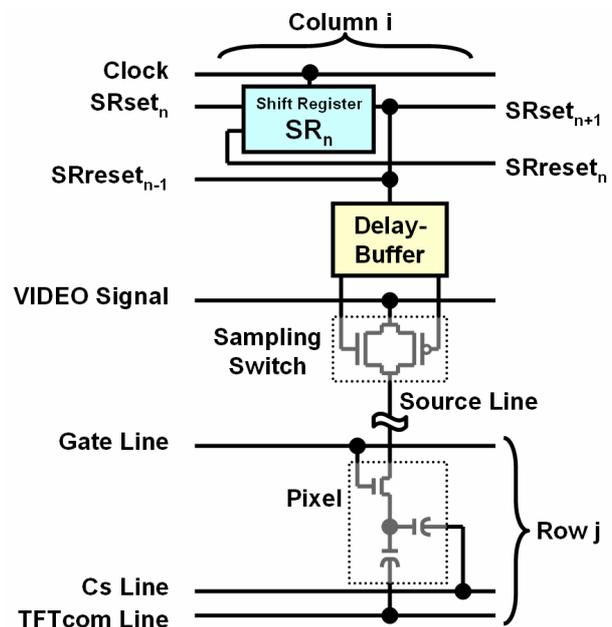


Fig. 1: Column driver in active matrix LCD.

Given a pixel, let V_{vd} denote the video voltage to be fed into it, and let V_{px} represent the pixel voltage. Then for this pixel we have $RPV = V_{px}/V_{vd}$. Our ideal goal is how to make this RPV approach to 100[%], or in other words, how to make each pixel attain the desired grey shade.

Recently, with the advance of LCD technologies, the column and row drivers have to be implemented more and more finely on the same substrate as the picture plane. However, in such implementation there occur considerable fluctuations in the transistor performance, which make the design of column drivers difficult from the aspect of the functional

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verification as well as the minimization of circuit area and power consumption.

This paper intends to seek a design scheme dedicated for the sampling switch of a column driver, aiming at the following objectives:

- Given a specified value B , restrict the RPV within $100 \pm B$ [%].
- Minimize the power consumption.
- Minimize the delay and its fluctuation of the sampling pulse from the system clock.
- Implement the column driver within a certain width specified for a pixel column.

To achieve these objectives, the most intensive work is on the subject of how to determine the size of each transistor in the column driver. This paper first analyzes how the design parameters of sampling switch and sampling pulse are related to the RPV, and then seeks a minimal number of parameters which contribute most to the behavior of RPV, so as to simplify the circuit simulation. With the use of these parameters a design scheme is described for the sampling switch of the column driver. Experimental results show that an optimal sampling switch can be attained by this scheme, which gives rise to a column driver with almost 50% less power consumption than the one by manual design.

2 PREPARATIONS

First, consider the behavior of a sampling switch composed of a parallel connection of nMOS and pMOS TFTs, as shown in Fig.1. Let W_n be the gate width of an nMOS TFT, and let SMP denote a sampling pulse input to this nMOS TFT, for which the rising time, falling time, and intermediate time between them are denoted by t_r , t_f , and t_w , respectively. Similarly, let W_p be the gate width of a pMOS TFT, and let $SMPB$ designate a pulse input to this pMOS TFT. For simplicity, let both of SMP and $SMPB$ be of the piece-wise linear waveform, reverse to each other. Thus, W_n , W_p , t_r , t_f , and t_w are regarded as the basic design parameters for pulses SMP and $SMPB$.

Although t_r , t_f , and t_w are common to SMP and $SMPB$, RPV changes differently according as the combination of video voltage V_{vd} and common electrode voltage V_{com} differs, as outlined in what follows.

Here, it should be remarked that the common electrode voltage V_{com} alternates a high voltage level $V_{com-high}$ and a low voltage level $V_{com-low}$, frame by frame, that is, if a pixel receives a video signal when V_{com} is at high level $V_{com-high}$, then next time it receives a video signal, V_{com} is at low level $V_{com-low}$. When V_{com} is at low level $V_{com-low}$ (or at high level $V_{com-high}$), let the feeding a video signal to a pixel be designated as the *plus* (or *minus*) feeding.

Now, to cope with the worst-case variation of RPV, consider the case in which it takes the longest time from the instance when SMP has just risen to the peak to the instance when pixel voltage V_{px} approaches enough to video voltage V_{vd} , that is, the case in which the feeding a video voltage into a pixel is most difficult. Thus, in such an ill case, let us impose a constraint that RPV should be over $100 - B$ [%], where it should be noted that in any other case RPV may remain greater than this lower bound. In this way, by repeated application of circuit simulation for typical combinations of video voltage V_{vd} and common electrode voltage V_{com} , all such ill cases are checked so as to make RPV remain within the required range.

However, it should be remarked that there may occur the case that although SMP has risen to the peak to make RPV satisfy the constraint, the drain voltage of the nMOS TFT is changed by the *channel charge injection*, and subsequently RPV breaks out of the required range, while SMP is falling or the sampling switch turns off[2,3,4]. Here, let Δ denote the deviation of RPV, which is dependent on W_n , W_p , and source-gate voltage V_{gs} of TFT. If this V_{gs} is constant, then we can derive a relation $W_p = a \cdot W_n + b$ between W_p and W_n such that the deviation Δ becomes 0. However, a and b are constants dependent on V_{gs} , which is also dependent on video voltage V_{vd} , and hence for any V_{vd} it is impossible to find an explicit relation between W_n and W_p .

Noting the nonlinear relation between RPV and pixel voltage V_{px} , we can see that there exists a pixel voltage V_{px} which makes RPV change most steeply. Now, seek the video voltage V_{vd} which gives rise to this V_{px} , and then by using the source-gate voltage V_{gs} attained by this video voltage V_{vd} , we can find constants a and b which reduce Δ to 0. Thus by using the relation $W_p = a \cdot W_n + b$, the parameters necessary for analyzing the constraint imposed on RPV can be reduced to W_n , t_r , t_f , and t_w .

Here, it should be added that the constants a and b thus obtained can reduce Δ to 0 at a certain video voltage V_{vd} , and hence it may happen that pixel voltage V_{px} can approach very quickly to this V_{vd} , that is, the feeding V_{vd} to a pixel can be very easy. If this is the case, it can be highly possible for RPV to exceed $100 + B$ [%], even if SMP is falling or has fallen to the bottom. Thus, another set of constrains should be investigated in detail for RPV not to exceed $100 + B$ [%] just in the same way as the constrains so far discussed for RPV not to drop from $100 - B$ [%].

3 DESIGN PROCEDURE

Seeing that in the real world of producing active matrix LCDs there exist a large variety of fluctuations in the design parameters, transistor

performances, voltage sources, etc., mainly incurred by the implementation of drivers on the same substrate as the picture plane, of practical importance are technical ideas of how to treat these fluctuations in the process of designing the sampling switch. Motivated by this, our design scheme attempts to adopt these fluctuations in the design process as follows.

Assume that the gate widths W_n and W_p are fluctuated with $W_n \pm \sigma_n$ and $W_p \pm \sigma_p$, respectively, the high and low voltage levels V_{high} and V_{low} of pulse SMP (SMPB) are with $V_{\text{high}} \pm v_{\text{high}}$ and $V_{\text{low}} \pm v_{\text{low}}$, respectively, and their rising time t_r , falling time t_f , and intermediate time t_w are with $t_r(1 \pm \varepsilon_r)$, $t_f(1 \pm \varepsilon_f)$, and $t_w(1 \pm \varepsilon_w)$, respectively, where ε 's are between 0 and 1. Moreover, assume that the time T necessary for activating a video signal in a pixel is distorted within $T(1 \pm \varepsilon_T)$, where ε_T is between 0 and 1.

Since these ε 's are dependent on the performance of the delay-buffer to generate SMP and SMPB, they are unknown in advance, and hence let their estimated values be adopted in the following design.

Now, let us set the pulse width $t_r + t_w + t_f$ of SMP as long as possible, not only because the longer is the opening period of SMP, the shorter we can make widths W_n and W_p , but also because shortening W_n and W_p can contribute to the area and power minimization. Thus in our design scheme the following equations are settled:

<simple sampling>

$$(1 + \varepsilon_r) \cdot t_r + (1 + \varepsilon_w) \cdot t_w + (1 + \varepsilon_f) \cdot t_f = T \cdot (1 - \varepsilon_T) \quad (1)$$

<double sampling>

$$(1 + \varepsilon_r) \cdot t_r + (1 + \varepsilon_w) \cdot t_w + (1 + \varepsilon_f) \cdot t_f = 2T \cdot (1 - \varepsilon_T) \quad (2)$$

Here, simple and double samplings mean the methods to open the sampling switch, whose timing charts are shown in Fig.2.

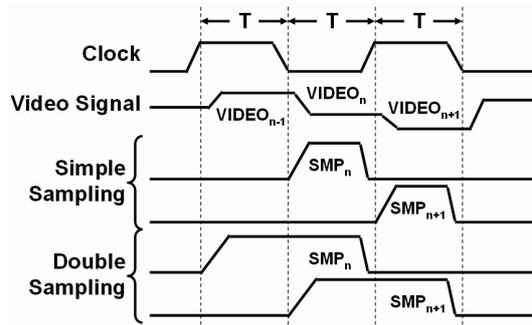


Fig. 2: Timing charts of simple and double samplings.

Considering that the sampling switch is driven by pulses SMP and SMPB generated in the delay-buffer, t_r and t_f are regulated by this buffer. Since t_r and t_f

together with W_n contribute to the constraint on RPV, they can be sought with respect to the constraint, whereas t_w is determined by (1) or (2).

Now, let $t_{r-\text{min}}$ and $t_{f-\text{min}}$ denote the minimum of t_r and t_f , respectively. The values of $t_{r-\text{min}}$ and $t_{f-\text{min}}$ are determined by the pulses generated by TFTs with the maximal values of W_n and W_p , respectively. As for the upper bounds of t_r and t_f , we consider the following two conditions:

- (i) During the time interval t_{ph} from the instance when SMP falls to the bottom to the instance when the video signal begins to show the voltage of the next pixel, SMP must turn off.
- (ii) $t_r + t_f$ should not exceed T , since otherwise SMP can not fully swing.

Thus we have

$$t_{f-\text{min}}/(1 - \varepsilon_f) < t_f < 2 \cdot t_{\text{ph}}/(1 + \varepsilon_f) \quad (3)$$

$$t_{r-\text{min}}/(1 - \varepsilon_r) < t_r < \{T \cdot (1 - \varepsilon_r) - t_f(1 + \varepsilon_f)\}/(1 + \varepsilon_r) \quad (4)$$

On the basis of the above discussion, the constraint imposed on RPV can be sought through the following procedures.

Step1: For the video voltage which makes RPV change most steeply, seek constants a and b of relation $W_p = a \cdot W_n + b$ which reduces Δ due to the charge injection to 0.

Step2: For a number of pairs (t_r, t_f) satisfying (3) and (4), apply the following:

2.1 Given a pair (t_r, t_f) , calculate t_w using (1) or (2).

2.2 For (t_r, t_w, t_f) , seek the condition in which RPV is difficult to grow (see **comment 1** below), and under this condition calculate the minimum value $W_{n-\text{min}}$ of W_n which makes RPV equal to $100 - B[\%]$.

2.3 For (t_r, t_w, t_f) , seek the condition in which RPV is easy to grow (see **comment 2** below), and under this condition calculate the maximum value $W_{n-\text{max}}$ of W_n which makes RPV equal to $100 + B[\%]$.

//**comment 1**// The condition stated in **2.2** indicates the one satisfying

- (i) by the time when SMP falls, the pixel voltage is difficult to reach the video voltage, and
- (ii) the deviation Δ due to the charge injection can not contribute to raising RPV.

//**comment 2**// The condition stated in **2.3** indicates the one satisfying

- (i) by the time SMP falls, the pixel voltage is easy to reach the video voltage, and
- (ii) the deviation Δ due to the charge injection raises RPV.

4 EXPERIMENTAL RESULTS

We have applied the proposed procedure to a sampling switch of the column driver already designed manually. Fig.3 shows the experimental results, where the upper and lower surfaces at the left hand side of the figure indicate (t_r, t_f, W_{n-max}) and (t_r, t_f, W_{n-min}) , respectively, and the space between these two surfaces corresponds to (t_r, t_f, W_n) for which RPV satisfies the constraint. An optimal sampling switch can be attained by selecting (t_r, t_f, W_n) such that

- (i) both of $W_{n-max}-W_n$ and W_n-W_{n-min} exceed the fluctuation σ_n ,
- (ii) W_n can be minimal, and
- (iii) t_r and t_f can be maximal.

With the use of this method, parameters t_r, t_w, t_f, W_n , and W_p are calculated. Then, W_n and W_p have been reduced by 62% and 47%, respectively, and t_r has been increased by 50% in comparison with those obtained by manual design. As a result, the constraints imposed on the sampling pulse generation can be lightened such that the power consumption of a column driver can be reduced by 46% through 54%.

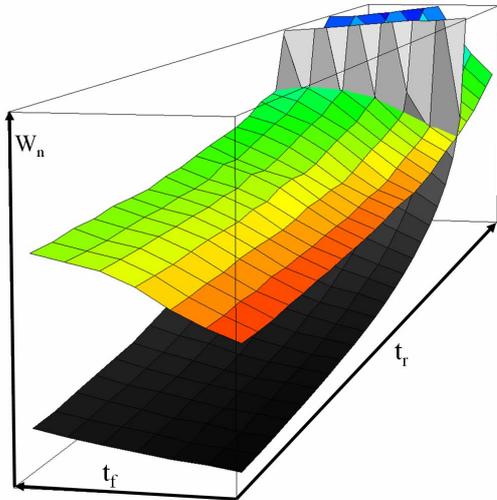


Fig. 3: Surfaces of (t_r, t_f, W_{n-min}) and (t_r, t_f, W_{n-max}) .

Moreover, RPVs have been evaluated for 270 combinations of the feeding of video voltage into pixel and the fluctuation of supply voltages and sampling transistors, where the combinations are selected from 2 feedings (plus and minus), 3 fluctuations (high, typical, and low) of V_{ss}, V_{dd} and system clock voltage, and 5 fluctuations (best, typical, and worst) of SPICE parameters of nMOS and pMOS of the sampling switch. The histograms of RPVs obtained by our design scheme and by manual design are shown in Fig. 4, where it can be seen that most of the objectives set

up for RPVs have been achieved. It should also be pointed out that in manual design there occur the cases in which the constraints for RPV are not satisfied due to the lack in the insufficient treatment of charge injection.

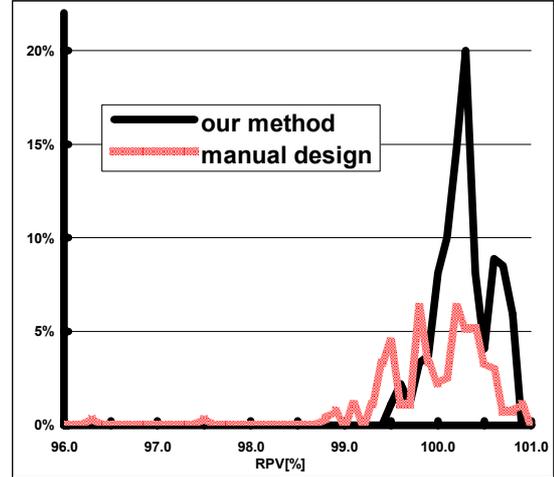


Fig. 4: Histogram of RPVs.

5 CONCLUSIONS

A practical design scheme has been devised dedicatedly for the sampling switch of active matrix LCDs which satisfies the required constraint for RPV. This design scheme provides a very powerful tool which contributes greatly to the design automation of column drivers.

Development is continuing on constructing a full set of design tools for column drivers.

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