Computer Systems Laboratory
Cornell University, Ithaca, NY 14853

Analysis and Synthesis of Static Translinear Circuits

Bradley A. Minch

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Bradley A. Minch

School of Electrical and Computer Engineering
Cornell University
Ithaca, NY 14853-5401

minch@ee.cornell.edu
http://www.ee.cornell.edu/~minch

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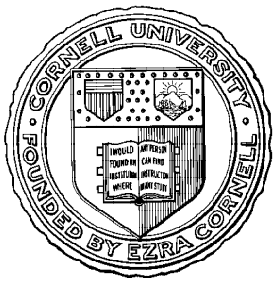

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minch@ee.cornell.edu

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Abstract

This report describes the class of static translinear circuits*, which are capable of accurately implementing a wide range of static nonlinear relationships in the current signal domain, such as products, quotients, fixed power-law relationships, vector magnitude, and rational functions. After a brief historical account of the emergence of the class of translinear circuits, we examine the representation of information in translinear circuits and systems. Then, we describe the translinear principle and its application to the analysis and synthesis of translinear-loop circuits, illustrating the processes with several example circuits. We then describe the operation and implementation of a translinear-circuit primitive called the* multiple-input translinear element *(MITE). From such elements, we build MITE networks, a class of low-voltage translinear circuits that is equivalent to the class of translinear-loop circuits. We describe intuitively the operation of MITE networks. We also describe how to analyze and synthesize such circuits, illustrating these processes with several example circuits.*

1 Translinear Circuits: What's in a Name?

In 1975, Barrie Gilbert coined the word *translinear* to describe a class of circuits whose large-signal behavior hinges on the extraordinarily precise exponential current–voltage characteristic of the bipolar transistor and the intimate thermal contact and close matching of monolithically integrated devices [1]. The functions performed by these fundamentally large-signal circuits—including multiplication [2–7], wideband signal amplification [3,8], and various power-law relationships [9]—were utterly incomprehensible from the customary linear-circuit picture of the bipolar transistor

as a linear current amplifier whose key property is its forward current gain, β. At the same time, Gilbert also succinctly enunciated a general circuit principle, the *translinear principle* (TLP), by which we can analyze the (steady-state) large-signal characteristics of such circuits quickly, usually with only a few lines of algebra, by considering only the currents flowing in the circuits.

The word *translinear* derives from a contraction of one way of stating the exponential current–voltage characteristic of the bipolar transistor that is central to the functioning of these circuits—that is, the bipolar transistor's *trans*conductance is *linear* in its collector current. Gilbert also meant the word to convey the notion of analysis and design techniques (e.g., the translinear principle) that bridge the gap between the well-established domain of linear-circuit design and the largely uncharted domain of nonlinear-circuit design, for which precious little can be said in general [10–12]. As we shall see in Section 4, the translinear principle is essentially a *trans*lation through the exponential current–voltage relationship of a *linear* constraint on the voltages in a circuit (i.e., Kirchhoff's voltage law) into a product-of-power-law constraint on collector currents flowing in the circuit.

Since Gilbert coined the word *translinear*, the translinear principle has been the basis of a plethora of useful nonlinear circuits, including wideband analog multipliers [13–15], translinear current conveyors [16–18], translinear frequency multipliers [19–22], operational current amplifiers [23–26], RMS–DC converters [27–32], and vector-magnitude circuits [28, 33–36]. In the 1980s, Evert Seevinck [37, 38] made significant contributions to the state of the art of translinear-circuit design by developing systematic techniques for the analysis and synthesis of these circuits.

Since the mid-1990s, there has been a growing interest in translinear circuits, primarily because of the development of the class of *dynamic translinear circuits*, which had its origins in 1979 in the work of Robert Adams [39]. Although he does not appear to have made a connection between his own ideas and the growing body of work on translinear circuits, Adams proposed a method of implementing large-signal–linear, continuous-time filters using linear capacitors, constant current sources, and translinear devices, which he called *log-domain filtering*, because all of the filtering occurred on log-compressed voltage state variables using translinear devices. The concept of log-domain filtering remained in obscurity for over a decade, only to be independently rediscovered by Seevinck. In 1990, Seevinck presented a first-order filter, which he dubbed a *companding current-mode integrator* [40]. Unfortunately, it appears that neither Seevinck nor Adams had a clear idea of how to generalize their ideas to implement filters of higher order. In 1993, encouraged by Adams to pursue the idea of log-domain filtering, Doug Frey introduced a general method for synthesizing log-domain filters of arbitrary order using a state-space approach and he presented a highly modular technique for implementing such filters [41].

Jan Mulder *et al.* coined the phrase *dynamic translinear circuits* and have made the clearest connection between translinear circuits and log-domain filters [42–45]. They have extended Seevinck's translinear analysis and synthesis methodology to encompass dynamic constraints based on what they have called the *dynamic translinear principle*, with which we can express capacitive currents embedded within translinear loops directly in terms of products of the currents flowing through translinear devices and their time derivatives. Dynamic translinear circuit techniques have been successfully applied to the structured design of both linear dynamical systems (e.g., log-domain filters [41, 46–53]) and nonlinear dynamical systems (e.g., RMS-DC converters [30–32], oscilla-

tors [54–57], phase detectors [58], and phase-locked loops [59,60]). Although dynamic translinear circuits are beyond the scope of this report, the principles that we shall develop directly extend to and form a foundation for the analysis and synthesis of this emerging class of circuits.

2 The Ideal Translinear Element

Figure 1a shows a circuit symbol for an ideal *translinear element* (TE). This symbol, which has a gate, an emitter, and a collector, is commonly used in power electronics to represent an *insulated-gate bipolar transistor* (IGBT), which is a hybrid bipolar/MOS device that combines the high input impedance of an MOS transistor and the larger current-handling capabilities of a power bipolar transistor. Although it may be possible to build translinear circuits with IGBTs, that possibility is *not* what we are presently considering. Instead, we use the circuit symbol shown in Fig. 1a for two reasons. First, the ideal TE should have the nearly inviolate exponential current–voltage relationship of the bipolar transistor and the infinite input impedance of the MOS transistor; the hybrid symbol of Fig. 1a is highly suggestive of precisely this mixture of bipolar and MOS qualities. Second, even though translinear circuits were originally implemented with bipolar transistors, we can also implement such circuits using subthreshold MOS transistors. By using a symbol for the ideal TE that resembles both types of transistors, we remind ourselves continually of this fact.

We shall assume that the ideal TE produces a collector current, I, that is exponential in its gate-to-emitter voltage, V, and is given by

$$I = \lambda I_{\mathrm{s}} e^{\eta V / U_{\mathrm{T}}}, \tag{1}$$

where I_{s} is a pre-exponential scaling current, λ is a dimensionless constant that scales I_{s} proportionally, η is a dimensionless constant that scales the gate-to-emitter voltage, V, and U_{T} is the thermal voltage, kT/q. To demonstrate that the ideal TE is *translinear* in the first sense of the word that we discussed in Section 1, we can calculate its transconductance by simply differentiating Eq. 1 with respect to V to obtain

$$\begin{aligned} g_m &= \frac{\partial I}{\partial V} \\ &= \lambda I_{\mathrm{s}} e^{\eta V / U_{\mathrm{T}}} \times \frac{\eta}{U_{\mathrm{T}}} \\ &= \frac{\eta I}{U_{\mathrm{T}}}. \end{aligned}$$

Figures 1b through 1e show five practical circuit implementations of the ideal TE. The first of these TEs is the *pn* junction diode, shown in Fig. 1b. Although the forward-biased diode does have an exponential current–voltage characteristic, it is a two-terminal device and does not, strictly speaking, have a transconductance. Moreover, diodes seldom actually appear in translinear circuits; instead, for the sake of device matching, we almost invariably use diode-connected transistors in place of diodes. Nonetheless, for simplicity, many presentations of the translinear principle begin

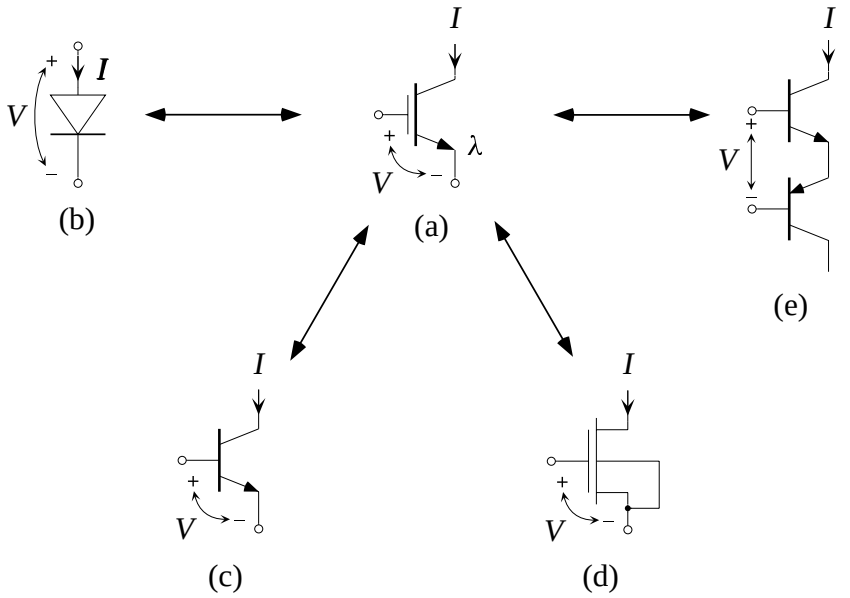


Figure 1: Translinear elements (TEs). (a) Circuit symbol for an ideal TE. Such a device produces a current, I, that is exponential in its controlling voltage, V. Parts b through f show five practical TE implementations comprising (b) a diode, (c) an *npn* bipolar transistor, (d) a subthreshold MOS transistor with its source and bulk connected together, and (e) a compound TE comprising an *npn* and a *pnp* with their emitters connected together. Of course, for the TEs shown in parts c and d, the appropriate complementary transistors are also TEs.

by considering a loop of diodes. For the diode, λ corresponds to the relative area of the *pn* junction and η is typically very nearly unity.

The bipolar transistor, shown in Fig. 1c, biased into its forward–active region is considered by most people to be the quintessential TE. The bipolar transistor commonly exhibits a precise exponential relationship between its collector current and its base-to-emitter voltage over more than eight decades of current. For the bipolar transistor, λ corresponds to the relative area of the emitter–base junction and η is typically close to one. The main limitation of the bipolar transistor as a TE is the existence of a finite base current, which is often what limits the range of usable current levels in bipolar translinear circuits.

The subthreshold MOS transistor with its source and bulk connected together, as shown in Fig. 1d, biased into saturation also has an exponential current–voltage characteristic. In this case, λ corresponds to the W/L ratio of the MOS transistor and η is equal to κ, which is the incremental capacitive-divider ratio between the gate and the channel. The requirement that the source and bulk be shorted together stems from the fact that the gate and source do not have the same effect on the energy barrier (i.e., the source-to-channel potential) that controls the flow of current in the channel. The source potential directly affects this barrier height, whereas the gate couples capacitively into

the channel and only partially determines (i.e., with a weight of κ) the channel potential. The bulk also couples into the channel capacitively and partially determines the channel potential (i.e., with a weight of $1-\kappa$. By connecting the source and bulk together, we can use the bulk in opposition to the source to reduce the source's net effectiveness at controlling the barrier height to match precisely the effectiveness of the gate.

In the majority of bulk CMOS technologies, we fabricate one type of MOS transistor (i.e., either *n*MOS or *p*MOS) in a global substrate that we maintain at a single common potential, while we fabricate the other type inside of isolated local substrates, called *wells* that we may have at different potentials. In such technologies, we can only connect the source and bulk together for the type of transistor that is fabricated inside of the well; for instance, in an *n*-well CMOS technology, the *p*MOS transistors are fabricated in *n*-wells. By fabricating *p*MOS transistors in separate wells, we can connect their sources and bulks together and simultaneously have different TEs operating with different source potentials. In such a technology, we fabricate all of the *n*MOS transistors inside a global *p*-type substrate; hence, if we must short all of the sources and bulks together, we cannot operate different TEs with their sources at different potentials. Fortunately, as we shall see in Section 4, for certain translinear-loop topologies, we do not need to connect together the source and bulk of all of the MOS transistors within the translinear loops.

We can construct a variety of *compound* TEs by combining two or more transistors in various ways. Figure 1e shows one such compound TE, comprising an *npn* transistor and a *pnp* bipolar transistor with their emitters connected together. For this TE, the controlling voltage is the voltage difference between the base of the *npn* and that of the *pnp* and the output current is available at the collector of either transistor. Also, λ corresponds to the geometric mean between the relative emitter area of the *npn* and the relative emitter area of the *pnp* and $\eta = \frac{1}{2}$.

3 Translinear Signal Representations

Translinear circuits are *current-mode* circuits, which means that their input and output signals are represented as currents. More precisely, we represent a dimensionless quantity, z, as the ratio of a *signal current*, I_z, to a *unit current*, I_u. In other words, we define a number, z, by

$$z \equiv \frac{I_z}{I_u}.$$

We call I_u the unit current precisely because it is the current level that represents unity in our number system; that is, $z = 1$ if and only if $I_z = I_u$. The value of the unit current ultimately determines the power dissipation, computational throughput, and the precision of a translinear analog information-processing system. By allowing the unit current level to change over time, we can build computing systems that can adaptively trade computational throughput and precision for power dissipation [61].

The representation of signals by currents in translinear circuits is something like a floating-point number representation in the digital domain. For translinear circuits, current signals span a large

dynamic range (typically several decades), but noise restricts the precision available at any given signal-current level to a certain finite fraction of that current level (i.e., given by the *noise-to-signal ratio* (NSR)). The manner in which the noise current scales with the signal current depends on the type of noise that is predominant in the system [62]. If white noise is predominant, then NSR scales inversely with the square root of the signal current, so we can trade power consumption for precision. On the other hand, if $1/f$ noise dominates the spectrum, then the NSR is roughly independent of the signal-current level, so we cannot obtain additional precision by increasing power consumption. In the digital domain, floating-point numbers similarly span a large dynamic range, but because the mantissa is represented by a finite number of bits, the precision for any given exponent is limited to a constant fraction of two raised to that exponent.

People normally either do not consider the voltages in translinear circuits, which are implicitly logarithmic representations of the various input and output signals, or at most consider them to be of little importance. However, from a computational point of view, the voltage signals in translinear circuits are directly analogous, in the digital domain, to representations called *logarithmic number systems* [63–66], in which numbers are represented internally by their binary logarithms to some finite precision. Many researchers [67–78] have proposed using logarithmic number systems in special-purpose digital signal processors for applications, such as digital filtering, FFT computation, and computer graphics, which typically require a large dynamic range and in which operations such as multiplication, division, squaring, and square-rooting occur more frequently than do addition and subtraction.

The appeal of such logarithmic number systems is that we can implement the operations of multiplication and division using only fixed-point adders and the operations of squaring and square-rooting using only shifters. However, in such digital arithmetic units, conversion between conventional number formats and the logarithmic number format is quite expensive, typically involving large lookup tables. Also, whereas multiplication and division are relatively inexpensive in such systems, addition and subtraction can only be approximated and involve additional lookup tables, making them quite cumbersome. By contrast, in translinear analog information-processing systems, conversion between the logarithmic (i.e., voltage) signal representation and the linear (i.e., current) signal representation is extremely inexpensive, requiring only a single translinear device. Consequently, with translinear circuits, operations like multiplication, division, squaring, and square-rooting are inexpensive *and* the operations of addition and subtraction, which we can implement simply using Kirchhoff's current law on a single wire, are also inexpensive.

Because of the logarithmic relationship that exists between the controlling voltage and the output current of a translinear device, we must ensure that the currents flowing through all translinear devices remain strictly positive at all times. In order to represent both positive and negative quantities by currents, we can follow one of two basic approaches. First, we can add an offset current, I_y, to a signal current, I_z, so that their sum, $I_z + I_y$, remain positive at all times, as shown in Fig. 2a. In this case, the signal current is a *bidirectional current*. Note that the condition that $I_z + I_y > 0$ implies that $I_z > -I_y$. Thus, while there is no restriction on the magnitude of positive values of I_z, negative values of I_z cannot exceed the magnitude of the offset current, I_y. Second, we can represent a quantity that can be both positive and negative as a *differential current*; that is, as the

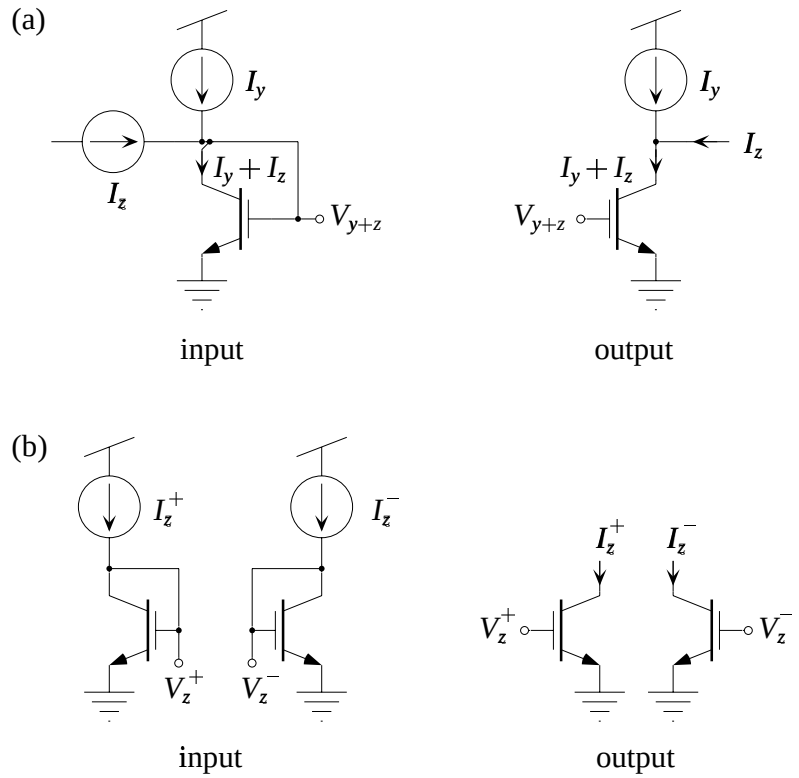


Figure 2: Translinear representations for quantities that can take on both positive and negative values. (a) The quantity, z, is represented by a *bidirectional current*, I_z, offset by another current, I_y, so that $I_z + I_y > 0$. (b) The quantity, z, is represented by a *differential current*, $I_z \equiv I_z^+ - I_z^-$, where $I_z^+ > 0$ and $I_z^- > 0$.

difference between two strictly positive components, each of which is represented independently as the ratio of a signal current to the unit current, as shown in Fig. 2b. In other words, we represent a number, z, as $z \equiv z^+ - z^-$, where

$$z^+ \equiv \frac{I_z^+}{I_u} > 0 \text{ and } z^- \equiv \frac{I_z^-}{I_u} > 0.$$

4 The Translinear Principle

In this section, we shall derive the *translinear principle* for a loop of ideal TEs and illustrate its use in analyzing translinear circuits. We shall then consider a loop of subthreshold MOS transistors with their bulks all connected to the common substrate potential to determine how the translinear principle is modified for such devices by the body effect.

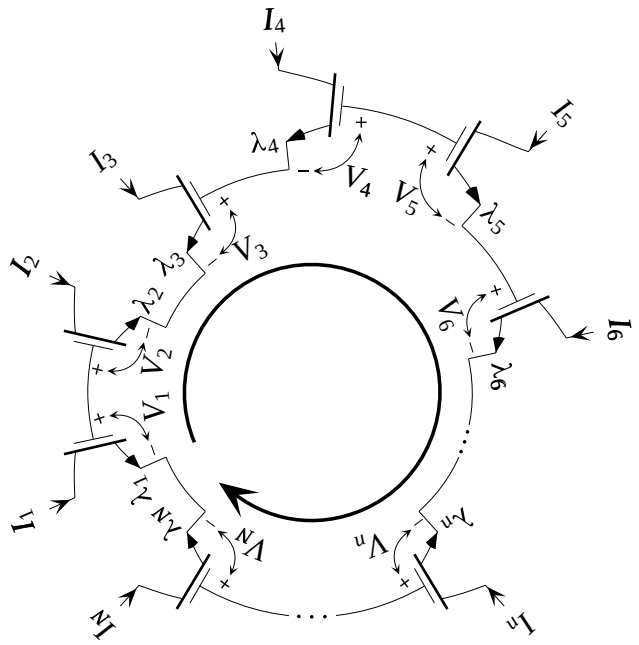


Figure 3: A conceptual translinear loop comprising N ideal TEs. The large arrow shows the clockwise direction around the loop. If a TE symbol's emitter arrow points in the direction opposite to that of the arrow, then we consider the element a *counterclockwise element*. If a TE symbol's emitter arrow points in the same direction as the large arrow, then the element is a *clockwise element.* The translinear principle states that the product of the currents flowing through the clockwise elements is equal to the product of the currents flowing through the counterclockwise elements.

4.1 Translinear Loops of Ideal Translinear Elements

Consider the closed loop of N ideal TEs, shown in Fig. 3. The large arrow shows the clockwise direction around the loop. If the emitter arrow of a TE points in the clockwise direction, we classify the TE as a *clockwise element.* If the emitter arrow of a TE points in the counterclockwise direction, we classify the TE as a counterclockwise element. Let us denote by CW the set of clockwise-element indices and by CCW the set of counterclockwise-element indices.

As we proceed around the loop in the clockwise direction, the gate-to-emitter voltage of a counterclockwise element corresponds to a voltage increase, whereas the gate-to-emitter voltage of a clockwise element corresponds to a voltage drop. One way of stating Kirchhoff's voltage law is that the sum of the voltage increases around a closed loop is equal to the sum of the voltage drops around the loop. Consequently, by applying Kirchhoff's voltage law around the loop of TEs shown in Fig. 3, we have that

$$\sum_{n \in \mathrm{CCW}} V_n = \sum_{n \in \mathrm{CW}} V_n. \tag{2}$$

By solving Eq. 1 for V in terms of I and substituting the resulting expression for each V_n in Eq. 2, we obtain

$$\sum_{n\in\mathrm{CCW}} \frac{U_\mathrm{T}}{\eta} \log \frac{I_n}{\lambda_n I_\mathrm{s}} = \sum_{n\in\mathrm{CW}} \frac{U_\mathrm{T}}{\eta} \log \frac{I_n}{\lambda_n I_\mathrm{s}}. \tag{3}$$

Assuming that all TEs are operating at the same temperature, we can cancel the common factor of U_T/η in all of the terms in Eq. 3 to obtain

$$\sum_{n\in\mathrm{CCW}} \log \frac{I_n}{\lambda_n I_\mathrm{s}} = \sum_{n\in\mathrm{CW}} \log \frac{I_n}{\lambda_n I_\mathrm{s}}. \tag{4}$$

Because $\log x + \log y = \log xy$, we can rewrite Eq. 4 as

$$\log \prod_{n\in\mathrm{CCW}} \frac{I_n}{\lambda_n I_\mathrm{s}} = \log \prod_{n\in\mathrm{CW}} \frac{I_n}{\lambda_n I_\mathrm{s}}. \tag{5}$$

By exponentiating both sides of Eq. 5 we get

$$\prod_{n\in\mathrm{CCW}} \frac{I_n}{\lambda_n I_\mathrm{s}} = \prod_{n\in\mathrm{CW}} \frac{I_n}{\lambda_n I_\mathrm{s}},$$

which we can rearrange to obtain

$$\prod_{n\in\mathrm{CCW}} \frac{I_n}{\lambda_n} = I_\mathrm{s}^{N_\mathrm{CCW}-N_\mathrm{CW}} \prod_{n\in\mathrm{CW}} \frac{I_n}{\lambda_n}, \tag{6}$$

where N_CCW and N_CW denote respectively the number of counterclockwise elements and the number of clockwise elements. Now, it is easy to see that, if $N_\mathrm{CW} = N_\mathrm{CCW}$, then Eq. 6 reduces to

$$\prod_{n\in\mathrm{CCW}} \frac{I_n}{\lambda_n} = \prod_{n\in\mathrm{CW}} \frac{I_n}{\lambda_n}, \tag{7}$$

which has no remaining dependence on temperature or device parameters. Equation 7 is the *translinear principle*, which can be stated as follows.

> In a closed loop of ideal TEs comprising an equal number of clockwise and counterclockwise elements, the product of the (relative) current densities flowing through the counterclockwise elements is equal to the product of the (relative) current densities flowing through the clockwise elements.

If each TE in the loop has the same value of λ, then Eq. 7 becomes

$$\prod_{n\in\mathrm{CCW}} I_n = \lambda^{N_\mathrm{CCW}-N_\mathrm{CW}} \prod_{n\in\mathrm{CW}} I_n,$$

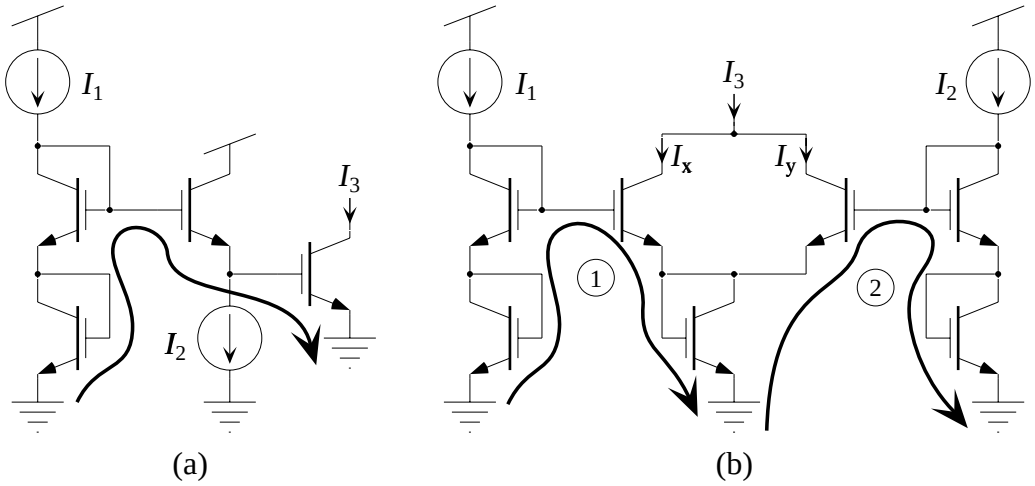


Figure 4: Two translinear-loop circuits. (a) A simple circuit with one translinear loop comprising two clockwise elements and two counterclockwise elements arranged in a stacked topology. (b) A circuit with two overlapping translinear loops each of which comprises two clockwise elements and two counterclockwise elements arranged in a stacked topology.

which, if $N_{\mathrm{CW}} = N_{\mathrm{CCW}}$, further reduces to

$$\prod_{n \in \mathrm{CCW}} I_n = \prod_{n \in \mathrm{CW}} I_n. \tag{8}$$

Equation 8 is an important special case of the translinear principle that can be stated as follows.

> In a closed loop of identical ideal TEs comprising an equal number of clockwise and counterclockwise elements, the product of the currents flowing through the counterclockwise elements is equal to the product of the currents flowing through the clockwise elements.

Note that the derivation of the translinear principle just described can be characterized as a *trans*lation of a *linear* set of algebraic constraints on the voltages in the circuit (i.e., Kirchhoff's voltage law applied around the loop of Fig. 3) into a product-of-power-law constraint on the currents flowing in the circuit. This characterization of the translinear principle is one way to state the second connotation of the word *translinear* originally intended by Gilbert [1, 10–12].

To illustrate the use of the translinear principle, we shall analyze the two translinear-loop circuits shown in Fig. 4. First, consider the circuit of Fig. 4a. This circuit has a single translinear loop comprising four identical TEs, two of which face in the clockwise direction and two of which face in the counterclockwise direction. Input current I_1 passes through both counterclockwise elements. Input current I_2 passes through one of the clockwise elements. The output current, I_3, passes

through the other clockwise element. Consequently, to analyze this circuit, we apply the translinear principle, as stated in Eq. 8, and write that

$$I_1^2 = I_2 I_3,$$

which we easily rearrange to obtain

$$I_3 = \frac{I_1^2}{I_2}.$$

Thus, the circuit of Fig. 4a is a squaring–reciprocal circuit.

Next, consider the circuit shown in Fig. 4b. This circuit has two overlapping translinear loops, each of which comprises four identical TEs with two in the clockwise direction and two in the counterclockwise direction. By Kirchhoff's current law, we have that the output current, I_3, is given by

$$I_3 = I_x + I_y. \tag{9}$$

In the first loop, input current I_1 passes through both counterclockwise elements. Intermediate current I_x passes through the first clockwise element and the output current, I_3, (i.e., $I_x + I_y$) passes through the second clockwise element. So, by the translinear principle, we have that

$$I_1^2 = I_x I_3,$$

which implies that

$$I_x = \frac{I_1^2}{I_3}. \tag{10}$$

In the second loop, input current I_2 passes through both clockwise elements. Intermediate current I_y passes through one of the counterclockwise elements and the output current, I_3, passes through the other counterclockwise element. So, by the translinear principle, we have that

$$I_2^2 = I_y I_3,$$

which implies that

$$I_y = \frac{I_2^2}{I_3}. \tag{11}$$

Substituting Eqs. 10 and 11 into Eq. 9, we have that

$$I_3 = \frac{I_1^2}{I_3} + \frac{I_2^2}{I_3},$$

which we can rearrange to find that

$$I_3^2 = I_1^2 + I_2^2.$$

By taking the square root of both sides of the preceding equation, we have that the output current, I_3, is given by

$$I_3 = \sqrt{I_1^2 + I_2^2}.$$

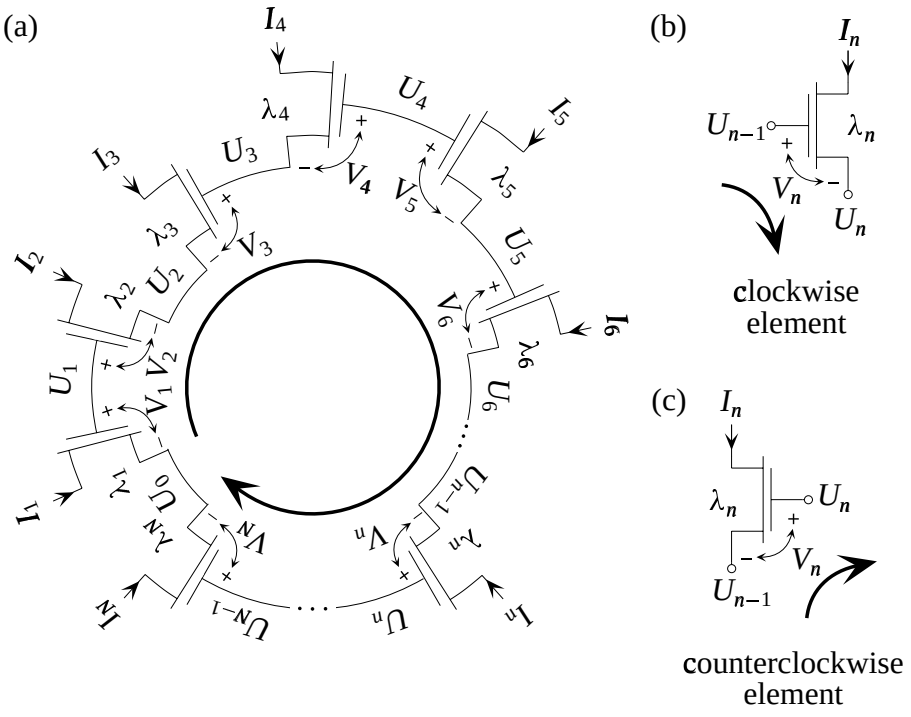


Figure 5: A translinear loop of subthreshold MOS transistors with their bulks tied to a common substrate potential. Here V_n refers to the gate-to-source voltage of the nth MOS transistor and U_n refers to the voltage on the nth node referenced to the common substrate potential. (a) A conceptual translinear loop comprising N subthreshold MOS transistors with their bulks tied to a common substrate. (b) A clockwise element is one whose gate-to-source voltage is a voltage drop in the clockwise direction around the loop. (c) A counterclockwise element is one whose gate-to-source voltage is a voltage increase in the clockwise direction around the loop.

4.2 Translinear Loops of Subthreshold MOS Transistors

Consider the closed loop of N saturated subthreshold MOS transistors whose bulks are all connected to a common substrate potential, shown in Fig. 5a. Here, V_n represents the gate-to-source voltage of the nth MOS transistor, and U_n is the voltage on the nth node relative to the substrate potential. Again, the large arrow in Fig. 5a, indicates the clockwise direction around the loop. As shown in Fig. 5b, we shall consider a clockwise element to be one whose gate-to-source voltage is a voltage drop in the clockwise direction around the loop. As shown in Fig. 5c, we shall consider a counterclockwise element to be one whose gate-to-source voltage is a voltage increase in the clockwise direction around the loop.

Recall that the channel current, I, of an nMOS transistor, operating in subthreshold, is given by

$$I = \lambda I_0 e^{\kappa V_g / U_T} \left(e^{-V_s / U_T} - e^{-V_d / U_T} \right), \tag{12}$$

where V_g is the gate-to-bulk voltage, V_s is the source-to-bulk voltage, V_d is the drain-to-bulk potential, λ is the W/L ratio of the transistor, I_0 is the subthreshold pre-exponential current factor, κ is the (incremental) capacitive divider ratio between the gate and the channel, and U_T is the thermal voltage, kT/q [79]. If the drain-to-source voltage is larger than about $4U_T$, then the transistor is saturated. Under these conditions, the second term in the parenthesis in Eq. 12 is negligible compared to the first one, which reduces Eq. 12 to

$$I = \lambda I_0 e^{(\kappa V_g - V_s)/U_T},$$

which has no remaining dependence on the drain-to-bulk potential.

Thus, if the nth MOS transistor is a clockwise element, we have that

$$I_n = \lambda_n I_0 e^{(\kappa U_{n-1} - U_n)/U_T},$$

which we can rearrange to find that

$$e^{U_n/U_T} = \left(e^{U_{n-1}/U_T}\right)^{\kappa} \left(\frac{\lambda_n I_0}{I_n}\right). \tag{13}$$

Equation 13 expresses a recurrence relationship between the nth node voltage to the $(n-1)$st node voltage for clockwise elements. On the other hand, if the nth MOS transistor is a counterclockwise element, we have that

$$I_n = \lambda_n I_0 e^{(\kappa U_n - U_{n-1})/U_T},$$

which we can rearrange to find that

$$e^{U_n/U_T} = \left(e^{U_{n-1}/U_T}\right)^{1/\kappa} \left(\frac{I_n}{\lambda_n I_0}\right)^{1/\kappa}. \tag{14}$$

Equation 14 likewise expresses a recurrence relationship between the nth node voltage and the $(n-1)$st node voltage for counterclockwise elements.

We can use the recurrence relationships, expressed in Eqs. 13 and 14, to build up the translinear-loop constraint equation for the subthreshold MOS translinear loop, shown in Fig. 5a, as follows. We begin at one of the nodes in the loop, say U_0, and proceed sequentially around the loop in the clockwise direction, recursively applying Eq. 13 or Eq. 14 to get to the next node, depending on whether the current element is clockwise or counterclockwise. When we encounter a clockwise element, we raise the partially formed translinear-loop equation to the κ power and multiply it by $\lambda_n I_0/I_n$, as expressed in Eq. 13. When we encounter a counterclockwise element, we raise the partially formed translinear-loop equation to the $1/\kappa$ power and multiply it by $(I_n/\lambda_n I_0)^{1/\kappa}$, as expressed in Eq. 14. Finally, when we return to the node with which we started, we stop and simplify the resulting expression.

To illustrate this process, we shall consider two simple subthreshold MOS translinear loops, shown in Fig. 6. Each of these loops comprises four transistors, two of which face in the clockwise

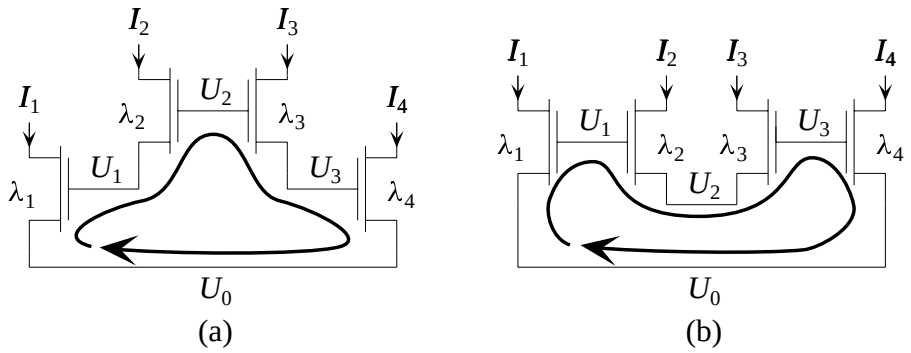


Figure 6: Two subthreshold MOS translinear loops comprising two clockwise transistors and two counterclockwise transistors. In each case, the bulks of all four transistors are tied to a common potential. (a) A *stacked* loop topology. (b) An *alternating* loop topology.

direction and two of which face in the counterclockwise direction. The first loop, shown in Fig. 6a, has a *stacked* topology; that is, all of the gate-to-source voltage drops are stacked up, one on top of the other. The second loop, shown in Fig. 6b has an *alternating* topology; that is, we alternate between clockwise and counterclockwise elements, as we go around the loop.

First, consider the stacked MOS translinear loop, shown in Fig. 6a. Starting with node U_0 and proceeding around the loop in the clockwise direction, we encounter two counterclockwise elements followed by two clockwise elements before we finish back at node U_0. Following the procedure just described, we have that

$$\underbrace{\Bigg(\underbrace{\Bigg(\underbrace{\Bigg(\underbrace{\Big(e^{U_0/U_\mathrm{T}}\Big)^{1/\kappa}\Big(\frac{I_1}{\lambda_1 I_0}\Big)^{1/\kappa}}_{e^{U_1/U_\mathrm{T}}}\Bigg)^{1/\kappa}\Big(\frac{I_2}{\lambda_2 I_0}\Big)^{1/\kappa}}_{e^{U_2/U_\mathrm{T}}}\Bigg)^{\kappa}\Big(\frac{\lambda_3 I_0}{I_3}\Big)}_{e^{U_3/U_\mathrm{T}}}\Bigg)^{\kappa}\Big(\frac{\lambda_4 I_0}{I_4}\Big) = e^{U_0/U_\mathrm{T}},$$

which we can simplify to get

$$\Big(e^{U_0/U_\mathrm{T}}\Big)^{1/\kappa}\left(\frac{I_1}{\lambda_1 I_0}\right)^{1/\kappa}\left(\frac{I_2}{\lambda_2 I_0}\right)\left(\frac{\lambda_3 I_0}{I_3}\right)\left(\frac{\lambda_4 I_0}{I_4}\right)^{1/\kappa} = \Big(e^{U_0/U_\mathrm{T}}\Big)^{1/\kappa}.$$

By canceling common factors and grouping the counterclockwise currents on the left-hand side of the equation and grouping the clockwise currents on the right-hand side of the equation, we obtain the following translinear-loop equation:

$$\underbrace{\left(\frac{I_1}{\lambda_1}\right)^{1/\kappa}\left(\frac{I_2}{\lambda_2}\right)}_{\mathrm{CCW}} = \underbrace{\left(\frac{I_3}{\lambda_3}\right)\left(\frac{I_4}{\lambda_4}\right)^{1/\kappa}}_{\mathrm{CW}}, \tag{15}$$

which has no remaining temperature dependence and no dependence on I_0, but does depend on the subthreshold slope factor, κ.

Next, consider the alternating MOS translinear loop, shown in Fig. 6b. Again, starting with node U_0 and proceeding around the loop in the clockwise direction, we first encounter a counterclockwise element followed by a clockwise element, followed by another counterclockwise element, followed by another clockwise element. Following the procedure just described, we have that

$$\underbrace{\underbrace{\underbrace{\underbrace{\left(e^{U_0/U_\mathrm{T}}\right)^{1/\kappa}\left(\frac{I_1}{\lambda_1 I_0}\right)^{1/\kappa}}_{e^{U_1/U_\mathrm{T}}}\left(\frac{\lambda_2 I_0}{I_2}\right)}_{e^{U_2/U_\mathrm{T}}}\right)^{1/\kappa}\left(\frac{I_3}{\lambda_3 I_0}\right)^{1/\kappa}}_{e^{U_3/U_\mathrm{T}}}\Bigg)^{\kappa}\left(\frac{\lambda_4 I_0}{I_4}\right) = e^{U_0/U_\mathrm{T}},$$

which we can simplify to get

$$\left(e^{U_0/U_\mathrm{T}}\right)\left(\frac{I_1}{\lambda_1 I_0}\right)\left(\frac{\lambda_2 I_0}{I_2}\right)\left(\frac{I_3}{\lambda_3 I_0}\right)\left(\frac{\lambda_4 I_0}{I_4}\right) = \left(e^{U_0/U_\mathrm{T}}\right).$$

By canceling common factors and grouping the counterclockwise currents on the left-hand side of the equation and grouping the clockwise currents on the right-hand side of the equation, we obtain the following translinear-loop equation:

$$\underbrace{\left(\frac{I_1}{\lambda_1}\right)\left(\frac{I_3}{\lambda_3}\right)}_{\mathrm{CCW}} = \underbrace{\left(\frac{I_2}{\lambda_2}\right)\left(\frac{I_4}{\lambda_4}\right)}_{\mathrm{CW}}, \tag{16}$$

which has no remaining temperature dependence, no dependence on I_0, *and* no dependence on κ.

From these examples, we can make a number of observations about subthreshold MOS translinear loops. First, if the number of clockwise elements is equal to the number of counterclockwise elements in a closed loop, then the e^{U_0/U_T} factor will cancel from both sides of the equation. In general, each time we traverse a clockwise element, we raise this factor to the κ power, and each time we traverse a counterclockwise element, we raise this factor to the $1/\kappa$ power. Thus, if there are N_CW clockwise elements and N_CCW elements, the factor of e^{U_0/U_T} will appear on the left-hand side of the translinear-loop equation raised to the $\kappa^{N_\mathrm{CW}-N_\mathrm{CCW}}$ power, which is equal to unity if $N_\mathrm{CW} = N_\mathrm{CCW}$. Therefore, this factor, which appears on both sides of the final translinear-loop equation will cancel.

Second, if the number of clockwise elements is equal to the number of counterclockwise elements, then the translinear-loop equation will be independent of I_0. To see why, consider first what happens to the power to which I_0 is raised after we traverse a clockwise element followed by a counterclockwise element. Suppose that I_0 appears in the initial translinear-loop equation raised to the α power. After traversing a clockwise element, we will have I_0 raised to the $\kappa\alpha + 1$. Then,

after traversing a counterclockwise element, we will have I_0 raised to the $(\kappa\alpha + 1)/\kappa - 1/\kappa = \alpha$ power. Thus, the power to which I_0 is raised in the translinear-loop equation remains unchanged when we pass from a sequence of clockwise elements to a sequence of counterclockwise elements. Next, consider what happens to the power to which I_0 is raised after we traverse a counterclockwise element followed by a clockwise element. Again, suppose I_0 appears in the initial translinear-loop equation raised to the α power. After traversing a counterclockwise element, we will find I_0 raised to the $\alpha/\kappa - 1/\kappa$ power. Then, after traversing a clockwise element, we will have I_0 raised to the $\kappa\,(\alpha/\kappa - 1/\kappa) + 1 = \alpha$ power. Thus, the power to which I_0 is raised in the translinear-loop equation also remains unchanged when we pass from a sequence of counterclockwise elements to a sequence of clockwise elements. Therefore, the power to which I_0 is raised in the translinear-loop equation remains unchanged when we pass through a boundary between a sequence of clockwise elements and a sequence of counterclockwise elements.

Now, if there are an equal number of clockwise and counterclockwise elements, then there will be at least two such boundaries; this lower bound is achieved when the loop has a purely stacked topology. If there are $2N$ elements in the loop (i.e., $N_{\mathrm{CW}} = N_{\mathrm{CCW}} = N$), then there can be at most N such boundaries; this upper bound is achieved when the loop has a purely alternating topology. Because the elements at the boundaries between runs of clockwise and counterclockwise elements do not alter the power to which I_0 is raised in the translinear-loop expression, we can drop the elements at each of these boundaries from the sequence in determining the overall power to which I_0 is raised. However, the elements adjacent to those that we have omitted then form another such boundary. Consequently, if there is a clockwise element in the loop for each counterclockwise element, then the overall power to which I_0 is raised as we go around the loop remains unaltered. Moreover, when we begin accumulating the translinear-loop expression, I_0 does not appear in the expression (i.e., it is raised to the zeroth power). Therefore, because the power to which I_0 is raised begins at zero and it remains unaltered for a loop comprising an equal number of clockwise and counterclockwise elements, the overall translinear loop expression remains independent of I_0. An identical argument holds if all of the MOS transistors have the same W/L ratio (i.e., $\lambda_1 = \cdots = \lambda_N = \lambda$); that is, if all of the transistors have the same W/L ratio and if the number of clockwise elements is equal to the number of counterclockwise elements, then the translinear-loop equation is independent of the transistors' common W/L ratio.

Finally, consider a purely alternating subthreshold MOS translinear loop comprising an equal number of clockwise and counterclockwise elements with their bulks connected to a common potential. For such a loop, the translinear-loop equation will be independent of κ. To see why, consider the loop-equation construction procedure. If we begin by traversing a counterclockwise element, the first current factor in the equation will be raised to the $1/\kappa$ power. After traversing the second element, which by hypothesis is a clockwise element, the first current factor will be raised to the κ power, canceling the initial $1/\kappa$. The second current factor will be added to the product raised to the first power. After traversing the third element, the first two current factors will be again raised to the $1/\kappa$ power as will the third current factor. After going through the fourth element, we raise the first three current factors to the κ power, again canceling the $1/\kappa$ power on each factor from the previous step. A forth current factor is then added to the partially formed product, raised

to the first power. Thus, in an alternating loop, we alternate between raising each factor to the $1/\kappa$ power and raising each one to the κ power, effectively removing the κ dependence from the partially formed product after every other step. Moreover, if there are an equal number of clockwise and counterclockwise elements in such a loop, then it follows that the final translinear-loop equation will be independent of κ, because there must be an even number of steps. A similar argument would hold if we begin with a clockwise element. This result has been demonstrated previously using other arguments by Vittoz [80] and by Andreou and Boahen [81].

With these considerations in mind, we can simplify our translinear-loop equation construction procedure for loops that comprise an equal number of clockwise and counterclockwise subthreshold MOS transistors whose bulks are all tied to a common potential. First, we do not have to write down the initial and final e^{U_0/U_T} factors; instead, we can replace them by unity, effectively dividing out the factor that will be common to both sides of the equation ahead of time. Next, we can dispense with keeping track of all of the I_0 factors, because we have shown that the final expression will be independent of I_0. To summarize this reduced procedure, we pick a starting point in the loop and begin the translinear loop expression with unity. Then, we proceed around the loop from node to node in the clockwise direction. If we traverse a clockwise element, we raise the partially formed expression to the κ power and then we multiply it by λ_n/I_n. If we traverse a counterclockwise element, we raise the partially formed expression to the $1/\kappa$ power and multiply by $(I_n/\lambda_n)^{1/\kappa}$. When we arrive back at the starting node, we equate the product that we have accumulated to unity and simplify it as necessary.

5 ABC's of Translinear-Loop–Circuit Synthesis

In this section, we shall give a brief overview of the basics of translinear-loop circuit synthesis. As with all synthesis problems, the task of constructing a translinear circuit that implements some desired functionality is underconstrained. For any given function, there will be a variety of circuit solutions with design decisions to be made and many trade-offs to consider. Thus, our brief discussion cannot, by any means, be exhaustive. Rather, we shall attempt to make the basic procedure clear and we shall illustrate it with two simple examples. In the process, we shall discuss some design decisions and trade-offs.

5.1 Synthesizing Static Translinear-Loop Circuits

The basic procedure for synthesizing translinear-loop circuits can be described as follows. First, we *acquire* a set of translinear-loop equations from the relationship(s) that we want to implement. Next, we *build* a translinear loop for each of the translinear-loop equations. Next, we *bias* each of the translinear loops. Finally, if possible, we *consolidate* the resulting circuits by merging some of the loops. We shall discuss each of these steps in turn, then we shall use them to synthesize two simple translinear-loop circuits, a squaring circuit and a two-quadrant multiplier.

Acquiring a set of translinear-loop equations. The starting point for synthesizing a translinear-loop circuit is a static linear or nonlinear mapping between dimensionless variables. The class of translinear circuits is capable of embodying a wide range of useful linear and nonlinear relationships. However, not all functions are directly implementable by translinear circuits; we can directly realize products, quotients, power-law relationships, polynomials, rational functions, and various combinations of such relationships. In many cases, we may need to find an acceptable approximation for one or more nonlinear functions in terms of polynomials, rational functions, continued fractions, or some other suitable mathematical form before we can realize the required relationship with translinear circuits. In his book on translinear circuits, Seevinck [38] provides a good discussion of suitable approximation techniques and approximations of various transcendental functions.

Once we have obtained a set of relationships that can be realized with translinear circuits, we then represent each of the dimensionless quantities as the ratio of a signal current to the unit current or as the ratio of a differential current to the unit current, as described in Section 3. Then, we decompose the resulting equations into a set of translinear-loop equations of the form of Eq. 7. In the decomposition process, it is sometimes convenient to introduce intermediate currents, which serve to parameterize some of the relationships, allowing us to further decompose the system of equations.

Building the translinear loops. Once we have a set of translinear-loop equations, we construct a closed loop of TEs for each one. In general, there will be more than one translinear loop that implements any given translinear-loop equation. Our choices of loop topology and current ordering must be guided by experience and other system-level design considerations. For instance, loops with an alternating topology are better than stacked loops for systems that require a low power-supply voltage. On the other hand, stacked loops are easier to bias in the case that the same current must pass through multiple TEs that face in the same direction. In a stacked loop, we only have to supply a single copy of the input current to the circuit and we can pass the same current from one element to the next in a stack of TEs. In an alternating loop, there are no runs of clockwise or counterclockwise TEs, so if we must pass the same current through N TEs facing in the same direction, we must supply N matched copies of the input current to the circuit.

Biasing the translinear loops. The process of biasing a translinear loop involves forcing input currents into the emitter or collector of each input TE in the loop and arranging some type of local negative feedback around it, adjusting its gate-to-emitter voltage so that the TE passes the input current. Once again, there are many possible feedback arrangements that will properly bias each TE in any given loop. In some cases, we may even use operational amplifiers to bias a translinear loop. Here, we shall consider only the three simplest possibilities, which are shown in Fig. 7.

Figure 7a shows the ubiquitous *diode connection*. Here, we force a current into the collector of a counterclockwise TE, which corresponds to a voltage increase, and we feed the collector voltage back to the gate. Any mismatch between the input current and the TE's collector current causes the gate voltage to charge up or down in such a way to reduce the mismatch. If the collector current is bigger than the input current, the gate will discharge, reducing the gate-to-emitter voltage

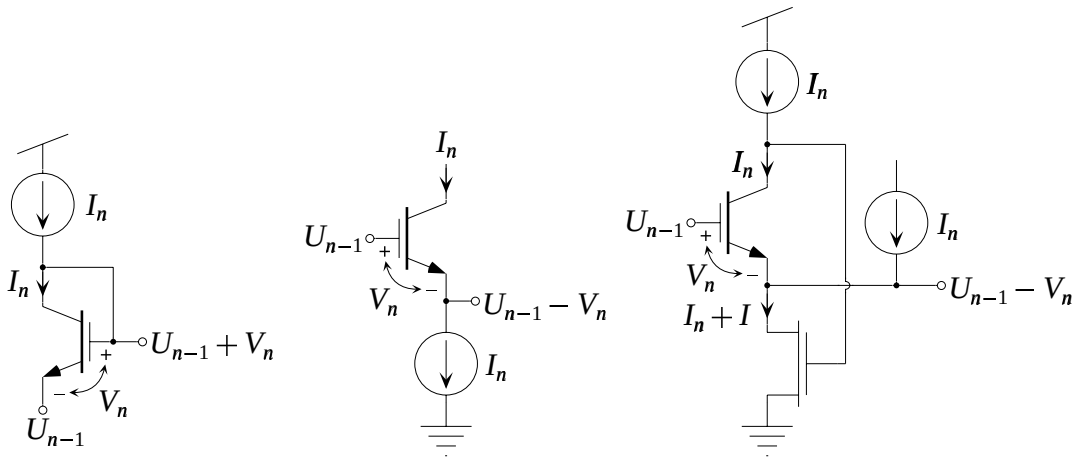


Figure 7: Three simple biasing arrangements for TEs. (a) Collector current forcing with the diode connection. (b) Emitter current forcing with the emitter-follower connection. (c) Collector current forcing with the Enz–Punzenberger (EP) connection.

thereby reducing the collector current. If the collector current is smaller than the input current, the gate will charge up, increasing the gate-to-emitter voltage, thereby increasing the collector current. Of course, we can introduce additional circuitry between the collector and the gate, such as one or more buffer stage, as long as changes in the collector voltage induce like changes in the gate voltage. In some cases, we actually use other TEs in the loop with their input-current sources to form emitter-follower buffer stages in making a diode connection. In some cases, we may introduce buffer stages to eliminate base-current errors in bipolar translinear-loop circuits.

Figure 7b shows an *emitter-follower connection*. Here, we force a current out of the emitter of a clockwise TE, which corresponds to a voltage drop. In such an arrangement, for any given gate voltage, the emitter voltage will adjust itself up or down so that the emitter current just balances the input current. If the emitter current is larger than the input current, the emitter voltage will charge up, reducing the gate-to-emitter voltage, thereby reducing the emitter current, until the currents match each other. If the input current is larger than the emitter current, the emitter will be discharged, increasing the gate-to-emitter voltage, thereby increasing the emitter current until the currents balance.

Figure 7c shows a simple alternative to the emitter-follower connection for biasing clockwise TEs. Here, we force a current into the collector of a clockwise TE and we feed the collector voltage back through another transistor to adjust the emitter current. An *n*MOS transistor is shown in Fig. 7c, but a bipolar transistor could be used instead. A similar feedback arrangement (i.e., forcing the collector current by feedback to the emitter terminal) involving operational amplifiers has been used in biasing translinear circuits for many years [10]. The use of this particularly elegant

implementation of such a feedback arrangement in the context of translinear-circuit biasing appears to have been first proposed by Enz and Punzenberger [82] to bias low-voltage log-domain filters. Consequently, we shall refer to this connection as the *Enz–Punzenberger* (EP) connection. For a given gate voltage, any imbalance between the collector current and the input current will cause the feedback transistor to adjust the gate-to-emitter voltage in such a way as to reduce the imbalance. If the input current is too large, the collector voltage will increase, causing the feedback transistor to pull a larger current out of the emitter. Conversely, if the collector current is to large, the collector voltage will decrease, reducing the amount of current flowing through the feedback transistor. This decreased current, in turn, will cause the emitter to charge up, reducing the gate-to-emitter voltage, thereby reducing the collector current. Note that if some additional current I is injected into the emitter node, the collector voltage will adjust itself so that the feedback transistor sinks both the current flowing through the TE and the additional current. This feature of the EP connection greatly facilitates the biasing of translinear loops with an alternating topology.

In general, we can bias any translinear loop using only two of the three simple arrangements of Fig. 7; we can use the diode connection for biasing counterclockwise TEs and we can use *either* the emitter-follower connection *or* the EP connection to bias the clockwise TEs. In general, the emitter-follower connection involves only one node, whereas the EP connection is involves two nodes, which can cause more complicated settling behavior with the EP connection. On the other hand, in an alternating translinear loop, by using the diode connection to bias the counterclockwise elements and the EP connection to bias the clockwise elements, we are always forcing collector currents and taking outputs from collector currents. This uniform use of collector currents allows us to freely use translinear devices whose emitter current and collector current are not nearly the same, such as the *compatible lateral bipolar transistor* (CLBT), which is always available in *any* CMOS process [83]. Such devices have at least two collectors, a lateral collector and a parasitic vertical collector, each of which collect only a finite fraction of the emitter current.

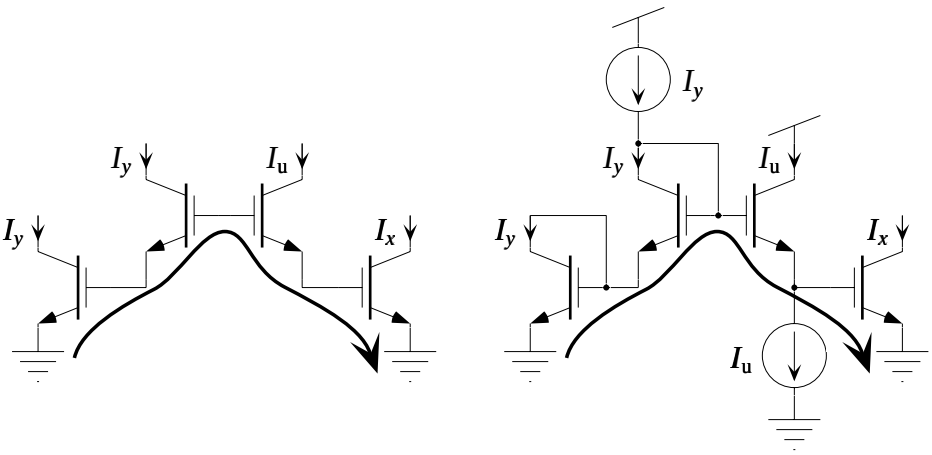
Consolidating the circuit. In some cases, after we have biased each of the translinear loops in the circuit, we will recognize some redundancy between the loops in the circuit. For example, if two TEs in different loops pass the same current and are at the same voltage level, then these devices are redundant and may be shared between the loops. Such consolidation is usually a good idea, because it usually results in smaller circuits and fewer opportunities for errors resulting from device mismatch.

5.2 Synthesis of a Translinear Squaring Circuit

Suppose that we want to implement a squaring operation with a strictly positive input using translinear-loop circuits. That is, we want to find a translinear-loop circuit that implements the relationship

$$x = y^2, \tag{17}$$

where $x > 0$ and $y > 0$ are dimensionless quantities. Here y is the independent variable (i.e., the input) and x is the dependent variable (i.e., the output). First, we represent x by I_x/I_u and y by



(a) (b)

Figure 8: Synthesis of a translinear squaring circuit based on a stacked translinear loop. (a) A stacked translinear loop that implements Eq. 18. (b) One possible biasing scheme.

I_y/I_u, where I_u is the unit current. Then, we substitute these definitions of x and y into Eq. 17, getting

$$\frac{I_x}{I_u} = \left(\frac{I_y}{I_u}\right)^2,$$

which we can easily rearrange to obtain the following translinear-loop equation:

$$\underbrace{I_x I_u}_{\text{CW}} = \underbrace{I_y^2}_{\text{CCW}}. \tag{18}$$

Next, to implement Eq. 18, we need to select a translinear loop comprising four TEs, two facing in the counterclockwise direction and two facing in the clockwise direction. Input current I_y passes through both of the counterclockwise TEs while I_u passes through one of the clockwise elements and I_x passes through the other. Figure 8a shows a stacked loop that implements Eq. 18. One possible biasing arrangement for the stacked loop is shown in Fig. 8b; here, we have diode connected each of the counterclockwise elements and we have used an emitter-follower connection for one of the clockwise elements. Because the counterclockwise elements come in sequence in the stacked loop arrangement, we can effectively reuse the input current, I_y, by passing the current from the emitter of one counterclockwise TE into the collector of the other one. Note that the resulting circuit is the same as the one shown in Fig. 4a.

Figure 9a shows an alternating loop that also implements Eq. 18. We shall consider two possible biasing arrangements for the alternating loop. Figure 9b shows an arrangement based on diode connections and an emitter-follower connection. Note that, because the counterclockwise elements

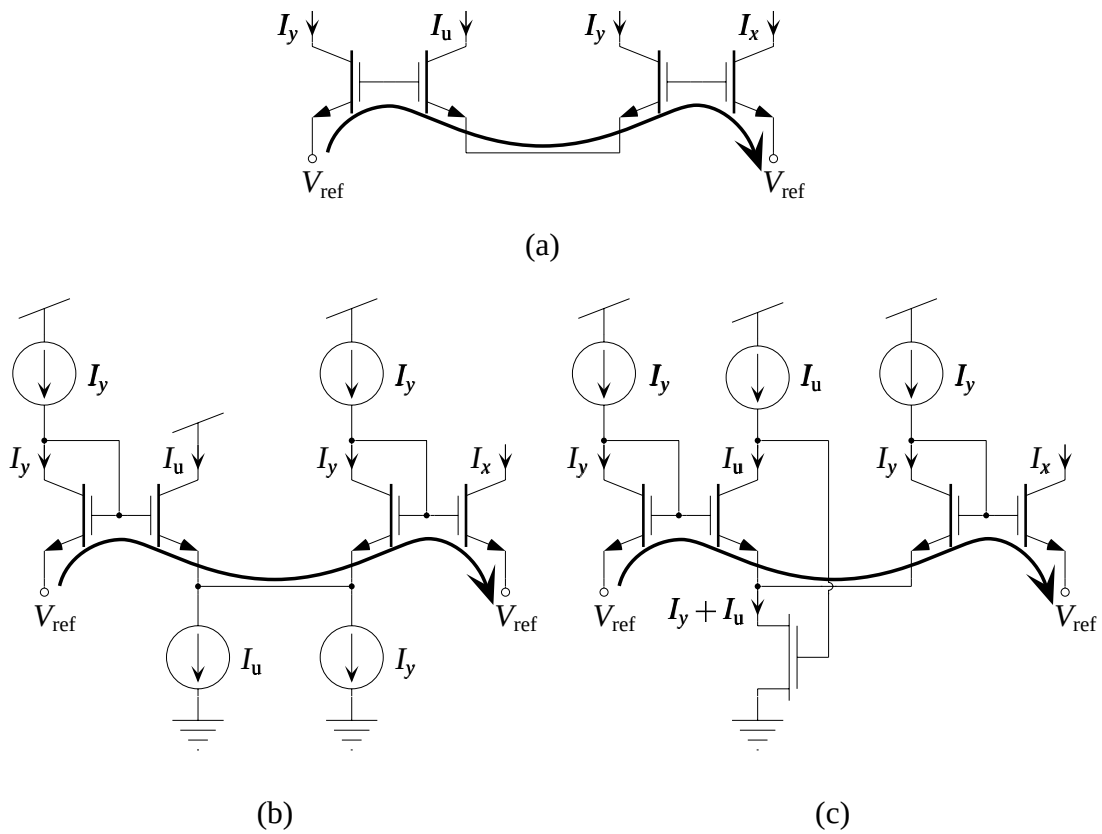


Figure 9: Synthesis of a translinear squaring circuit based on an alternating translinear loop. (a) An alternating translinear loop that implements Eq. 18 (b) A biasing scheme on diode-connections and emitter-follower connections. Note that we need to supply three matched copies of I_y, including two current sources and one current sink. (c) A biasing scheme based on diode connections and the EP connection. By using the EP connection, we only force collector currents and we only need to supply two matched copies of I_y, both of which are current sources.

are separated by a clockwise element, we must now supply a separate copy of I_y to each one. Also, because I_y also flows out of the emitter of the second counterclockwise element, to bias the clockwise element that passes I_u properly, we must sink I_y out of the central emitter node in addition to I_u. Figure 9c shows a biasing arrangement based on diode connections and an EP connection. Here, while we still have to supply two matched copies of I_y to the circuit, we are not required to also supply a matched current sink; the EP feedback connection will adjust the gate of the feedback transistor to compensate for the extra I_y flowing into the common-emitter node. For both biasing schemes, the exact value of the voltage V_{ref} is not critical—it should be high enough allow an adequate swing on the common-emitter node while keeping the current-sinking devices acting properly.

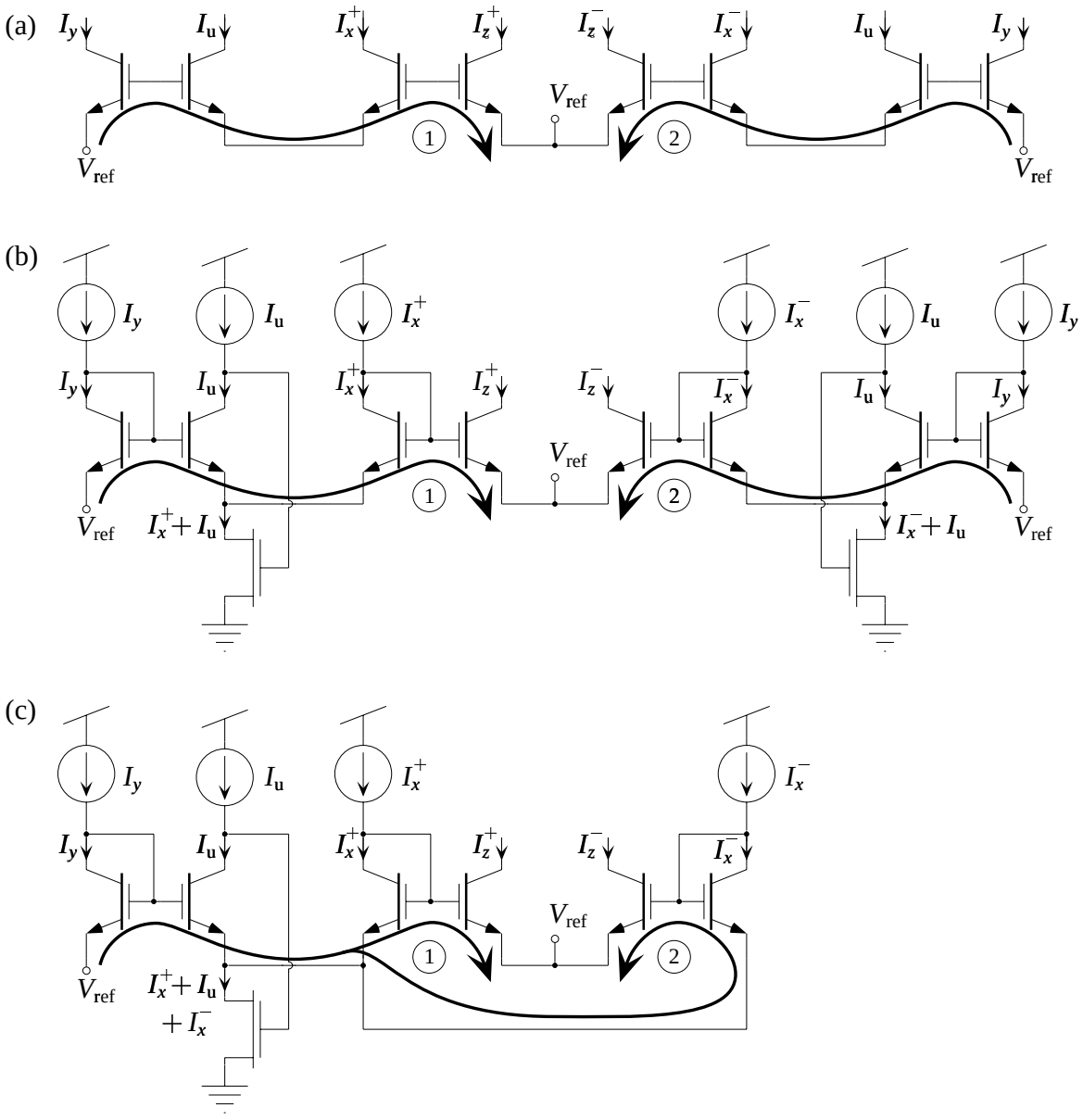


Figure 10: Synthesis of a two-quadrant translinear multiplier based on two alternating translinear loops. (a) A pair of alternating translinear loops that implement $I_u I_z^+ = I_y I_x^+$ and $I_u I_z^- = I_y I_x^-$. (b) A biasing scheme based on collector-current forcing with diode connections and EP connections. (c) The final consolidated two-quadrant translinear multiplier circuit. Here we could share the I_y and I_u circuitry between the two translinear loops.

5.3 Synthesis of a Two-Quadrant Translinear Multiplier

Suppose that we want to implement a circuit that multiplies two quantities, x and y. Further, suppose that x can be either positive or negative and that y is strictly positive. Thus, their product, z, which is given by

$$z = xy, \tag{19}$$

can be either positive or negative. We shall represent y by I_y/I_u and we use a differential representation for x and z, as described in Section 3; that is, we represent x by

$$x = x^+ - x^-,$$

where $x^+ \equiv I_x^+/I_\mathrm{u}$ and $x^- \equiv I_x^-/I_\mathrm{u}$. Likewise, we represent z by

$$z = z^+ - z^-,$$

where $z^+ \equiv I_z^+/I_\mathrm{u}$ and $z^- \equiv I_z^-/I_\mathrm{u}$.

Next, we substitute these definitions for x, y, and z into Eq. 19 to get

$$\left(\frac{I_z^+}{I_\mathrm{u}} - \frac{I_z^-}{I_\mathrm{u}}\right) = \left(\frac{I_x^+}{I_\mathrm{u}} - \frac{I_x^-}{I_\mathrm{u}}\right)\left(\frac{I_y}{I_\mathrm{u}}\right),$$

which we can rearrange to obtain

$$I_\mathrm{u} I_z^+ - I_\mathrm{u} I_z^- = I_y I_x^+ - I_y I_x^-.$$

One straightforward way to decompose this equation into a pair of translinear-loop equations is to equate individually the positive and negative terms on each side of the equation. Using this decomposition, we obtain the following pair of translinear-loop equations:

$$\underbrace{I_\mathrm{u} I_z^+}_{\mathrm{CW}} = \underbrace{I_y I_x^+}_{\mathrm{CCW}} \qquad \text{and} \qquad \underbrace{I_\mathrm{u} I_z^-}_{\mathrm{CW}} = \underbrace{I_y I_x^+}_{\mathrm{CCW}}. \tag{20}$$

Figure 10a shows a pair of translinear loops with alternating topologies that implements Eq. 20. Figure 10b shows one possible biasing arrangement for these loops; we use diode connections for each of the counterclockwise elements and EP connections for each of the clockwise elements. Again, the exact value of the voltage V_ref is not critical—it should be high enough allow an adequate swing on the common-emitter node while keeping the feedback transistor acting properly. Note that in each loop, we have a copy of I_y forced into a diode-connected TE whose emitter is fixed at V_ref. Thus, we can eliminate one of these stages and connect the diode-voltage to both loops. Additionally, we supply a copy of I_u to both loops, and as we just observed, the gate of both TEs will be at the same potential. Thus, we can eliminate one of the I_u states, too. The consolidated two-quadrant multiplier is shown in Fig. 10c.

6 The Multiple-Input Translinear Element

We have recently described a new translinear circuit primitive, called the *multiple-input translinear element* (MITE) [84,85]. Such an element produces an output current, I, that is exponential in a weighted sum of its K input voltages, V_1 through V_K, given by

$$I = \lambda I_s e^{\left(\sum_{k=1}^{K} w_k V_k - U\right)/U_T}, \tag{21}$$

where V_k is the kth input voltage, w_k is a dimensionless positive weight that scales V_k, and U is the emitter voltage of the MITE. Here I_s, λ, and U_T are the same as they were for the ideal TE. So defined, the MITE has K different *trans*conducances, each of which is *linear* in the MITE's output current.

Figure 11a shows a circuit symbol for an ideal K-input MITE. This symbol looks like an ideal TE whose gate voltage is set by a K-input capacitive voltage divider, where the kth divider ratio is given by a nearby w_k. The inputs do not need to be capacitive, but we shall assume that the input terminals draw a negligible amount of DC current and that we can control the values of the weights proportionally. In many cases, we shall be interested primarily in the number of identical unit weights, each with value w, coupling an input voltage into a MITE rather than the actual weight values involved. In such cases, we shall omit the w associated with each of the inputs.

Figures 11b through 11g show six different practical circuit implementations of the MITE. For the first of these MITEs, shown in Fig. 11b, we use a resistive voltage divider to implement the weighted voltage summation and a bipolar transistor to implement the exponential voltage-to-current transformation. In this case, the weight associated with each input is proportional to the conductance through which that input couples into the base of the bipolar. Here, we must buffer the input voltages into the resistive network so, in a circuit, the network neither supplies current to nor sinks current from the input nodes. This resistor-bipolar circuit is only a good MITE implementation over those collector currents for which the base impedance of the bipolar transistor is much greater than the resistances in the resistive network. When the base impedance becomes comparable to the resistances in the resistor network, the base voltage is clamped by the base-emitter junction and the collector current then increases only linearly, instead of exponentially, with the input voltages.

In subthreshold, the drain current of the K-input floating-gate MOS (FGMOS) transistor is proportional to the exponential of a weighted sum of its K control-gate voltages [61]. Consequently, we can implement a MITE using a single subthreshold FGMOS transistor, as shown in Fig. 11c. In this case, the weight of each input is proportional to the capacitance through which that input couples into the floating gate. The subthreshold FGMOS transistor is a good MITE implementation over the entire range of subthreshold currents. The main limitation of the subthreshold FGMOS transistor as a MITE is the existence of a parasitic gate-to-drain capacitance, which results from a small region of overlap between the polysilicon gate and the drain diffusion region that arises during processing. Because the gate of a FGMOS transistor is floating, an increase in the drain voltage couples into the floating gate through this overlap capacitance, thereby increasing the subthreshold drain current exponentially. In principle, we can decrease this coupling as much as we like by

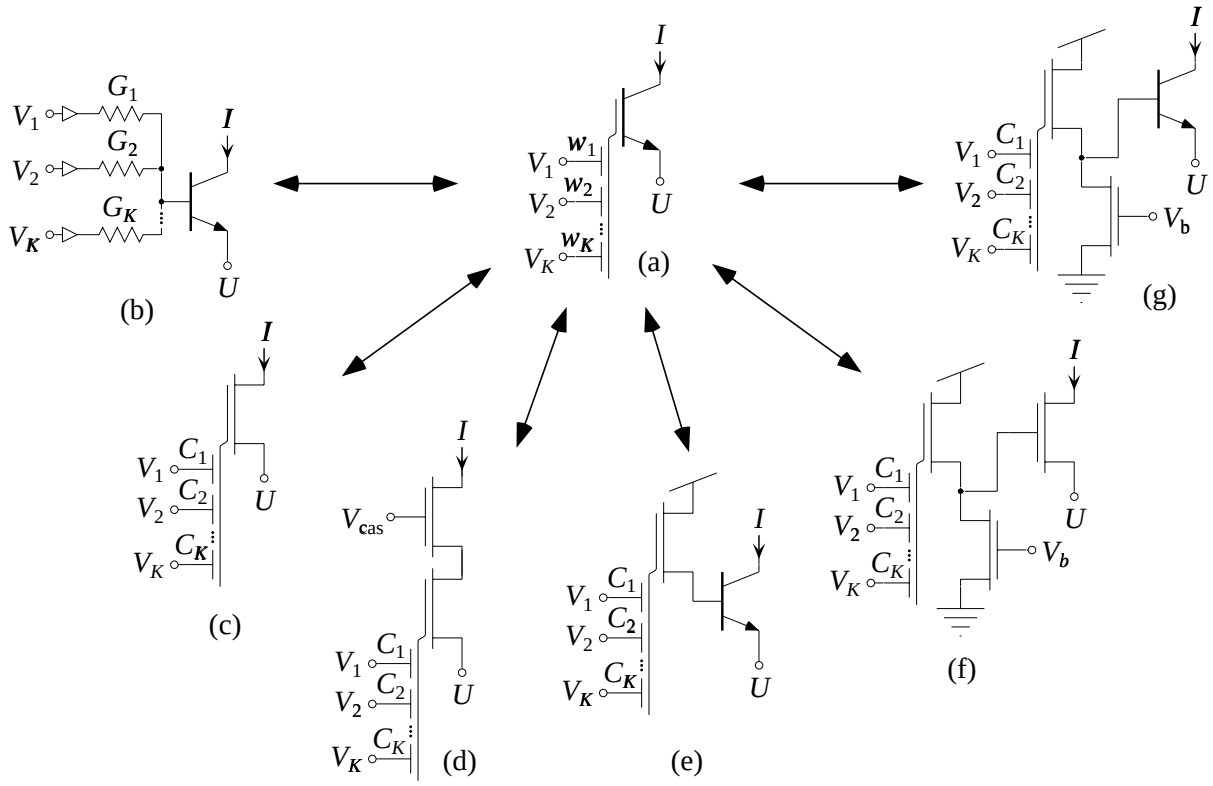


Figure 11: Multiple-input translinear elements (MITEs). (a) Circuit symbol for an ideal K-input MITE. Such an element produces an output current that is exponential in a weighted sum of its input voltages. Parts b through g show six different MITE implementations comprising (b) a resistive voltage divider and a bipolar transistor, (c) a single subthreshold floating-gate MOS (FGMOS) transistor, (d) a cascoded subthreshold FGMOS transistor, (e) a subthreshold FGMOS transistor and a bipolar transistor, (f) a floating-gate source follower and a subthreshold MOS transistor, and (g) a floating-gate source follower and a bipolar transistor. For each of the five FGMOS MITE implementations, shown in parts c through g, we can use the amount of floating-gate charge to store electronically adjustable, nonvolatile multiplicative scale factors that we can use to build adaptive information-processing systems or to compensate for device mismatch.

making the FGMOS transistor narrower (thereby decreasing the overlap capacitance) or by making the control-gate capacitances larger (thereby increasing the total floating-gate capacitance and, hence, decreasing the drain capacitive-divider ratio), or by using both techniques. However, in practice, neither of these solutions are attractive. A better solution to this problem is to cascode the subthreshold FGMOS transistor, as shown in Fig. 11d. We can think of the cascode transistor as a source follower with a constant input voltage, V_{cas}; thus, it fixes the drain voltage of the FGMOS transistor (i.e., the source follower's output voltage), effectively reducing the change

in current through both transistors resulting from a change in the drain voltage of the cascode transistor. The cascoded subthreshold FGMOS transistor is an excellent MITE implementation over the subthreshold range of currents.

Figure 11e depicts a two-transistor MITE comprising a K-input subthreshold FGMOS transistor and a bipolar transistor. Intuitively, this bipolar-FGMOS MITE works as follows. The subthreshold FGMOS transistor produces a current that is exponential in the weighted sum of the input voltages; again, the weight of each input is proportional to the capacitance through which that input couples into the floating gate. The bipolar transistor then acts as a current-gain stage by multiplying the subthreshold FGMOS transistor current by the bipolar's forward current gain. Consequently, the upper end of the current range over which this two-transistor circuit is a good MITE implementation is extended over that of the subthreshold MOS transistor by the bipolar's current gain, β. Because the drain of the FGMOS transistor is held at a fixed potential, this MITE is insensitive to the parasitic drain-overlap capacitance.

The final two MITEs, shown in Figs. 11f and 11g, are similar—each comprises a two-transistor FGMOS source follower and a third transistor that has an exponential current–voltage characteristic. Intuitively, the floating-gate voltage develops as a weighted sum of the K input voltages via a capacitive voltage divider. In the source-follower configuration, the FGMOS transistor's source voltage is approximately a linear function of the floating-gate voltage. Consequently, the source voltage is also a weighted sum of the input voltages. The third transistor then generates a current that is exponential in this source voltage. In the MITE of Fig. 11f, the exponential element is a subthreshold MOS transistor, whereas, in that of Fig. 11g, the exponential element is a bipolar transistor. Because the drains of the FGMOS transistors are held at a fixed potential, these MITEs also do not suffer from the drain-overlap capacitance problem.

Because the source-follower circuit configuration does not depend on the form of the current–voltage relationship of the MOS transistor, these three-transistor circuits are good MITE implementations even when we bias the FGMOS source follower with an above-threshold current. For the circuit of Fig. 11f, biasing the FGMOS source follower with an above-threshold current allows us to make the output MOS transistor as wide as necessary to get a larger range of exponential currents without having to make the FGMOS transistor, and, hence, the floating-gate capacitance large. The above-threshold bias gives the FGMOS source follower enough bandwidth to drive the large gate capacitance of a wide output MOS transistor. The circuit of Fig. 11g is a good MITE implementation only when the base current is negligible compared with the source-follower bias current. Thus, for the circuit of Fig. 11g, biasing the FGMOS source follower with above-threshold currents allows us to operate this MITE at high current levels and, thus, potentially with high bandwidths.

For each of the five FGMOS-transistor–based MITE implementations just described, the floating-gate charge linearly shifts the weighted sum of the control-gate voltages. When mapped through the exponential, this voltage offset translates into a multiplicative factor that scales the output current. Thus, we can think of the floating-gate charge as determining an electronically adjustable λ parameter, which we can use to store adaptable weights for building learning systems or to compensate for scale-factor errors resulting from device mismatch. None of the FGMOS-based MITE implementations, except for the single subthreshold FGMOS transistor, is affected adversely by the

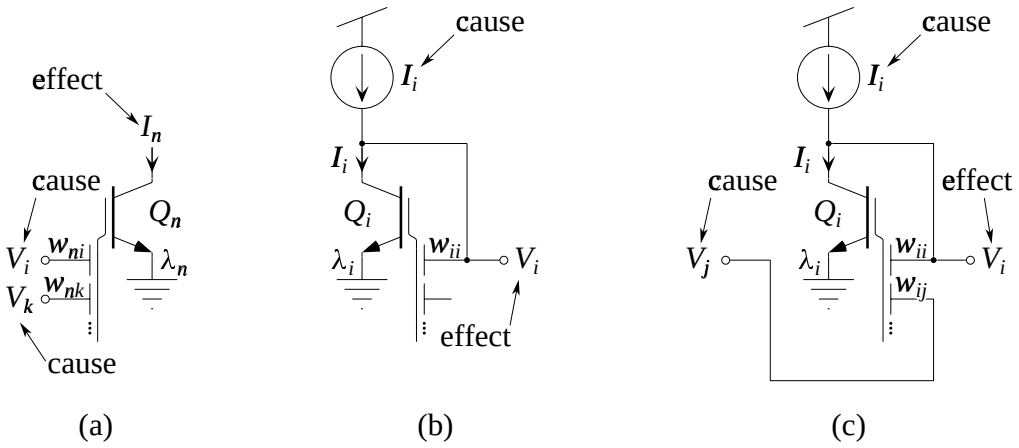


Figure 12: Three basic circuit stages, each comprising a single MITE. (a) A voltage-in, current-out (VICO) stage. (b) A current-in, voltage-out (CIVO) stage. (c) A voltage-in, voltage-out (VIVO) stage.

parasitic overlap capacitances.

7 Multiple-Input Translinear Element Networks

In this section, we introduce three basic circuit stages, each constructed from a single MITE. These three circuit stages are the bricks from which we build a class of low-voltage translinear circuits, which we call *MITE networks*, that are equivalent to the class of translinear-loop circuits. Then, we shall examine how we can compose these stages to make translinear circuits.

7.1 Basic MITE Circuit Stages

Consider the three basic MITE circuit stages that are depicted in Fig. 12. The first of these circuits is a *voltage-in, current-out* (VICO) stage, shown in Fig. 12a. Here, we apply input voltages, V_i and V_k, to two different input terminals of MITE Q_n, which, in response, generates an output current, I_n. To see how I_n depends on V_i and V_k, using Eq. 21, we write

$$I_n \propto e^{(w_{ni}V_i + w_{nk}V_k + \cdots)/U_T}.$$

By breaking out the first two terms of the weighted summation and using the fact that $e^{x+y} = e^x e^y$, we can rewrite the preceding expression as

$$I_n \propto e^{w_{ni}V_i/U_T} e^{w_{nk}V_k/U_T}. \tag{22}$$

The second of the three basic MITE stages, shown in Fig. 12b, is a *current-in, voltage-out* (CIVO) stage. Here, we source an input current, I_i, into the output of MITE Q_i, and we feed the output voltage, V_i, back through the self-coupling weight, w_{ii}. This feedback configuration adjusts V_i, so that the current sunk by MITE Q_i just balances the input current, I_i. A MITE in this feedback configuration is analogous to a diode-connected transistor, so we say that it is *diode connected through* w_{ii}. To determine how the output voltage, V_i, depends on the input current, I_i, we begin with Eq. 21, and solve for V_i in terms of I_i. So, we write

$$I_i \propto e^{(w_{ii}V_i+\cdots)/U_\mathrm{T}},$$

which we rearrange to find that

$$V_i = \frac{U_\mathrm{T}}{w_{ii}} \log I_i - \cdots. \tag{23}$$

The third basic MITE stage is a *voltage-in, voltage-out* (VIVO) stage, shown in Fig. 12c. This configuration is identical to the CIVO stage of Fig. 12b, except that we now hold the current, I_i, fixed, and we are instead concerned with how the output voltage, V_i, depends on an input voltage, V_j, which we apply to another of the input terminals of MITE Q_i. Beginning with Eq. 21, we write that

$$I_i \propto e^{(w_{ii}V_i+w_{ij}V_j+\cdots)/U_\mathrm{T}},$$

which we rearrange to solve for V_i in terms of V_j, as follows:

$$V_i = -\frac{w_{ij}}{w_{ii}} V_j - \cdots. \tag{24}$$

We can use the circuit stage of Fig. 12c both as a CIVO stage and as a VIVO stage simultaneously. In this case, it is easy to see that V_i depends on V_j and I_i through a linear combination of of Eqs. 23 and 24 as follows:

$$V_i = \frac{U_\mathrm{T}}{w_{ii}} \log I_i - \frac{w_{ij}}{w_{ii}} V_j - \cdots. \tag{25}$$

7.2 Elementary MITE Networks

In this section, we shall examine two simple current-mode MITE circuits, each comprising two CIVO stages and a single VICO stage. These two basic current-mode circuits illustrate all of the basic intuition behind the operation of MITE networks.

In the first current-mode circuit, shown in Fig. 13a, we connect the outputs of two different CIVO stages directly to a single VICO stage through separate inputs. To analyze this circuit, we apply Eq. 22 to the output stage, obtaining

$$I_n \propto e^{w_{ni}V_i/U_\mathrm{T}} e^{w_{nk}V_k/U_\mathrm{T}}. \tag{26}$$

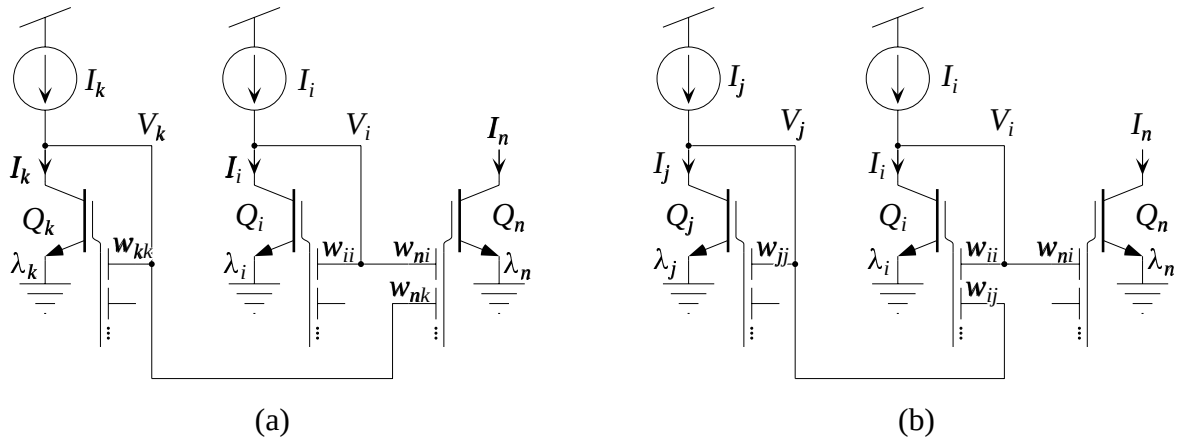


Figure 13: Two basic current-mode circuits comprising two CICO stages and one VICO stage. These two circuits illustrate all of the intuition underlying the class of MITE networks (a) A product-of-power-law circuit. (b) A quotient-of-power-law circuit.

Substituting Eq. 23 into Eq. 26 for each of V_i and V_k, we obtain

$$I_n \propto \exp\left[\frac{w_{ni}}{U_\mathrm{T}}\left(\frac{U_\mathrm{T}}{w_{ii}}\log I_i - \cdots\right)\right]\exp\left[\frac{w_{nk}}{U_\mathrm{T}}\left(\frac{U_\mathrm{T}}{w_{kk}}\log I_k - \cdots\right)\right].$$

When we break out the first term in each of the two summations and regroup, this expression becomes

$$I_n \propto \exp\left[\frac{U_\mathrm{T}}{U_\mathrm{T}}\frac{w_{ni}}{w_{ii}}\log I_i\right]\exp\left[\frac{U_\mathrm{T}}{U_\mathrm{T}}\frac{w_{nk}}{w_{kk}}\log I_k\right]. \tag{27}$$

Note that, if MITEs Q_i, Q_k, and Q_n are operating at the same temperature, then the primary temperature dependence of the relationship among I_i, I_k, and I_n disappears from Eq. 27. In this intuitive analysis, we have not kept track of the scaling currents, I_s, which can be strongly temperature dependent, but, as we have demonstrated previously [84], if the products of the input currents raised to their respective powers has units of Amperes (i.e., as opposed to Amperes raised to some other power than unity), then the relationship between the output current and the input currents is generally insensitive to isothermal variations. Now, because $x\log y = \log y^x$ and $e^{\log x} = x$, we can rewrite Eq. 27 as

$$I_n \propto I_i^{w_{ni}/w_{ii}} \times I_k^{w_{nk}/w_{kk}}. \tag{28}$$

Thus, the output current is proportional to the product of the two input currents, each of which is raised to a power that is set by a ratio of MITE weights.

For the second basic current-mode MITE circuit, instead of connecting the output of the second CIVO stage directly to a second input of the output VICO stage, as we do in the circuit of Fig. 13a, we connect the output of the second CIVO stage to the output stage through the first CIVO stage,

as shown in Fig. 13b. This first CIVO stage both generates a voltage that is logarithmic in the input current, I_i, and serves as a VIVO stage for the second CIVO stage. This connection allows us to obtain negative powers. To show that it will, we apply Eq. 21 to the output stage, obtaining

$$I_n \propto e^{(w_{ni} V_i + \cdots)/U_T}. \tag{29}$$

Substituting Eq. 25 into Eq. 29, we get

$$I_n \propto \exp\left[\frac{w_{ni}}{U_T}\left(\frac{U_T}{w_{ii}}\log I_i - \frac{w_{ij}}{w_{ii}}V_j - \cdots\right)\right],$$

into which we substitute Eq. 23 for V_j, and thus obtain

$$I_n \propto \exp\left[\frac{w_{ni}}{U_T}\left(\frac{U_T}{w_{ii}}\log I_i - \frac{w_{ij}}{w_{ii}}\left(\frac{U_T}{w_{ii}}\log I_i - \cdots\right)\right)\right].$$

Now, if we break out the first two terms of the summation and regroup, we find that

$$I_n \propto \exp\left[\frac{U_T}{U_T}\frac{w_{ni}}{w_{ii}}\log I_i\right]\exp\left[-\frac{U_T}{U_T}\frac{w_{ni}}{w_{ii}}\frac{w_{ij}}{w_{jj}}\log I_j\right]. \tag{30}$$

Again, because $x \log y = \log y^x$ and $e^{\log x} = x$, we can rewrite Eq. 30 as

$$I_n \propto I_i^{w_{ni}/w_{ii}} \times I_j^{-(w_{ni}/w_{ii})(w_{ij}/w_{jj})},$$

which, in turn, becomes

$$I_n \propto \frac{I_i^{w_{ni}/w_{ii}}}{I_j^{(w_{ni}/w_{ii})(w_{ij}/w_{jj})}}. \tag{31}$$

Thus, the output current is proportional to the quotient of the two input currents, each of which is raised to a power that is set by ratios of MITE weights. Here, the powers are not completely independent of each other—however, for any value of w_{ni}/w_{ii}, we can adjust the value of w_{ij}/w_{jj} to set the power of I_j to whatever we want. This quotient-of-power-law relationship is also insensitive to isothermal variations.

These two basic current-mode MITE circuits capture all of the intuition underlying MITE-network operation. We generate voltages that are logarithmic in the input currents using diode-connected MITEs. We set power laws through ratios of MITE weights. We obtain negative powers by using voltage-inversion stages. We get products by summing two or more logarithmic voltages on MITEs. We have formalized this intuitive analysis and have obtained systematic analysis and synthesis procedures for this class of nonlinear circuits [84, 86].

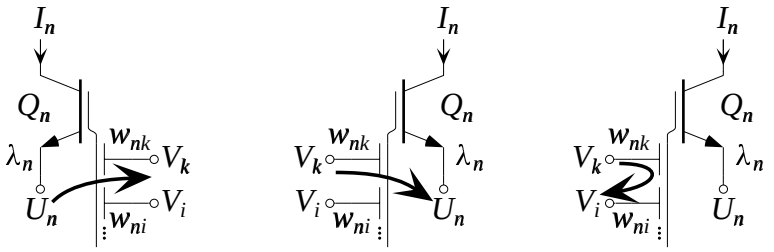


Figure 14: The three types of moves that we can encounter in traversing a loop within a MITE network. We can go (a) from an emitter to a control gate, (b) from a control gate to an emitter, or (c) from a control gate to another control gate.

8 Analysis of MITE Networks

In this section, we shall develop a by-inspection analysis procedure for MITE networks by extending the analysis procedure for translinear loops of subthreshold MOS transistors that we discussed in Section 4.2. We have previously published analysis procedures for MITE networks [84, 87]. The analysis method that we develop here is somewhat more general and requires fewer initial definitions. Additionally, we can use this procedure directly to analyze subthreshold MOS translinear circuits that make use of the back gate (i.e., the substrate) in addition to the front gate [81, 88–91]. To do so, we simply view the four-terminal subthreshold MOS transistor as a two-input MITE with a weight of κ for the front gate and of $1-\kappa$ for the back gate and apply the procedure that we shall develop.

As we go around loops in a MITE network, we can traverse a MITE in three possible ways, which are depicted in Fig. 14. As shown in Fig. 14a, we can traverse MITE Q_n, by going from its emitter, U_n, to one of its control gates, V_k; this possibility corresponds to going through a counterclockwise element in a translinear-loop circuit. In this case, we can rearrange Eq. 21 to obtain the following recursion relation:

$$e^{V_k/U_T} = \left(e^{U_n/U_T}\right)^{1/w_{nk}} \left(\frac{I_n}{\lambda_n I_s}\right)^{1/w_{nk}} \prod_{j \neq k} \left(e^{V_j/U_T}\right)^{-w_{nj}/w_{nk}} . \tag{32}$$

Conversely, as shown in Fig. 14b, we can traverse MITE Q_n by going from one of its control gates, V_k, to its emitter, U_n; this transition corresponds to going through a clockwise element in a conventional translinear-loop circuit. In this case, we can rearrange Eq. 21 to obtain the following recursion relation:

$$e^{U_n/U_T} = \left(e^{V_k/U_T}\right)^{w_{nk}} \left(\frac{\lambda_n I_s}{I_n}\right) \prod_{j \neq k} \left(e^{V_j/U_T}\right)^{w_{nj}} . \tag{33}$$

Finally, as shown in Fig. 14c, we can traverse MITE Q_n by going one of its control gates, V_k to another of its control gates, V_i; this transition has no analog in conventional translinear-loop

circuits. In this case, we can rearrange Eq. 21 to obtain another recursion relationship:

$$e^{V_i/U_T} = \left(e^{V_k/U_T}\right)^{-w_{nk}/w_{ni}} \left(\frac{I_n}{\lambda_n I_s}\right)^{1/w_{ni}} \left(e^{U_n/U_T}\right)^{1/w_{ni}} \prod_{j \neq i,k} \left(e^{V_j/U_T}\right)^{-w_{nj}/w_{ni}} \tag{34}$$

The final product in each of these three recursion relationships accounts for the contributions of peripheral control gates, which do not lie directly on the particular path through the MITE network that we have chosen. Multiple translinear loops can flow together through these extra control gates, like tributaries joining to form a river. Translinear loops can split into multiple paths and merge back together again. We shall call such translinear loops *confluent*. The existence of confluent translinear loops makes the analysis of MITE networks slightly more involved than conventional translinear-loop circuits, because we may have to traverse several confluent translinear loops to analyze a given circuit completely. To analyze a MITE network, we first identify a loop through the circuit that traverses most of the MITEs. We proceed around the loop from node to node, building up a translinear-loop expression as we go by applying the recursion relationship appropriate to each transition. If there is a confluence of translinear loops, we trace through each one until we have built a complete translinear-loop expression.

We shall now illustrate this analysis procedure by applying it to several simple MITE networks. Consider the MITE network shown in Fig. 15a, which comprises three two-input MITEs. Note that all of the MITE emitters are grounded in this circuit. In this case, all of the e^{U_n/U_T} factors in the recursion relationships evaluate to unity; consequently, we can ignore them in applying the recursion relationships. Moreover, we shall show by construction in Section 9 that any translinear-loop equation can be realized by a MITE network with grounded emitters. However, in some cases, it may prove beneficial to have some MITE emitters at some potential other than ground. In such cases, we would have to keep track of the emitter factors. To analyze the circuit of Fig. 15a, we first identify a loop through the circuit that traverses as many of the MITEs as possible. We begin at the emitter of MITE Q_1, which is grounded, and proceed to node V_1 through MITE Q_1. Then, we move to node V_2 through MITE Q_3. Finally, we return to ground by moving to the emitter of MITE Q_2. This single loop traverses each MITE in the circuit; there are no confluent loops. By following the procedure just described, we have that

$$\underbrace{\left(\underbrace{(1)^{1/2}\left(\frac{I_1}{\lambda_1 I_s}\right)^{1/2}}_{e^{V_1/U_T}}\right)^{-1/1}\left(\frac{I_3}{\lambda_3 I_s}\right)^{1/1}}_{e^{V_2/U_T}}\Bigg)^{2}\left(\frac{\lambda_2 I_s}{I_2}\right) = 1,$$

which we can simplify to get

$$\left(\frac{\lambda_1}{I_1}\right)\left(\frac{I_3}{\lambda_3}\right)^2\left(\frac{\lambda_2}{I_2}\right) = 1.$$

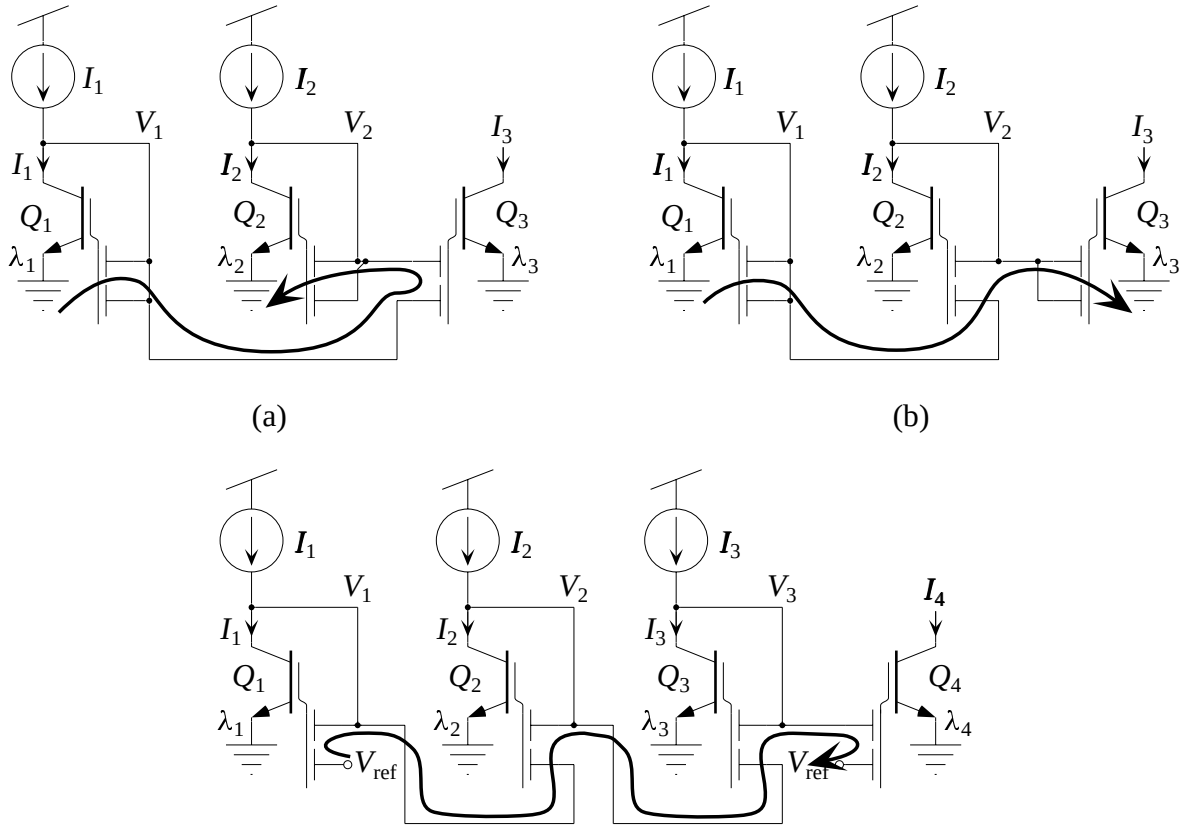


Figure 15: Three MITE networks comprising two-input MITEs that can be analyzed completely by tracing a single loop. (a) A two-input geometric-mean circuit. (b) A squaring-reciprocal circuit. (c) A multiply-reciprocal circuit.

By rearranging the preceding equation, we obtain the following translinear-loop expression:

$$\left(\frac{I_3}{\lambda_3}\right)^2 = \left(\frac{I_1}{\lambda_1}\right)\left(\frac{I_2}{\lambda_2}\right),$$

which we can solve for the output current, I_3, to get

$$I_3 = \frac{\lambda_3}{\sqrt{\lambda_1\lambda_2}}\sqrt{I_1 I_2}.$$

Thus, the circuit of Fig. 15a is a two-input geometric-mean circuit. If each MITE has the same value of λ (i.e., $\lambda_1 = \lambda_2 = \lambda_3 = \lambda$), then the output current is simply given by

$$I_3 = \sqrt{I_1 I_2}.$$

Next, consider the MITE network shown in Fig. 15b, which also comprises three two-input MITEs. To analyze this circuit, we first identify a loop through the circuit that traverses as many of the MITEs as possible. We begin at the emitter of MITE Q_1, which is grounded, and proceed to node V_1 through MITE Q_1. Then, we move to node V_2 through MITE Q_2. Finally, we return to ground by moving to the emitter of MITE Q_3. This single loop traverses each MITE in the circuit; once again, there are no confluent loops for us to trace. If we go around this loop, applying the recursion relationship appropriate to each move, we find that

$$\underbrace{\left(\underbrace{(1)^{1/2}\left(\frac{I_1}{\lambda_1 I_s}\right)^{1/2}}_{e^{V_1/U_T}}\right)^{-1/1}\left(\frac{I_2}{\lambda_2 I_s}\right)^{1/1}}_{e^{V_2/U_T}}\Bigg)^2\left(\frac{\lambda_3 I_s}{I_3}\right)=1,$$

which can simplify to get

$$\left(\frac{\lambda_1}{I_1}\right)\left(\frac{I_2}{\lambda_2}\right)^2\left(\frac{\lambda_3}{I_3}\right)=1.$$

By rearranging the preceding expression, we obtain the following translinear-loop equation:

$$\left(\frac{I_2}{\lambda_2}\right)^2=\left(\frac{I_1}{\lambda_1}\right)\left(\frac{I_3}{\lambda_3}\right), \tag{35}$$

which, apart from a simple renumbering of the currents, is identical to that which we derived for the circuit of Fig. 15a. This result should not be too surprising, because the two MITE networks shown in Fig. 15 have the same basic topology; they are merely biased differently. We can rearrange Eq. 35 to obtain the following expression for the output current:

$$I_3=\frac{\lambda_1\lambda_3}{\lambda_2^2}\frac{I_2^2}{I_1}.$$

Thus, the circuit of Fig. 15b is a squaring-reciprocal circuit. Again, if each MITE has the same value of λ (i.e., $\lambda_1=\lambda_2=\lambda_3=\lambda$), then the output current is simply given by

$$I_3=\frac{I_2^2}{I_1}.$$

Next, consider the MITE network shown in Fig. 15c, which comprises four two-input MITEs. To analyze this circuit, we first identify a loop through the circuit that traverses as many of the MITEs as possible. We begin at one of the control gates of MITE Q_1, which is connected to V_{ref}, and proceed to node V_1 through MITE Q_1. Then, we move to node V_2 through MITE Q_2. Then, we move to V_3 through MITE Q_3. Finally, we return to V_{ref} through MITE Q_4. This single loop

traverses each MITE in the circuit; once again, there are no confluent loops for us to trace. If we go around this loop, applying the recursion relationship appropriate to each move, we find that

$$\underbrace{\left(\underbrace{\left(\underbrace{\left(e^{V_{\text{ref}}/U_{\text{T}}}\right)^{-\frac{1}{1}}\left(\frac{I_1}{\lambda_1 I_{\text{s}}}\right)^{\frac{1}{1}}}_{e^{V_1/U_{\text{T}}}}\right)^{-\frac{1}{1}}\left(\frac{I_2}{\lambda_2 I_{\text{s}}}\right)^{\frac{1}{1}}}_{e^{V_2/U_{\text{T}}}}\right)^{-\frac{1}{1}}\left(\frac{I_3}{\lambda_3 I_{\text{s}}}\right)^{\frac{1}{1}}}_{e^{V_3/U_{\text{T}}}}\right)^{-\frac{1}{1}}\left(\frac{I_4}{\lambda_4 I_{\text{s}}}\right)^{\frac{1}{1}} = e^{V_{\text{ref}}/U_{\text{T}}},$$

which can simplify to get

$$\left(e^{V_{\text{ref}}/U_{\text{T}}}\right)\left(\frac{\lambda_1}{I_1}\right)\left(\frac{I_2}{\lambda_2}\right)\left(\frac{\lambda_3}{I_3}\right)\left(\frac{I_4}{\lambda_4}\right) = e^{V_{\text{ref}}/U_{\text{T}}}.$$

By rearranging the preceding expression, we obtain the following translinear-loop equation:

$$\left(\frac{I_1}{\lambda_1}\right)\left(\frac{I_3}{\lambda_3}\right) = \left(\frac{I_2}{\lambda_2}\right)\left(\frac{I_4}{\lambda_4}\right). \tag{36}$$

We can rearrange Eq. 36 to obtain the following expression for the output current:

$$I_4 = \frac{\lambda_2\lambda_4}{\lambda_1\lambda_3}\frac{I_1 I_3}{I_2}.$$

Thus, the circuit of Fig. 15c is a multiply-reciprocal circuit. Again, if each MITE has the same value of λ (i.e., $\lambda_1 = \lambda_2 = \lambda_3 = \lambda_4 = \lambda$), then the output current is simply given by

$$I_4 = \frac{I_1 I_3}{I_2}.$$

For each of the MITE networks that we have analyzed so far, we only had to trace a single loop around the network to fully characterize the circuit. We shall now consider a simple example where we must trace at least two confluent translinear loops to fully analyze the circuit. Figure 16 shows a MITE network comprising four two-input MITEs. We cannot identify a single loop through this circuit that traverses each MITE—we must consider at least two loops that are confluent with one another. To analyze this circuit, we first identify a loop through the circuit that traverses as many of the MITEs as possible. As shown in Fig. 16a, we begin at the emitter of MITE Q_1, which is grounded, and proceed to node V_1 through MITE Q_1. Then, we move to node V_3 through MITE Q_3. Then, we return to ground through MITE Q_4. We have not traversed MITE Q_2 at all in this loop. If we go around this loop, applying the recursion relationship appropriate to each move, we find that

$$\underbrace{\left(\underbrace{\left(\underbrace{(1)^{1/2}\left(\frac{I_1}{\lambda_1 I_{\text{s}}}\right)^{1/2}}_{e^{V_1/U_{\text{T}}}}\right)^{-1/1}\left(\frac{I_3}{\lambda_3 I_{\text{s}}}\right)^{1/1}}_{e^{V_3/U_{\text{T}}}}\right)^{1}\left(\frac{\lambda_4 I_{\text{s}}}{I_4}\right)\left(e^{V_2/U_{\text{T}}}\right)^{1} = 1, \tag{37}$$

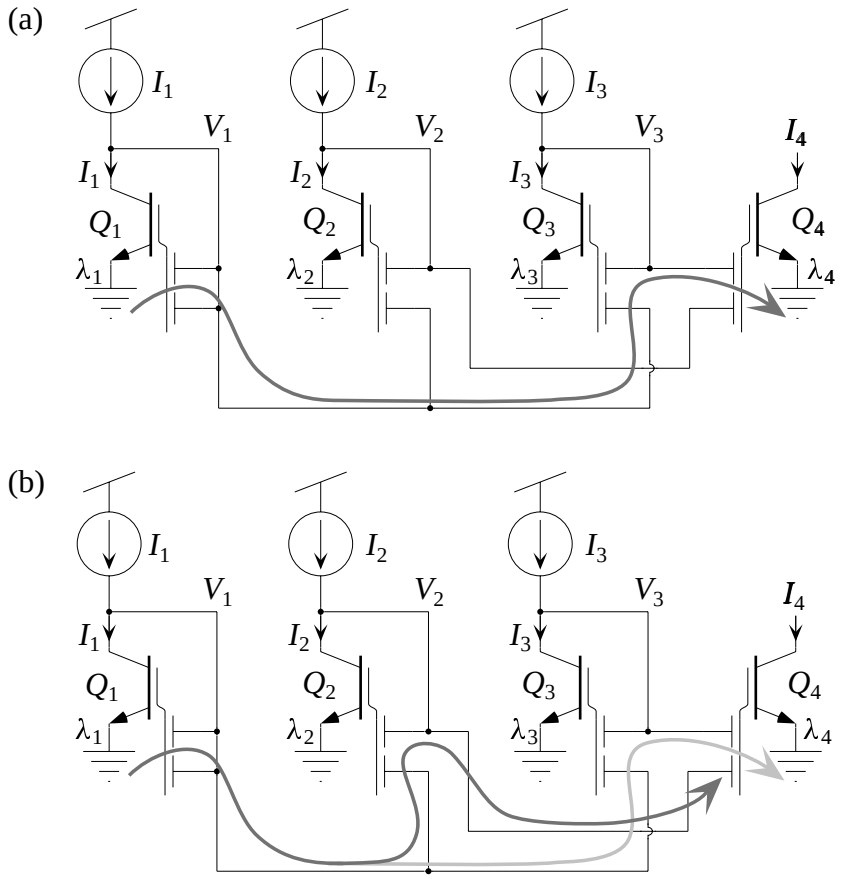


Figure 16: A MITE network comprising four two-input MITEs. To analyze this circuit, we must consider consider at least two loops that are confluent with one another. (a) The primary loop that we use to analyze the circuit. (b) The confluent loop that we trace to complete the analysis.

which has a factor of e^{V_2/U_T}, that we would like to express in terms of the MITE collector currents. We can derive a suitable expression for e^{V_2/U_T} by traversing the confluent loop shown in Fig. 16b. If we go around this second loop, applying the recursion relationship appropriate to each move and substitute the resulting expression for e^{V_2/U_T} directly into Eq. 37, we find that

$$\underbrace{\left(\underbrace{\left(1^{\frac{1}{2}}\left(\frac{I_1}{\lambda_1 I_s}\right)^{\frac{1}{2}}\right)}_{e^{V_1/U_T}}{}^{-\frac{1}{1}}\left(\frac{I_3}{\lambda_3 I_s}\right)^{\frac{1}{1}}\right)}_{e^{V_3/U_T}}{}^{1}\left(\frac{\lambda_4 I_s}{I_4}\right)\underbrace{\left(\left(\underbrace{1^{\frac{1}{2}}\left(\frac{I_1}{\lambda_1 I_s}\right)^{\frac{1}{2}}}_{e^{V_1/U_T}}\right)^{-\frac{1}{1}}\left(\frac{I_2}{\lambda_2 I_s}\right)^{\frac{1}{1}}\right)}_{e^{V_2/U_T}}{}^{1} = 1.$$

By simplifying the preceding equation, we have that

$$\left(\frac{\lambda_1}{I_1}\right)^{1/2}\left(\frac{I_3}{\lambda_3}\right)\left(\frac{\lambda_4}{I_4}\right)\left(\frac{\lambda_1}{I_1}\right)^{1/2}\left(\frac{I_2}{\lambda_2}\right)=1,$$

which we can rearrange to obtain the following translinear-loop equation:

$$\left(\frac{I_3}{\lambda_3}\right)\left(\frac{I_2}{\lambda_2}\right)=\left(\frac{I_1}{\lambda_1}\right)\left(\frac{I_4}{\lambda_4}\right). \tag{38}$$

We can rearrange Eq. 38 to obtain the following expression for the output current:

$$I_4=\frac{\lambda_4\lambda_1}{\lambda_2\lambda_3}\frac{I_2I_3}{I_1}.$$

Thus, the circuit of Fig. 16 is also a multiply-reciprocal circuit. Again, if each MITE has the same value of λ (i.e., $\lambda_1=\lambda_2=\lambda_3=\lambda_4=\lambda$), then the output current is simply given by

$$I_4=\frac{I_2I_3}{I_1}.$$

9 ABC's of MITE-Network Synthesis

In this section, we shall consider the basics of MITE-network synthesis. As was the case with translinear-loop circuit synthesis, the problem of synthesizing MITE networks is underconstrained and there are design trade-offs involved in the process. Once again, in our brief discussion, we cannot be exhaustive and we shall endeavor to make the basic procedure clear illustrate it with some simple examples. The starting point for MITE-network synthesis is identical to that of translinear-loop circuit synthesis—a set of translinear-loop equations derived from some functional or behavioral description of the system to be implemented. Also, we can often consolidate MITE networks in the same way that we can translinear-loop circuits, by merging redundant parts of the circuits that we have synthesized, so the final steps are similar too. Consequently, we shall focus on the middle steps in the synthesis procedure—the construction of MITE networks from translinear-loop equations.

9.1 Synthesizing Static MITE Networks

As with the synthesis of translinear-loop circuits, we can summarize the synthesis of MITE networks as follows. First, we *acquire* a set of translinear-loop equations from a behavioral or functional description of the system that we want to implement. Next, we *build* a MITE network for each of the translinear-loop equations, which involves a *building* phase, a *balancing* phase, a *biasing* phase, and a *completion* phase. Finally, if possible, we *consolidate* the resulting MITE networks by merging parts of them where possible. We shall discuss each of these steps in turn, then we shall use them to synthesize three simple MITE networks, a squaring circuit, one-quadrant multipliers, and a two-quadrant multiplier.

Acquiring a set of translinear-loop equations. We start the construction process with a set of translinear-loop equations, each of the form

$$\prod_{n\in\text{“CW”}} I_n^{k_n} = \prod_{n\in\text{“CCW”}} I_n^{k_n}, \tag{39}$$

where “CW” denotes a set of clockwise currents and “CCW” denotes a set of counterclockwise currents (in the context of MITE networks, such designations are not as meaningful as they are in translinear-loop circuits), and the k_n are positive integer powers to which the currents are raised, such that

$$\sum_{n\in\text{“CW”}} k_n = \sum_{n\in\text{“CCW”}} k_n. \tag{40}$$

With translinear-loop circuits, the reason for restricting the powers to be integers is obvious: A current is raised to a given power because it passes through an integer number of TEs facing in the same direction around a loop. A current cannot pass through a fractional number of TEs. However, with MITE networks, it is certainly possible to allow these powers to be positive real numbers subject to the constraint expressed in Eq. 40, but we shall restrict our attention here to the case of integer powers for two reasons. First, integer powers suffice for many practical purposes. Second, with MITE networks these powers are set by ratios of MITE weights and we obtain the most accurate ratios by connecting an integer number of identical unit cells in parallel with one another. The procedure by which we obtain such translinear-loop equations is identical to the one that we described in Section 5.

Building MITE networks. For each translinear-loop equation, we build a MITE network. We begin a MITE network by picking a current from each set (e.g., current I_i from the “clockwise” set and current I_j from the “counterclockwise” set). We create a new MITE for each one and make a new node in the circuit, coupling it into MITE Q_i through k_j unit inputs and into MITE Q_j through k_i unit inputs, as shown in Fig. 17a. If k_i and k_j have a factor in common, we can divide both by that factor in determining the number of unit inputs for each connection. For each additional current in the translinear-loop equation (e.g., current I_k from the “clockwise” set), we create a new MITE, and we make a new node in the circuit, connecting it to an existing MITE whose current is from the *opposite* set (e.g., MITE Q_j) through k_k unit inputs and to MITE Q_k through k_j unit inputs, as shown in Fig. 17b. Once again, if k_j and k_k have a factor in common, we can divide both by that factor in determining the number of unit inputs for each connection. We continue adding MITEs in this way until we have exhausted all of the currents in the translinear-loop equation. The order in which we add MITEs and the existing MITEs to which we connect them affect the structure of the final MITE network and the number of inputs required fan-in for each MITE.

Once we have built the basic MITE network for a translinear-loop equation, as just described, we then balance the fan-in of all MITEs in the network. Suppose that the largest MITE fan-in is K. We then add a sufficient number of unit inputs to each MITE, connected to an appropriate voltage V_{ref}, so they each have a fan-in of K, as shown in Fig. 17c. As long as the translinear-loop equation from which we started conforms to Eq. 40, the exact value of V_{ref} is not critical—the

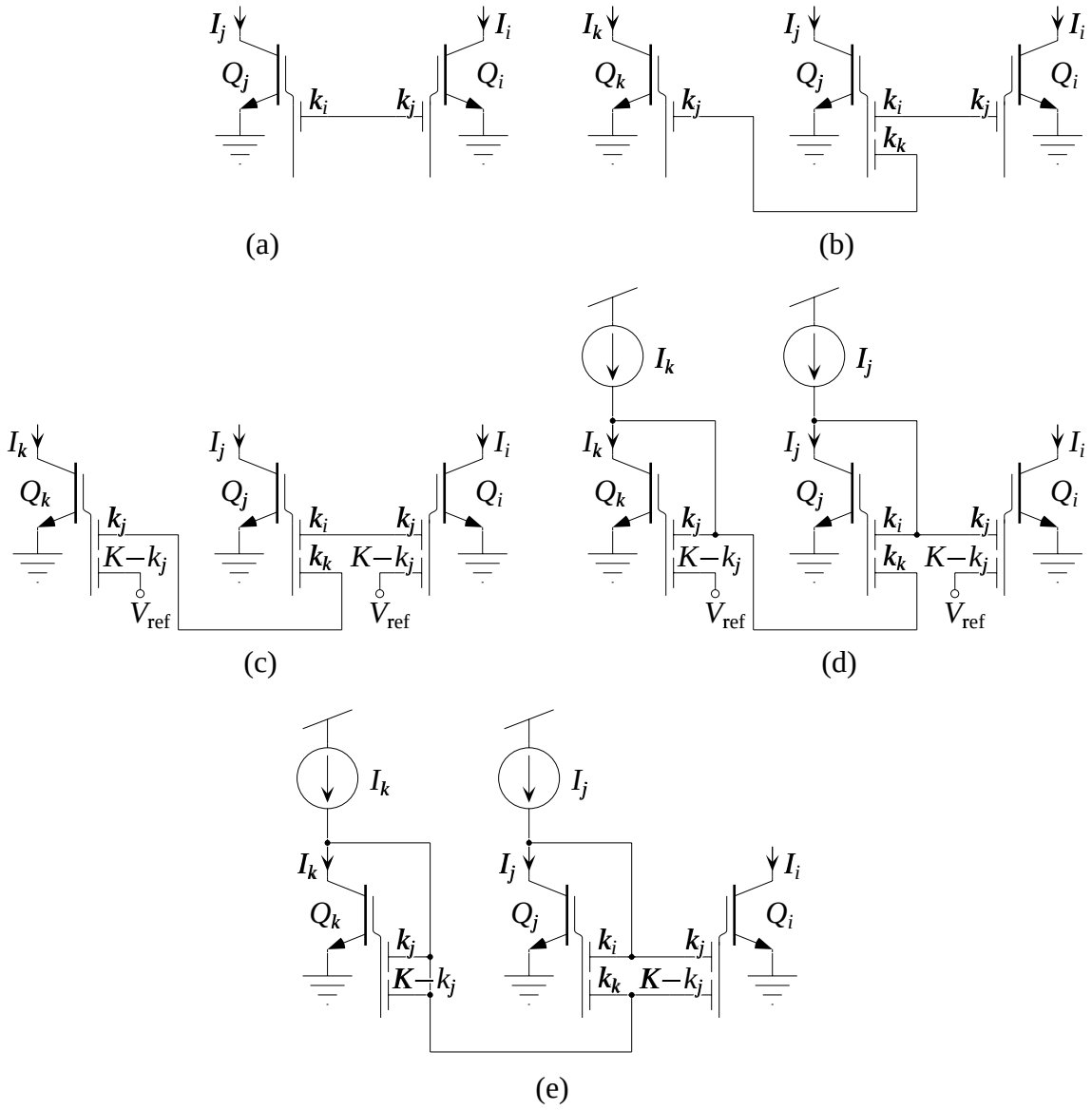


Figure 17: Steps in the construction of MITE networks. (a) Beginning the network. (b) Building the network. (c) Balancing the network. (d) Biasing the network. (e) Completing the network.

quiescent collector voltages in the MITE network will depend on the value of V_{ref}, but as long as all of the collector voltages stay sufficiently far away from the power supply rails, the MITE network's behavior is independent of the value of V_{ref}.

We need to balance the number of inputs to each MITE in the network because of the way in which we implement the weighted voltage summation. If we implement the weighted voltage

summation using a capacitive voltage divider, as discussed in Section 6, then each weight is equal to a coupling capacitance divided by a total floating-gate capacitance. The power-law relationships implemented by a MITE network are given by ratios of weights. As designers, we would like these powers to be independent of the total floating-gate capacitances, because they include (nonlinear) parasitic capacitances. By requiring the total floating-gate capacitance of each MITE to be the same, the total floating-gate capacitances will cancel in the weight ratios, making them depend only on ratios of coupling capacitors. The best way to ensure that the total floating-gate capacitances are the same is to require that each MITE have an identical complement of inputs. In the context of integer numbers of unit inputs, we would give each MITE the same number of unit inputs.

Biasing MITE networks. The process of biasing a MITE network is considerably simpler than that of biasing a translinear-loop circuit. We simply force input currents into the collectors of some of the MITEs and diode-connect them by connecting some of their control gates to their collectors, as shown in Fig. 17d. Those MITEs that are diode connected become inputs, while those that are not diode connected are outputs. Other biasing schemes are certainly possible, but are never needed.

Completing MITE networks. It may seem that by adding unused MITEs in the process of balancing the fan-in in a MITE network, we are wasting resources. Indeed, such unused inputs can account for a significant fraction of the total transconductance of a MITE. Leaving them unused leads to larger collector-voltage swings and a higher required power-supply voltage. It so happens that, as long as the translinear-loop equation from which we started conforms to Eq. 40, we can utilize all of the extra control gates that we add during the balancing phase [84]. Intuitively, because the behavior of a MITE network is unaffected by the value of V_{ref}, we can short V_{ref} to one of the collector voltages in the MITE network without affecting the behavior of the circuit. This MITE-network transformation is called *completion* [84]. We connect all of the unused inputs to one of the collector voltages, as shown in Fig. 17e. In doing so, we should generally avoid the creation of feedback loops in the MITE network that could affect its stability. We can always do this by choosing a MITE that only has self connections.

Consolidating MITE networks. In some cases, as with translinear-loop circuits, after we have biased each of the MITE networks in the circuit, we will recognize some redundancy between them. For example, if two MITEs in different networks pass the same current and their control gates are connected in the same manner, then these MITEs are redundant and may be shared between the MITE networks. Such consolidation is usually a good idea, because it usually results in smaller circuits and fewer opportunities for errors resulting from device mismatch. Other, more subtle forms of MITE-network consolidation are possible [92], but are beyond the scope of this report.

9.2 Synthesis of a MITE-Network Squaring Circuit

Suppose that we want to implement a squaring operation with a strictly positive input using a MITE network. That is, we want to find a MITE network that implements the relationship

$$x = y^2, \tag{41}$$

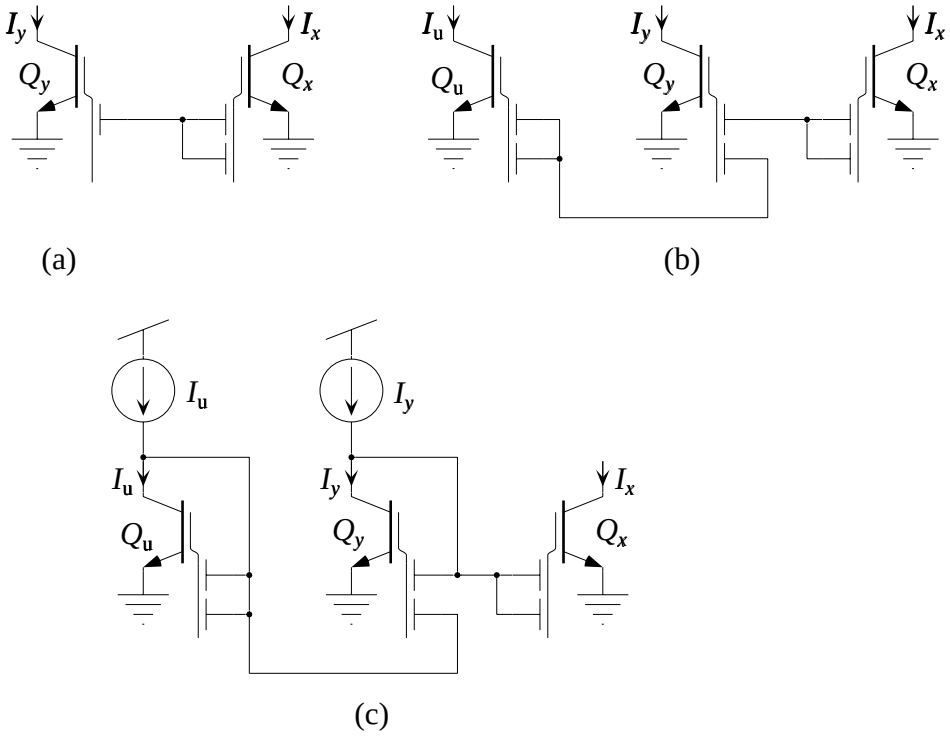


Figure 18: Synthesis of a MITE-network squaring circuit. (a) Beginning the network. (b) Building the network. (c) Biasing the network.

where $x > 0$ and $y > 0$ are dimensionless quantities. Here y is the independent variable (i.e., the input) and x is the dependent variable (i.e., the output). First, we represent x by I_x/I_u and y by I_y/I_u, where I_u is the unit current. Then, we substitute these definitions of x and y into Eq. 41, getting

$$\frac{I_x}{I_u} = \left(\frac{I_y}{I_u}\right)^2,$$

which we can easily rearrange to obtain the following translinear-loop equation:

$$\underbrace{I_x I_u}_{\text{“CW”}} = \underbrace{I_y^2}_{\text{“CCW”}}. \tag{42}$$

Starting from Eq. 42, we select I_y from the “CCW” set and I_x from the “CW” set and make a MITE for each one. Then, we make a new node in the circuit and couple it into MITE Q_x through two unit inputs and into MITE Q_y through one unit input, as shown in Fig. 18a. Next, we select I_u from the “CW” set and make another MITE for it. We make a new node and couple it into MITE Q_y, which is our only choice in this case, through one unit input and into MITE Q_u through two unit inputs, as shown in Fig. 18b. Next, we balance the fan-in of all MITEs. In this case, each

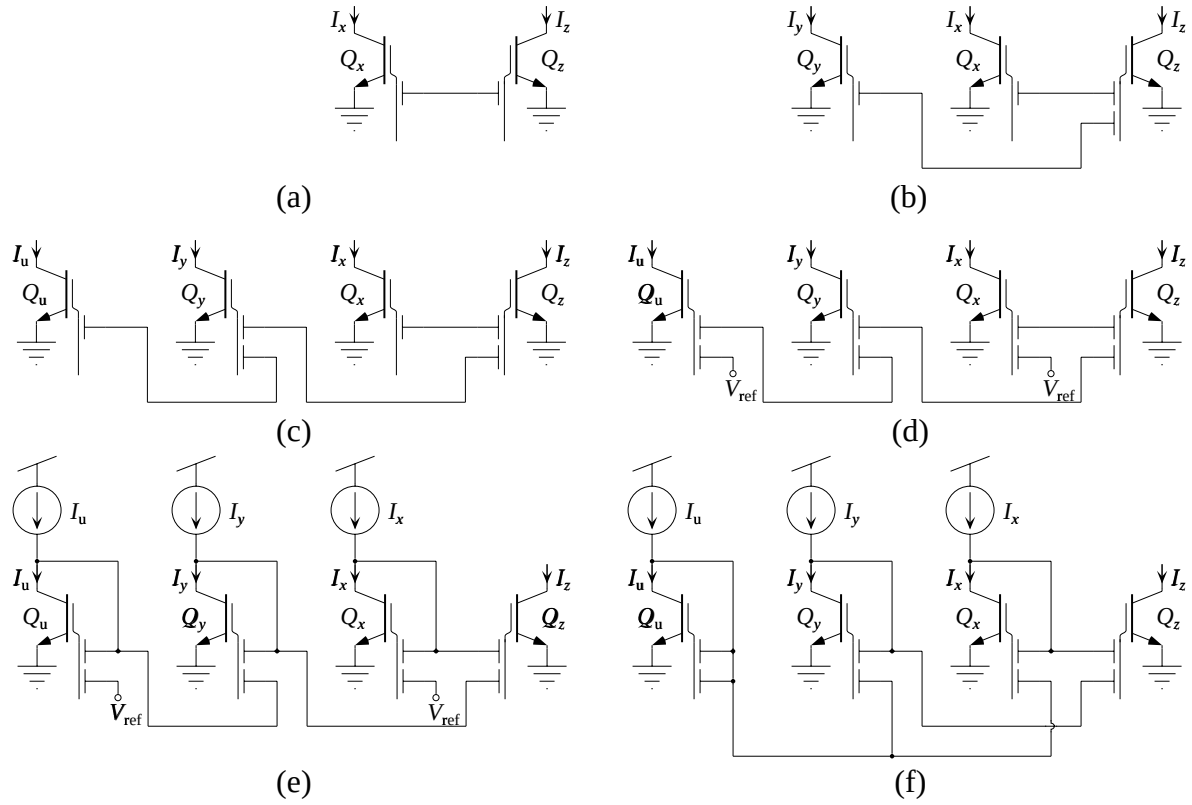


Figure 19: Synthesis of a one-quadrant MITE-network multiplier. (a) Beginning the network. (b) Building the network. (c) Building the network. (d) Balancing the network. (e) Biasing the network. (f) Completing the network.

MITE has the same number of inputs, so the network is already balanced. We bias the network by forcing I_{u} into MITE Q_{u} and diode connecting it through its two unit inputs. Then, we force I_y into MITE Q_y and diode connect it through one of its control gates, as shown in Fig. 18c. There are no unused inputs, so the MITE network requires no completion. Finally, no consolidation is possible.

9.3 Synthesis of One-Quadrant MITE-Network Multipliers

Suppose that we want to implement a multiplication operation with strictly positive inputs using a MITE network. That is, we want to find a MITE network that implements the relationship

$$z = xy, \tag{43}$$

where $x > 0$, $y > 0$, and $z > 0$ are dimensionless quantities. Here x and y are the independent variables (i.e., the inputs) and z is the dependent variable (i.e., the output). First, we represent x by

I_x/I_u, y by I_y/I_u and z by I_z/I_u, where I_u is the unit current. Then, we substitute these definitions of x, y, and z into Eq. 43, getting

$$\frac{I_z}{I_u} = \frac{I_x}{I_u}\frac{I_y}{I_u},$$

which we can easily rearrange to obtain the following translinear-loop equation:

$$\underbrace{I_z I_u}_{\text{“CW”}} = \underbrace{I_x I_y}_{\text{“CCW”}}. \tag{44}$$

Starting from Eq. 44, we shall synthesize two different MITE networks to illustrate how the building order can influence the structure of the final MITE network. We begin the first MITE network by selecting I_z from the “CW” set and I_x from the “CCW” set and make a MITE for each one. Then, we make a new node in the circuit and couple it into MITE Q_z through one unit input and into MITE Q_x through one unit input, as shown in Fig. 19a. Next, we select I_y from the “CW” set and make another MITE for it. We make a new node and couple it into MITE Q_z through one unit input and into MITE Q_y through one unit input, as shown in Fig. 19b. Next, we select I_u from the “CCW” set and make another MITE for it. We make a new node and couple it into MITE Q_y through one unit input and into MITE Q_u through one unit input, as shown in Fig. 19c. Next, we balance the fan-in of all MITEs. In this case, MITEs Q_z and Q_y have two inputs, whereas MITEs Q_x and Q_u have only one. To balance the fan-in in the MITE network, we add another unit input to MITEs Q_x and Q_u, each connected to V_{ref}, as shown in Fig. 19d. Next, we bias the network by forcing I_u into MITE Q_u, I_y into MITE Q_y, and I_x into MITE Q_x, and diode connect each one through one control gate, as shown in Fig. 19e. This MITE network implements Eq. 43, but it has two unused inputs. We can utilize these two inputs and complete the network by connecting V_{ref} to the collector of MITE Q_u, as shown in Fig. 19f. This MITE network also implements Eq. 43, but has no unused inputs. Finally, no consolidation is possible.

We begin the second MITE network by selecting I_z from the “CW” set and I_x from the “CCW” set and make a MITE for each one. Then, we make a new node in the circuit and couple it into MITE Q_z through one unit input and into MITE Q_x through one unit input, as shown in Fig. 20a. Next, we select I_u from the “CCW” set and make another MITE for it. We make a new node and couple it into MITE Q_x through one unit input and into MITE Q_u through one unit input, as shown in Fig. 20b. Next, we select I_y from the “CW” set and make another MITE for it. We make a new node and couple it into MITE Q_y through one unit input and into MITE Q_u through one unit input, as shown in Fig. 20c. Next, we balance the fan-in of all MITEs. In this case, MITEs Q_x and Q_u have two inputs, whereas MITEs Q_y and Q_z have only one. To balance the fan-in in the MITE network, we add another unit input to MITEs Q_y and Q_z, each connected to V_{ref}, as shown in Fig. 20d. Next, we bias the network by forcing I_u into MITE Q_u, I_y into MITE Q_y, and I_x into MITE Q_x, and diode connect each one through one control gate, as shown in Fig. 20e. This MITE network implements Eq. 43, but it has two unused inputs. We can utilize these two unused inputs and complete the network by connecting V_{ref} to the collector of MITE Q_y, as shown in Fig. 20f. Note that, if we had connected V_{ref} to the collector of MITE Q_u, then we would have introduced a

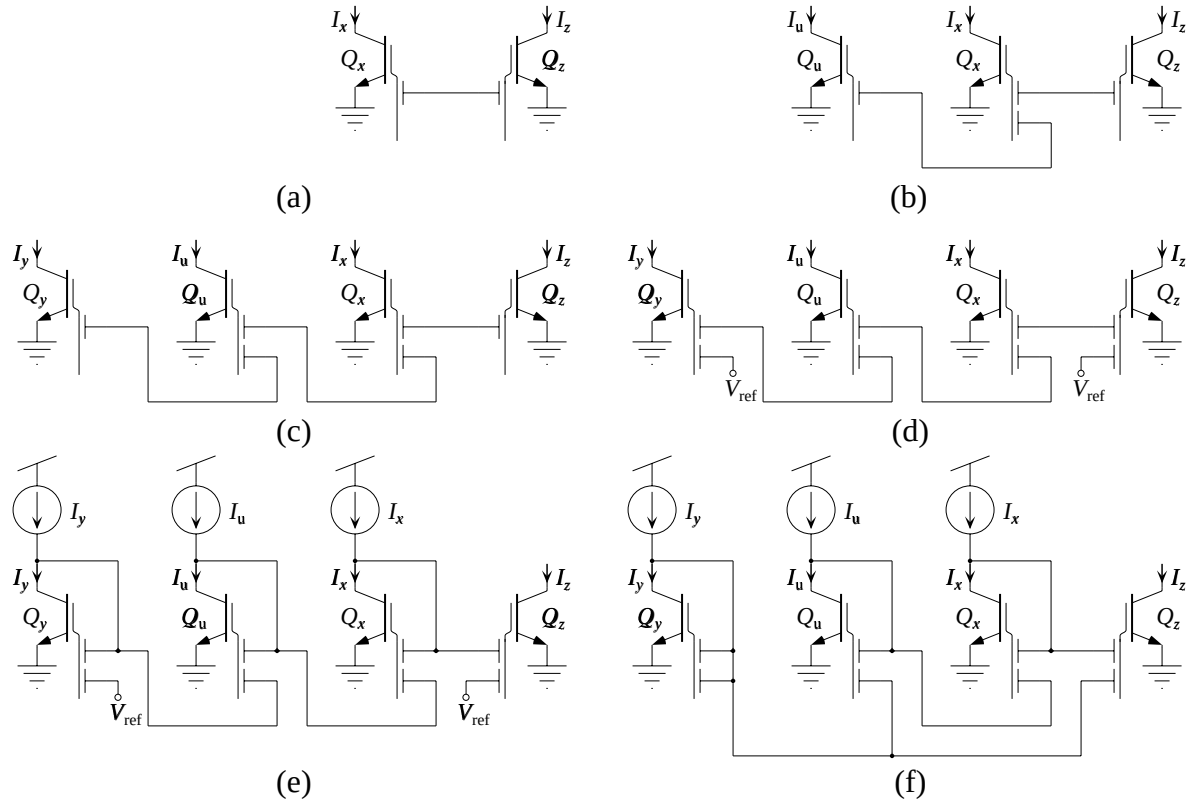


Figure 20: Synthesis of a one-quadrant MITE-network multiplier. (a) Beginning the network. (b) Building the network. (c) Building the network. (d) Balancing the network. (e) Biasing the network. (f) Completing the network.

positive feedback loop into the MITE network with a loop gain of unity, making the desired MITE network equilibrium an unstable one. If we had connected V_{ref} to the collector of MITE Q_x, then we would have introduced a negative feedback loop, creating the potential for instability. This MITE network also implements Eq. 43, but has no unused inputs. Finally, no consolidation is possible.

We have synthesized four different MITE networks (i.e., those shown in Figs. 19e, 19f, 20e, and 20f) that each implement Eq. 43. The circuits of Fig. 19 are more symmetric with respect to how many stages separate the x and y inputs from the z output than those of Fig. 20. Intuitively, we should expect that, a MITE network with fewer stages on average between the inputs and an outputs would be less sensitive to mismatch in MITE weight values than would be a MITE network with more stages. We have demonstrated this fact for these four one-quadrant multiplier circuits elsewhere [84]. The circuits shown in Fig. 19 differ from those shown in Fig. 20 in the order in which we selected the currents in the building process and where we chose to connect their MITEs. Because the number of ways in which currents can be chosen from a translinear-loop equation grows rapidly in the number of currents, it is difficult to say general things about how the chosen order

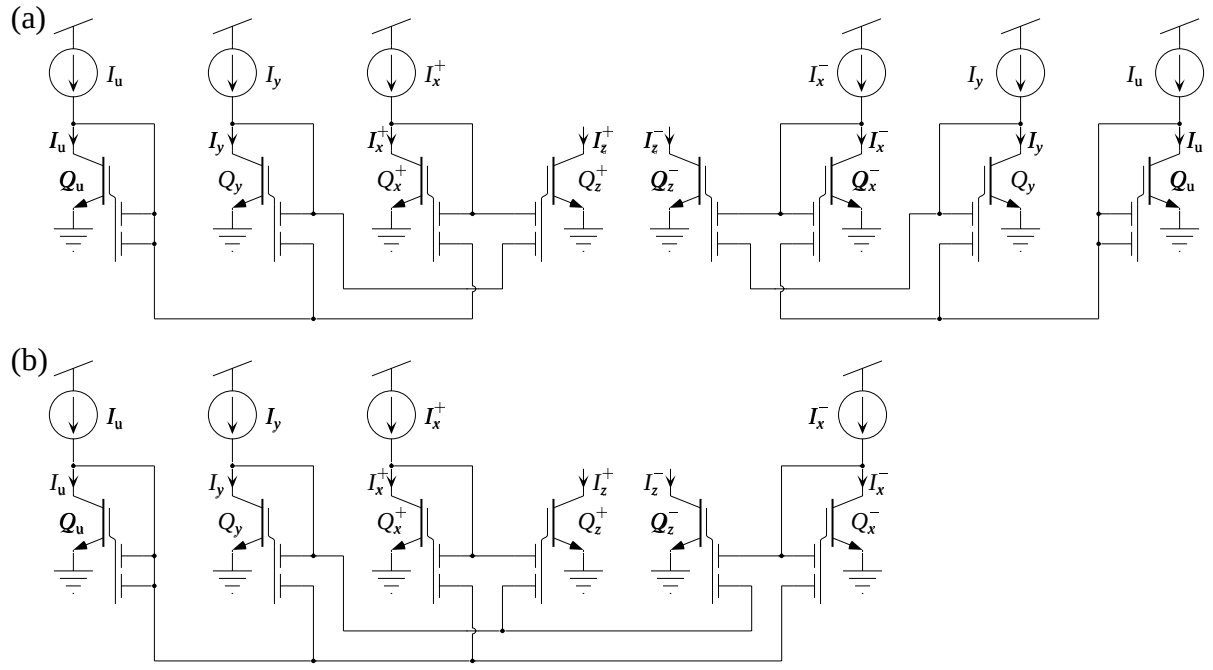


Figure 21: Synthesis of a two-quadrant MITE-network multiplier. (a) Two independent copies of the one-quadrant multiplier of Fig. 19f. (b) The final consolidated two-quadrant MITE-network multiplier circuit. Here we have shared the I_y and I_u circuitry between the two MITE networks.

affects the performance of the final MITE network. However, we shall make some observations. First, the more MITEs that we connect to any given MITE, the larger the required fan-in per MITE in the network as a whole, but the less the average number of intermediate stages between any two MITEs. We have shown previously [84] that any translinear-loop equation can be implemented as a MITE network with a maximum of one MITE between any pair of MITEs. MITE networks with fewer intermediate stages should be less sensitive to offset and noise accumulation than MITE networks with more intermediate stages. Additionally, the response time of a MITE network with fewer intermediate stages will be faster than that of a MITE network with more intermediate stages, because of parasitic node capacitances.

9.4 Synthesis of a Two-Quadrant MITE-Network Multiplier

Suppose that we want to implement a circuit that multiplies two quantities, x and y, where x can be either positive or negative and that y is strictly positive. Thus, their product, z, which is given by

$$z = xy, \tag{45}$$

can be either positive or negative. We shall represent y by I_y/I_u and we shall use a differential representation for x and z, as described in Section 3; that is, we represent x by

$$x = x^+ - x^-,$$

where $x^+ \equiv I_x^+/I_u$ and $x^- \equiv I_x^-/I_u$. Likewise, we represent z by

$$z = z^+ - z^-,$$

where $z^+ \equiv I_z^+/I_u$ and $z^- \equiv I_z^-/I_u$.

Next, we substitute these definitions for x, y, and z into Eq. 45 to get

$$\left(\frac{I_z^+}{I_u} - \frac{I_z^-}{I_u}\right) = \left(\frac{I_x^+}{I_u} - \frac{I_x^-}{I_u}\right)\left(\frac{I_y}{I_u}\right),$$

which we can rearrange to obtain

$$I_u I_z^+ - I_u I_z^- = I_y I_x^+ - I_y I_x^-.$$

One straightforward way to decompose this equation into a pair of translinear-loop equations is to equate individually the positive and negative terms on each side of the equation. Using this decomposition, we obtain the following pair of translinear-loop equations:

$$\underbrace{I_u I_z^+}_{\text{CW}} = \underbrace{I_y I_x^+}_{\text{CCW}} \qquad \text{and} \qquad \underbrace{I_u I_z^-}_{\text{CW}} = \underbrace{I_y I_x^+}_{\text{CCW}}.$$

By following the procedure shown in Fig. 19 for each of these translinear-loop equations, we obtain the two independent MITE networks shown in Fig. 21a. Note that in each MITE network, we supply a copy of I_u to a MITE that is diode connected through two unit inputs. The collector voltages of these two MITEs should be identical, so we can share a single MITE Q_u between the two networks. Also, in each network, we supply a copy of I_y to a MITE that is diode connected through a single control gate and its other control gate is connected to an identical voltage. Thus, their collector voltages are also identical, and we should be able to share a single MITE Q_y between the two circuits. The consolidated two-quadrant MITE-network multiplier is shown in Fig. 21b.

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