Accurate Rise Time and Overshoots Estimation in *RLC* Interconnects

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ABSTRACT

A closed form expression for the rise time of a gate driving a distributed *RLC* line is introduced that is within 8% of dynamic circuit simulations for a wide range of *RLC* loads. It is shown that the rise time decreases as the inductance effect increases. Also, a closed form expression for the maximum percentage overshoots is introduced that is within 5% error of dynamic circuit simulations. The expressions introduced here are analytical and differentiable over all damping conditions. Hence, these solutions are suitable for design and optimization tools.

1. INTRODUCTION

Inductance effects in on-chip interconnect structures have become increasingly significant due to longer metal interconnects, reductions in wire resistance (as a result of copper interconnects and wider upper-layer metal lines) and higher frequency operation. These effects are particularly significant for global interconnect lines such as those in clock distribution networks, signal buses, and power grids for high-performance microprocessors. On-chip inductance impacts these in terms of delay variations, degradation of signal integrity due to overshoots, oscillations, aggravation of signal crosstalk, and increased power grid noise[1]-[2].

Hence the traditional lumped or distributed *RC* models of the interconnect, especially of global wires, are no longer adequate since they can result in substantial errors in predicting both delay and crosstalk [1],[3].

Accurate analysis of inductance effects is therefore critical for predicting the performance of interconnects, which in turn are known to determine the chip performance. Also, accuracy of the inductance analysis is important for the precise quantification of their impact on performance optimization [5].

In [4], a closed form expression for the propagation delay of a CMOS gate driving a distributed *RLC* line was introduced and applied to the problem of repeater insertion in *RLC* interconnects.

The same approach is extended in this paper for the rise time and percentage overshoots of a CMOS gate. These parameters have significant importance in performance optimization, clock skew, slew rate, noise estimation, and power consumption.

The paper is organized as follows. In section 2, the rise time formula describing a gate driving a distributed *RLC* load is presented. In section 3, the percentage overshoots formula is presented. Some conclusions are offered in section 4 .

2. RISE TIME OF A GATE DRIVING AN *RLC* LOAD

A formula characterizing the rise time of a gate driving an *RLC* transmission line is presented. The closed form solution for the rise time is shown to be within 8% error of ELDO [6] simulations for a wide range of *RLC* lines.

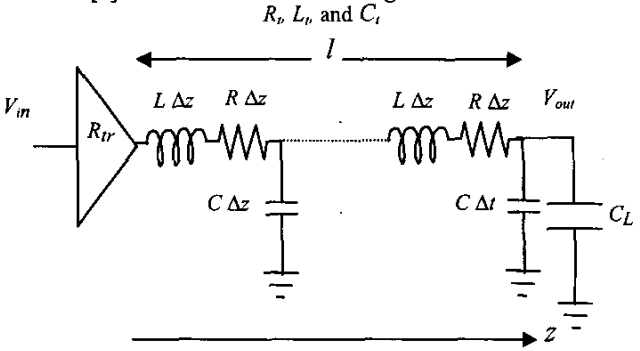

Fig. 1. A gate driving an *RLC* transmission line.

A gate driving an *RLC* transmission line representation of an interconnect line is shown in Fig. 1. R_t, L_t, and C_t are the total resistance, inductance, and capacitance of the line, respectively. The parasitic impedances R_t, L_t, and C_t are given by $R_t = Rl$, $L_t = Ll$, and $C_t = Cl$, respectively, where R, L, and C are the resistance, inductance, and capacitance per unit length of the interconnect and l is the length of the line. R_{tr} is the equivalent output resistance of the gate driving the interconnect. C_L is the input capacitance of the following gate at the end of the interconnect section. The input voltage V_{in} is a fast rising signal that can be approximated by a step signal. V_{out} is the far output voltage at the end of the interconnect section [4].

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A time scaling is applied by substituting t'/ω_n for each t where

$$\omega_n = \frac{1}{\sqrt{L_t(C_t + C_L)}}. \quad (1)$$

With this time scaling, the transfer function $V_{out}(S')/V_{in}(S')$ is a function of only three variables: ζ, R_T, and C_T [4]which are

$$R_T = \frac{R_{tr}}{R_t}, \quad (2)$$

$$C_T = \frac{C_L}{C_t}, \quad (3)$$

$$\zeta = \frac{R_t}{2}\sqrt{\frac{C_t}{L_t}} \cdot \frac{R_T + C_T + R_T C_T + 0.5}{\sqrt{(1 + C_T)}}. \quad (4)$$

The first few terms of the series expansion in S' for the transfer function $V_{out}(S')/V_{in}(S')$ are

$$\frac{V_{out}(S')}{V_{in}(S')} = \frac{1}{1 + 2\zeta S' + \left(\frac{0.5 + C_T}{1 + C_T} + 1\zeta^2\left(1 - \frac{R_T^2 + C_T^2 + (R_T C_T)^2}{(R_T + C_T + R_T C_T + 0.5)^2}\right)\right)S'^2 + \cdots}. \quad (5)$$

Thus, for a unit step input function, the output voltage waveform $V_{out}(t') = (1/S)^* V_{out}(S')/V_{in}(S')$ is also a function of the three variables ζ, R_T, and C_T. The scaled time t'_r can be calculated by solving both $V_{out}(t'_{r90\%}, \zeta, R_T, C_T) = 0.9$ and $V_{out}(t'_{r10\%}, \zeta, R_T, C_T) = 0.1$ then substituting in $t'_r = t'_{r90\%} - t'_{r10\%}$ which means that t'_r is only a function of ζ, R_T, and C_T. Thus, the rise time of an RLC line with a source resistance R_{tr} and a load capacitance C_L has the form

$$t_r = \frac{t'_r(\zeta, R_T, C_T)}{\omega_n}. \quad (6)$$

Note that this solution is a characteristic of an RLC line and that no approximations have been made in deriving this result.

The scaled rise time t'_r is dimensionless since ω_n has the units of 1/time. t'_r is a function of only three variables which is the canonical number of variables to describe t'_r. There are several ways to select these three variables. The three variables chosen here are R_T, C_T, and ζ since these variables are physically intuitive. The variables R_T and C_T characterize the relative significance of the gate parasitic impedances with respect to the interconnect parasitic impedances [4]. Increasing R_T and C_T demonstrates that the gate parasitic impedances affect the rise time even further. The third variable ζ is the coefficient of S' and was shown in [4] to characterize the relative importance of inductance with $\zeta < 1$ indicating large inductance effects. Note that the three variables R_T, C_T, and ζ are not independent since ζ is a function of R_T and C_T.

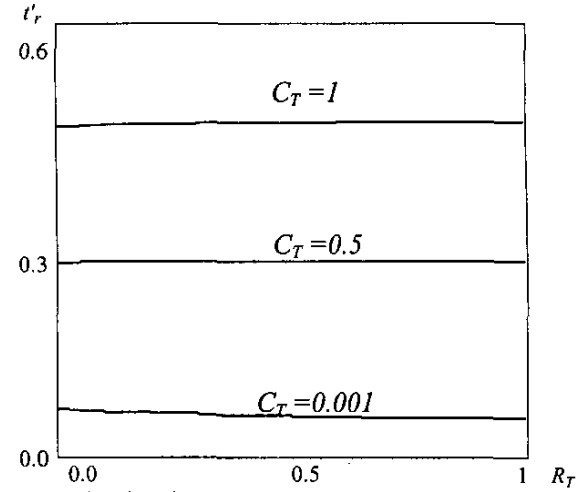

Fig. 2. The rise time is plotted versus R_T for different values of C_T, when ζ=0.1 .

As shown in Fig. 2, the dependence on R_T is fairly weak. Based on this observation, the rise time can be modeled by the following function

$$t_r = \frac{t'_r(\zeta, C_T)}{\omega_n}. \quad (7)$$

Note that the rise time is primarily a function of ζ and C_T. This characteristic does not imply that the transistor driving the interconnect has a weak effect on the rise time since ζ includes the effect of R_T. Note also that this effect is particularly weak in the range where R_T and C_T are between zero and one. This range is most important for global interconnect and long wires in current deep sub-micrometer technologies [4]. Thus, the rise time is primarily a function of ζ, and C_T which collects the five impedances that affect the rise time, R_t, L_t, C_t, R_{tr}, and C_L, into two parameters.

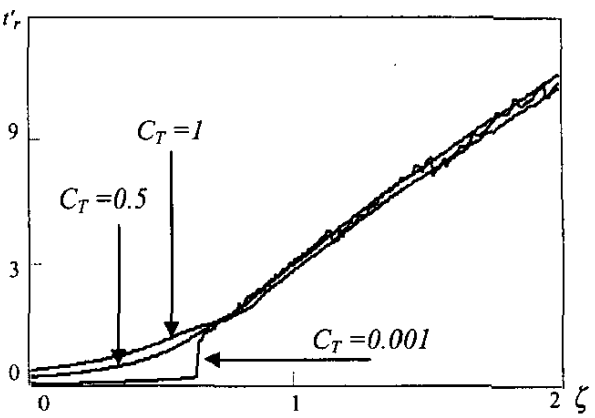

Fig. 3. ELDO [6] simulations of the time scaled rise time t'_r of an RLC transmission line with a source resistance R_{tr} and a load capacitance C_L. The rise time is plotted versus ζ for different values of C_T.

ELDO [6] simulations of the time scaled rise time of a gate driving an *RLC* transmission line t'_r as a function of ζ, R_T, and C_T are shown in Fig. 3. A curve fitting method is used to minimize the error when C_T is between zero and one as shown in Fig. 3.

Using this approach the rise time can be modeled by the following function

$$t'_r = ae^{b\zeta^c} + \left(\frac{1}{1+e^{-d(\zeta-e)}}\right)\left(4.65\zeta - ae^{b\zeta^c} - 1.8\right), \tag{8}$$

Table 1. Parameters in (8) corresponding to different values of C_T.

C_T	a	b	c	d	e
0.001	0.0418	2.402	1	400	0.63
0.03	0.044	2.4	1.05	300	0.615
0.05	0.052	2.5	1.22	370	0.57
0.07	0.06	2.6	1.32	100	0.559
0.1	0.0618	2.7	1.46	30	0.55
0.2	0.105	4	1.4	30	0.55
0.3	0.146	3.5	1.32	30	0.55
0.4	0.19	3	1.22	30	0.55
0.5	0.22	2.7	1.12	30	0.65
0.7	0.29	2.4	1.05	30	0.65
1	0.39	2	1	30	0.65

Curve fitting techniques were applied to the parameters in Table 1 to model a, b, c, d and e by the following functions,

$$a = \frac{(0.0148 - 0.014C_T + 5.9C_T^2 - 29.54C_T^3)e^{-100(C_T-0.1)}}{1+e^{-100(C_T-0.1)}} + 0.019 + 0.44C_T - 0.07C_T^2 \tag{9}$$

$$b = \frac{\left(2.39 + 1.83C_T + 53.7C_T^2\right)e^{-100(C_T-0.2)} + \left(5.1 - 6.21C_T + 3.18C_T^2\right)}{1+e^{-100(C_T-0.2)}} \tag{10}$$

$$c = \frac{\left(1 + 4.65C_T\right)e^{-100(C_T-0.1)} + \left(1.59 - 1.18C_T + 0.59C_T^2\right)}{1+e^{-100(C_T-0.1)}} \tag{11}$$

$$d = 570\ e^{-40\,C_T} + 30 \tag{12}$$

$$e = \frac{1}{1+e^{-100(C_T-0.0435)}+e^{100(C_T-0.45)}}\left\{0.65e^{100(C_T-0.45)} + 0.05e^{-15C_T} + 0.55 + \left(0.627 + 2.59C_T - 316.87C_T^2 + 10767C_T^3 - 118700C_T^4\right)e^{-100(C_T-0.0435)}\right\} \tag{13}$$

ELDO [6] simulations of the rise time of an *RLC* transmission line as compared to t'_r in (8) are shown in Table 2.

Note that the solution exhibits high accuracy (the maximum error is less than 8% and the mean error is 4.1%) for a wide range of interconnect (R_t, L_t, and C_t) and gate impedances (R_{tr} and C_L). Note also that the simulation data listed in Table 2 include those cases where the response is underdamped and overshoots occur (high inductive effects), and those cases where the response is overdamped (low inductive effects).

3. OVERSHOOTS FORMULA

The voltage overshoots is the amount by which the output voltage exceeds the supply voltage at high inductive effects. The percentage overshoots is calculated by the following formula:

$$\%overshoots = \frac{V_{out}(t) - V_{DD}}{V_{DD}}, \tag{14}$$

where V_{DD} is the supply voltage.

Similar to the rise time case, the percentage overshoots has a fairly weak dependence on R_T , making the overshoots primarily a function of ζ, and C_T.

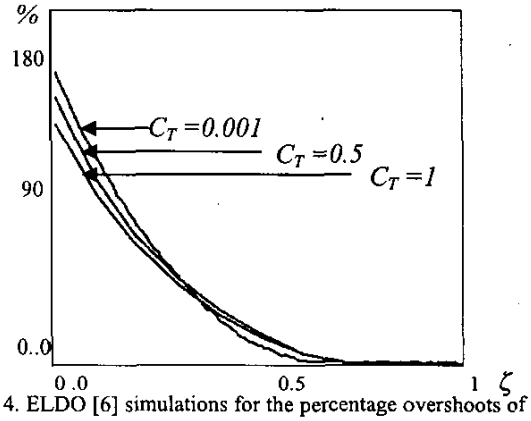

Fig. 4. ELDO [6] simulations for the percentage overshoots of an *RLC* transmission line. with a source resistance R_{tr} and a load capacitance C_L, is plotted versus ζ for different values of C_T.

$$\%\,overshoots = \left(149 - 24C_T\right)e^{-3.55\left(\zeta + \frac{0.00025}{C_T}\right)\left(1.24 + \frac{0.00022}{C_T}\right)} + \frac{0.001}{C_T} - \left(5 - 2C_T\right)e^{-\left(15 + \frac{0.035}{C_T}\right)\left(\zeta - 0.72 + \frac{0.0012}{C_T}\right)} \tag{15}$$

ELDO [6] simulations of the percentage overshoots of a gate driving an *RLC* transmission line as a function of ζ and C_T are shown in Fig. 4. A curve fitting method is used to minimize the error when C_T is between zero and one as shown in Fig. 4.

ELDO [6] simulations of the percentage overshoots of an *RLC* transmission line as compared to (15) are shown in Table 3. Note that the solution exhibits high accuracy (the maximum error is less than 5% and the mean error is 2.6%) for a wide range of interconnect (R_t, L_t, and C_t) and gate impedances (R_{tr} and C_L).

Table 2. Comparison of t_r in (8) to ELDO simulations characterizing the rise time of a gate driving an *RLC* transmission line. C_t = 1 pF and R_{tr} = 25 Ω.

R_T	L_t(nH)	C_T = 0.1			C_T = 0.5			C_T = 1.0		
		(8)	ELDO	Error	(8)	ELDO	Error	(8)	ELDO	Error
0.1	2	329	305	7.8%	555	529	4.9%	882	826	6.7%
	5	282	263	7.2%	502	496	1.2%	820	795	3.1%
	8	248	230	7.8%	463	464	0.21%	776	765	1.4%
	10	229	213	7.5%	441	440	0.22%	752	733	2.6%
0.5	2	48.5	47.6	1.9%	105	99.8	5.2%	185	182	1.6%
	5	10.9	11.8	7.6%	66.4	70.7	6%	131.9	142.7	7.5%
	8	11.2	12.1	7.4%	63.2	64.2	1.5%	132	139	5%
	10	11.97	12.73	5.9%	63.1	63.3	0.3%	133	137	2.9%
1.0	2	11	10.24	7.4%	50.6	53.9	6.1%	97.7	97.3	0.4%
	5	8.5	9.2	7.6%	45.1	44.2	2%	93.3	93.4	0.1%
	8	9.6	10.4	7.6%	46.9	46.3	1.3%	99	96.7	2.3%
	10	10.3	11.1	7.2%	48.7	48.2	1%	102.3	99.5	2.8%

Table 3. Comparison of percentage overshoots error calculated in (15) to ELDO simulations characterizing the percentage overshoots error of a gate driving an *RLC* transmission line. C_t = 1 pF , R_{tr} = 25 Ω and R_t = 25 Ω.

ζ	C_T = 0.001			C_T = 0.5			C_T = 1		
	(15) (%)	EL--DO (%)	Error (%)	(15) (%)	EL--DO (%)	Error (%)	(15) (%)	EL--DO (%)	Error (%)
1	1.2	1.17	2.56	0.02	0.02	0	0	0	0
0.8	1.79	1.72	4	0.4	0.39	2.5	3.3	3.27	0.9
0.6	2.28	2.39	4.6	6.97	6.97	0	6.83	6.88	0.7
0.4	24.1	25.2	4.3	27.6	29	4.8	26.7	25.5	4.7
0.2	73.6	74.1	0.67	70.4	67.7	3.9	62.9	64.2	2
0.1	111	109	1.8	103	98.1	4.9	89.9	94.3	4.6

4. CONCLUSIONS

Closed form solutions for the rise time and percentage overshoots of a CMOS gate driving a distributed *RLC* load are presented. These expressions are analytical, differentiable, and within 8% error of ELDO simulations.

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