

A 13-Bit, 1.4-MS/s Sigma-Delta Modulator for RF Baseband Channel Applications

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Abstract—A 13-bit, 1.4-MS/s, sixth-order cascaded sigma-delta modulator oversampling at 16 X is implemented in a 0.72 μm complementary metal-oxide-semiconductor process for use in the baseband path of a radio-frequency receiver. The modulator achieves 77 dB of dynamic range and dissipates 81 mW from a 3.3 V supply. It is characterized for the blocking and intermodulation requirements of a cordless telephone application.

Index Terms—Analog-digital conversion, radio receivers, sampled-data circuits, sigma-delta modulation, switched-capacitor circuits.

I. INTRODUCTION

WITH growing demand for portable wireless devices, recent efforts in the design of integrated circuits for radio-frequency (RF) communication receivers have focused on achieving higher levels of integration in a low cost technology such as complementary metal-oxide-semiconductor (CMOS) and adaptability to multiple RF communication standards [1], [2]. Both direct-conversion and wide-band intermediate frequency (IF) with double-conversion receiver architectures increase integration by moving channel select filtering from IF to baseband where on-chip solutions are practical [3], [4]. Baseband channel select filtering requires wide dynamic range and high linearity since a weak desired signal must be detected in the presence of strong adjacent channel interferers. In recent work, baseband channel select filtering has been done in the analog domain using either continuous-time or switched-capacitor filters [5]–[8]. However, to achieve adaptability to multiple communication standards, channel select filtering should be performed in the digital domain where programmable filters are more easily implemented. This requires a wide-band, high-resolution analog-to-digital (A/D) converter that can digitize both the desired channel and the adjacent channel interferers. Oversampled sigma-delta modulators are uniquely suited to this application because the adjacent channel interferers fall into the same band as the high-pass shaped quantization noise. Both the quantization noise and interferers can be removed with the same digital decimation filter.

This work focuses on the design of a sigma-delta modulator for use in RF receivers with relatively wide channel

bandwidths such as cordless telephones and wireless local-area networks (LAN's). Handling these wide bandwidths without excessive power dissipation requires a variety of strategies at the modulator architecture and circuit design levels. Section II describes the RF baseband channel application, compares analog and digital channel select filtering techniques, and develops additional performance metrics required to characterize a sigma-delta modulator for this application. Section III explores sigma-delta architecture tradeoffs with the goal of minimizing power dissipation and develops a 2-2-2 cascade architecture at 16 \times oversampling ratio. Section IV describes a kT/C noise limited capacitor scaling technique to reduce the power dissipation of the modulator. Switched-capacitor circuit design issues with emphasis on a two-stage operational amplifier with all N-channel (N)MOS signal path and capacitive coupling between the stages are discussed in Section V. Section VI presents experimental results, including characterization of the blocking and intermodulation performance required by the Digital Enhanced Cordless Telecommunications (DECT) standard.

II. RF BASEBAND CHANNEL APPLICATION

The choice of RF receiver architecture affects the ability to integrate the entire receive function on a single chip and the ability of the receiver to adapt to multiple communication standards. The conventional superheterodyne receiver shown in Fig. 1(a) employs high-Q off-chip bandpass filters, which are not amenable to integration, to perform image rejection and channel selection at IF. The use of an IF channel select filter and programmable gain amplifier greatly alleviates the dynamic range and distortion requirements on the baseband processing. In addition, the off-chip IF channel select filter is of specific bandwidth, making it difficult to adapt the receiver to multiple communication standards.

Both the direct-conversion and wide-band IF with double-conversion receiver architectures [Fig. 1(b) and (c), respectively] achieve integration by eliminating the off-chip IF filter and performing channel select filtering at baseband [3], [4]. While the direct-conversion and wide-band IF receiver architectures differ in the RF path, these receivers are identical with respect to their dynamic range and bandwidth requirements at baseband. Furthermore, with proper choice of baseband filter topology and A/D converter, it is possible to make these receivers adapt to multiple communications standards.

A. Channel Select Filtering

Baseband channel select filtering may be performed in either the analog or the digital domain. Fig. 2(a) shows an

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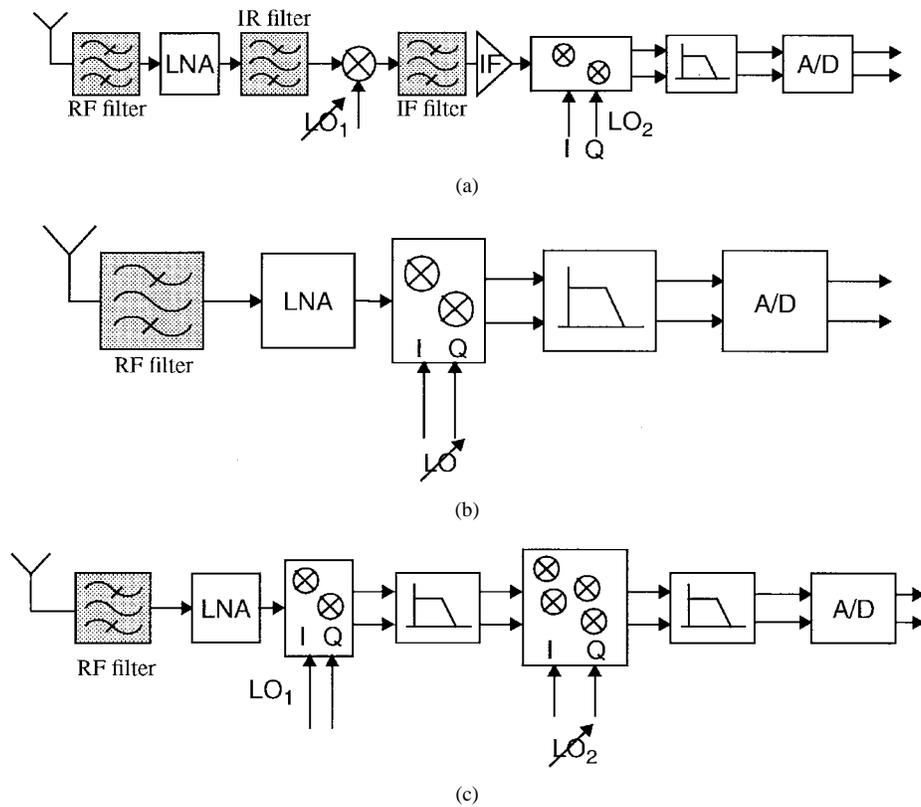


Fig. 1. RF receiver architectures. (a) Superheterodyne. (b) Direct conversion. (c) Wide-band IF with double conversion.

example analog baseband path for cordless applications, which consists of a continuous-time antialiasing filter, switched-capacitor filter including automatic gain control (AGC), and pipelined A/D converter [7]. The continuous-time antialiasing filter provides the necessary rejection at the switched-capacitor filter sampling frequency and some rejection of the interfering channels far away from the carrier. The switched-capacitor filter completes the selection of the desired channel and includes AGC to relax the dynamic range requirements on the 10-bit pipelined A/D converter. The digital baseband path in Fig. 2(b) consists of a continuous-time antialiasing filter, sigma-delta modulator, and digital decimation filter. The antialiasing filter in the digital baseband path performs the same function as in the analog case: rejection at the modulator sampling frequency and some rejection of interfering signals far away from the carrier. The sigma-delta modulator digitizes the desired channel with the adjacent channel interferers occupying the same frequency band as the quantization noise. The digital decimation filter removes both the interferers and quantization noise. Unlike the analog baseband path, AGC cannot be used to improve the dynamic range of the system because there is no significant filtering of the adjacent channel blockers in the analog domain; a simple low noise amplifier bypass mode may be required to avoid overloading the sigma-delta in the case of a large desired signal.

Both the analog and the digital channel select filtering schemes may be integrated into a direct-conversion or wide-band IF with double-conversion receiver. However, programmable filters that adapt to the different bandwidth, blocking, and dynamic range requirements of different RF

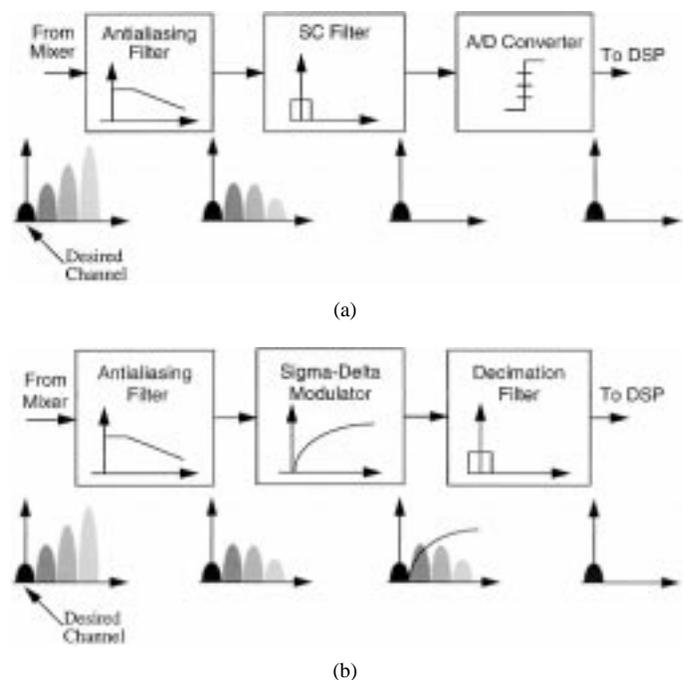


Fig. 2. Channel select filtering. (a) Analog. (b) Digital.

communication standards can be more easily implemented in the digital domain. As a result, adaptability to multiple communication standards favors the digital approach at baseband.

B. RF Performance Metrics for Sigma-Delta Modulators

The RF application places different requirements on a sigma-delta modulator than conventional audio rate applica-

tions. This section develops the specifications necessary to design and characterize a sigma-delta modulator for an RF application. For portable wireless devices, such as cordless and cellular telephones, minimizing power dissipation is a key requirement to extend battery life. At both the sigma-delta and circuit design levels, a variety of low-power techniques need to be employed. With the reduction of power supplies to 3.3 V or below in deep submicrometer CMOS processes, reduced signal swings will make these power-reduction strategies even more important.

This work investigates the use of a sigma-delta modulator in the baseband path for RF standards with wide channel bandwidths, such as cordless telephones and wireless LAN's. The DECT standard was particularly emphasized. For DECT, the baseband processing block, which includes the antialiasing filter and sigma-delta modulator, must achieve greater than 70 dB of dynamic range in a 700 kHz bandwidth. Additional dynamic range is desirable to reduce the impact of the baseband on the overall receiver noise figure.

The linearity requirements of a sigma-delta modulator in an RF application are set by the third-order intermodulation of large adjacent channel interferers into the desired signal band. The appropriate specification for a receiver and each of its subblocks is the input-referred third-order intermodulation intercept point (IIP_3). For DECT with 35 dB of receiver gain in front of the antialiasing filter, a baseband IIP_3 of approximately 17 dBV is required [7].

Desensitization or an increase in the modulator noise floor can occur when a small desired signal must be detected in the presence of a much larger adjacent channel signal. An appropriate specification for desensitization is to determine the out-of-band signal level for each channel that degrades the SNR of the smallest in-band signal by 1 dB. DECT requirements are described in detail in Section VI.

III. SIGMA-DELTA ARCHITECTURE TRADEOFFS

This section explores tradeoffs among various architectures that can be used to implement a wide bandwidth sigma-delta modulator. The focus is on selecting the appropriate architecture to minimize power dissipation given the DECT specifications described above and a $0.72 \mu\text{m}$ double-poly, double-metal CMOS process. As shown in the approximate relationship in (1), the designer has three degrees of freedom to achieve a given dynamic range (DR) [9]. The designer can trade off among the modulator order (L), oversampling ratio (M), and number of bits in the quantizer (B). Traditional audio rate modulators have oversampled at $64\times$ or

$$DR = \frac{3}{2} \frac{2L+1}{\pi^{2L}} M^{2L+1} (2^B - 1)^2 \quad (1)$$

above to achieve adequate dynamic range. However, amplifier settling constraints dictate that a modulator with 1.4 MS/s Nyquist rate in a $0.72 \mu\text{m}$ CMOS process must operate at $32\times$ oversampling ratio or below. This suggests that a modulator of relatively high order and possibly a multibit quantizer will be required.

Several wide-bandwidth sigma-delta modulators have been implemented previously [10]–[12]. Possible approaches in-

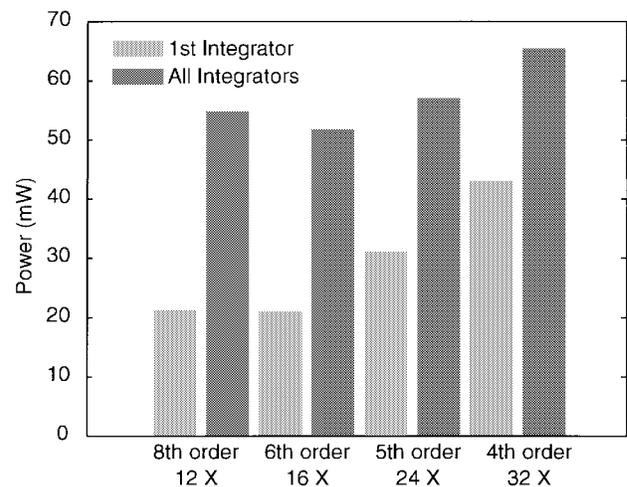


Fig. 3. Simulated power dissipation as a function of order and oversampling ratio.

clude cascade (MASH) architectures and single-loop architectures with multibit quantizers. Single-loop architectures with single-bit quantizers cannot achieve the required dynamic range at low oversampling ratio [13]. None of these previous converters paid particular attention to power dissipation, which is required by the RF application. Furthermore, these converters were implemented at 5 V supply with greater signal swings available rather than at the 3.3 V supply or below typically employed in RF applications.

A. Modulator Oversampling Ratio and Order Selection for Minimum Power Dissipation

The modulator oversampling ratio and order need to be optimized to minimize power dissipation. This approach assumes a cascade architecture so that the complexity associated with the use of either calibration or mismatch shaping techniques for multibit D/A converter at the input of a single loop can be avoided. Furthermore, this work only considers power dissipation in the analog portions of the modulator. Power dissipation in the decimation filter should also be considered to achieve the minimum power dissipation in the overall baseband processing system. Fig. 3 shows SPICE simulations of the integrators required to implement modulators of different orders and oversampling ratios in a $0.72 \mu\text{m}$ CMOS process to select the minimum power architecture. The first integrator dominates the power dissipation because it is limited by kT/C noise and must settle to the accuracy of the overall modulator independent of oversampling ratio. Subsequent integrators may employ smaller capacitors and settle less accurately, which reduces their power dissipation, as described in Section IV. As the oversampling ratio increases from 16 to $32\times$, first integrator power increases because 1) parasitic capacitances (C_{db} and C_{gs} of the MOS transistors), which become a larger fraction of the kT/C limited sampling capacitance, must be driven and 2) clock nonoverlap and rise and fall times become a larger fraction of the clock cycle, reducing the available settling time. With an oversampling ratio reduction from 16 to $12\times$, an eighth-order modulator is required to meet quantization noise specifications. Even if

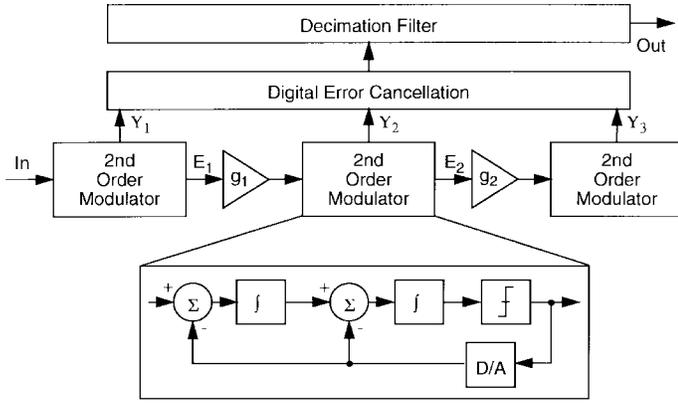


Fig. 4. A 2-2-2 cascade sigma-delta modulator.

matching constraints would allow for the implementation of an eighth-order cascade, the additional integrators required at the back end of the modulator will result in increased overall power dissipation. Thus, the simulations show that a sixth-order modulator at $16\times$ oversampling ratio minimizes power dissipation by providing the best tradeoff between parasitic capacitance and clocking issues and increased modulator order to reduce quantization noise.

B. 2-2-2 Cascade Architecture

The sixth-order modulator oversampling at $16\times$ is implemented as a cascade of three second-order sigma-delta loops as shown in Fig. 4. The cascade architecture recombines the outputs of each of the second-order modulators in the digital domain to achieve sixth-order noise shaping. Inherently linear single-bit D/A converters are employed in the first two stages while a three-level D/A converter is employed in the lower resolution third stage to improve dynamic range. While the 2-2-2 cascade is similar to the architecture reported in [14], a single-bit quantizer in the first stage avoids the requirement of an out-of-band dither signal to keep a three-level quantizer in the first sigma-delta loop active.

Capacitor mismatch in the first analog interstage gain coefficient (g_1) represents a gain mismatch between the analog modulator cascade and digital recombining network, resulting in incomplete quantization error cancellation. Following a method similar to that in [15], (2) shows that mismatch in the interstage gain (δg_1) causes first-stage quantization noise $[E_1(z)]$ shaped by a second-order difference to leak to the output of the overall modulator and increase the quantization noise floor. At

$$Y(z) \approx z^{-6}X(z) + \frac{1}{g_1 g_2} (1 - z^{-1})^6 E_3(z) - \delta g_1 (1 - z^{-1})^2 z^{-4} E_1(z) \quad (2)$$

13-bit resolution, simulations show that 0.4% capacitor matching is required; this level of matching is achievable without resorting to calibration. It is important to note that at $16\times$ oversampling ratio and 0.4% capacitor mismatch, the third stage in the cascade reduces the quantization noise floor by 18 dB as compared to using just the first two stages of the modulator.

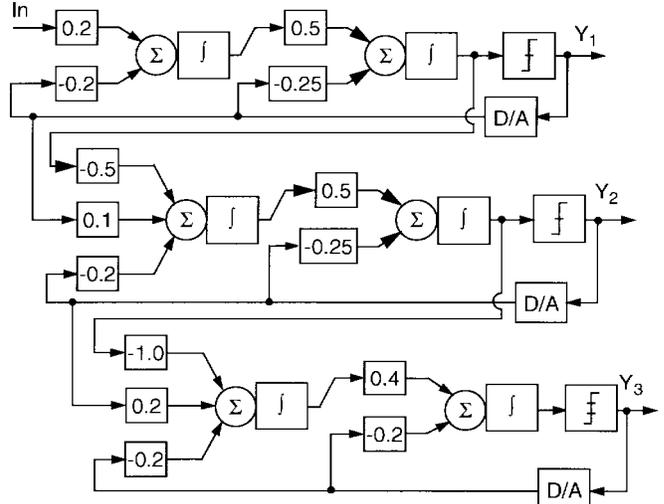


Fig. 5. Signal scaling for the 2-2-2 cascade sigma-delta modulator.

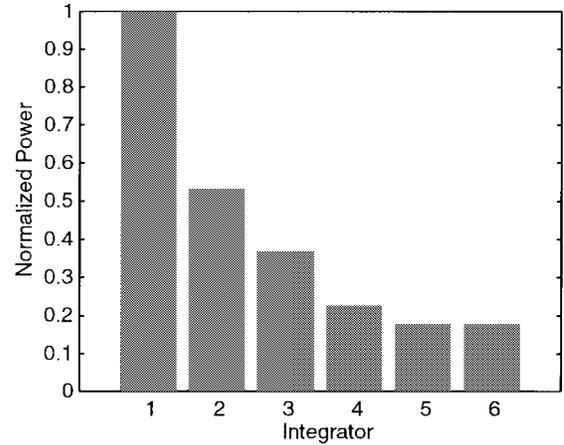


Fig. 6. Normalized power dissipation of each integrator with capacitor scaling.

The 2-2-2 cascade needs to be mapped into a suitable format to be implemented with switched-capacitor circuits. This entails signal scaling, or selecting forward and feedback path coefficients for each integrator in the cascade, with a goal of maximizing the modulator overload level [17]. The coefficients shown in Fig. 5 result in a modulator overload level of -2 dBFS.

IV. CAPACITOR SCALING

The power dissipation of switched-capacitor circuits is fundamentally limited by kT/C noise. To minimize power dissipation, the designer must use the minimum sized sampling capacitor required by kT/C noise considerations for each integrator in the cascade. Using a noise-shaping argument, the total input-referred thermal noise ($S_{N, \text{TOT}}$) of the modulator is given by (3), where S_{Ni} is the input-referred

$$S_{N, \text{TOT}} = \frac{S_{N1}}{M} + \frac{\pi^2}{3A_2^2 M^3} S_{N2} + \frac{\pi^4}{5A_3^2 M^5} S_{N3} + \frac{\pi^6}{7A_4^2 M^7} S_{N4} + \frac{\pi^8}{9A_5^2 M^9} S_{N5} + \frac{\pi^{10}}{11A_6^2 M^{11}} S_{N6} \quad (3)$$

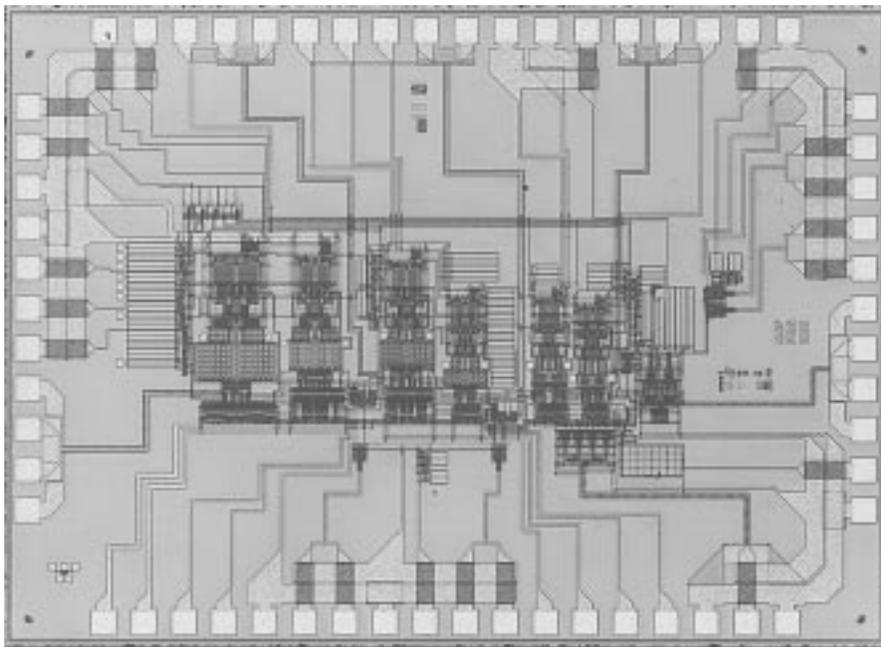


Fig. 10. Die photo.

capacitor common-mode feedback. Capacitor C_B is switched to fixed references V_{BN2} and V_{B01} on phase one of the two-phase nonoverlapping clocks and then switched into the circuit on phase two. Bias voltage V_{BN2} is generated by a replica of second-stage input devices M_9 and M_{10} while voltage V_{B01} is a fixed reference voltage generated in a similar manner to the amplifier output common-mode voltage. One drawback of the dynamic level shift is that the effective transconductance of the second-stage NMOS devices (G_{Meff}) is reduced by the capacitive divider given in (4), where C_{G9} represents the total gate capacitance of the second-stage NMOS device. This implies

$$G_{Meff} = \frac{C_{SH}}{C_{SH} + C_{G9}} \quad (4)$$

that capacitor C_{SH} must be large compared to the C_{G9} to maintain reasonable transconductance.

The amplifier also employs compensation to the cascode node of the first stage rather than conventional Miller compensation, which results in wider bandwidth [19]–[22]. Detailed design procedures and power-optimization techniques for this type of amplifier are given in [23] and [24].

Fully differential amplifiers require common-mode feedback to define the bias points at high-impedance nodes. This amplifier employs standard switched-capacitor common-mode feedback but requires an inversion circuit to achieve negative feedback. Inversion is accomplished through the use of a PMOS differential pair, as shown in Fig. 8. The PMOS differential pair adjusts the common-mode level by increasing or decreasing current I_{cmfb} , which either adds or bleeds current from the input devices (M_1 and M_2) as needed.

All NMOS switches are employed to reduce parasitic loading on the amplifiers. On-chip charge pumps shown in Fig. 9 are used to boost the clocks from 3.3 to 5 V to provide the necessary gate overdrive [18].

VI. EXPERIMENTAL RESULTS

An experimental prototype 2-2-2 cascade sigma-delta modulator was fabricated in a 0.72 μm double-poly double-metal CMOS process. The modulator samples at 22.4 MS/s with 1.4 MS/s Nyquist rate. The prototype dissipates 81 mW from a 3.3 V supply. The chip area excluding the pads is $2.7 \times 1.3 \text{ mm}^2$. Digital postprocessing in software is used to recombine the outputs of the cascaded second-order sections and evaluate the modulator using such functions as fast Fourier transforms (FFT's) and signal-to-noise-ratio (SNR) calculations. A die photo is shown in Fig. 10.

For a 100 kHz sinusoidal input, the modulator achieves 72 dB of peak SNR, 71 dB of peak signal-to-noise-and-distortion ratio (SNDR), and 77 dB of dynamic range as shown in Fig. 11. The FFT of the 700 kHz baseband for a -27 dBFS signal in Fig. 12 shows that the modulator performance is limited by thermal noise from the first and second integrators.

Fig. 13 shows the measured input-referred third-order IIP (IIP_3) of 28 dBV. The measurement procedure is to feed an in-band tone (100 kHz in this case) into the modulator to determine the linear response. Then, two tones at 3.4 and 6.5 MHz (two and four DECT channels away from carrier) are fed into the modulator to determine the spurious (intermodulation) response.

Densitization or an increase in the modulator noise floor can occur when a small desired signal must be detected in the presence of large adjacent channel interferers. Fig. 14 shows the DECT blocking profile assuming 35 dB of gain in front of the sigma-delta, the same profile following a three-pole antialiasing filter with cutoff frequency at 1.5 MHz (required to reject out-of-band signals at the sampling frequency), and the measured signal levels for three adjacent DECT channels that degrade the in-band SNR of a small desired signal by 1 dB.

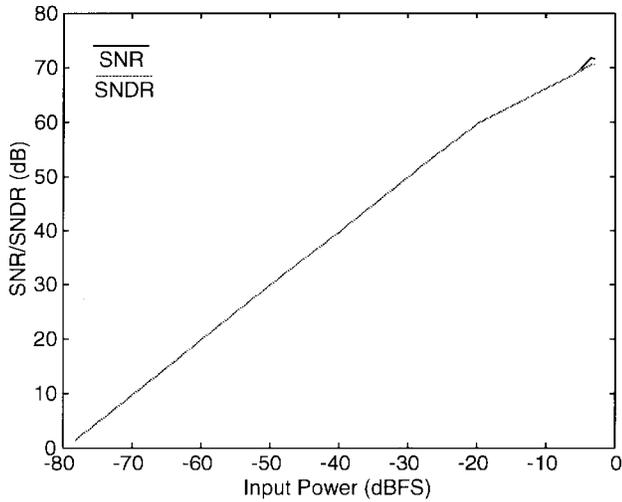


Fig. 11. Measured SNR/SNDR.

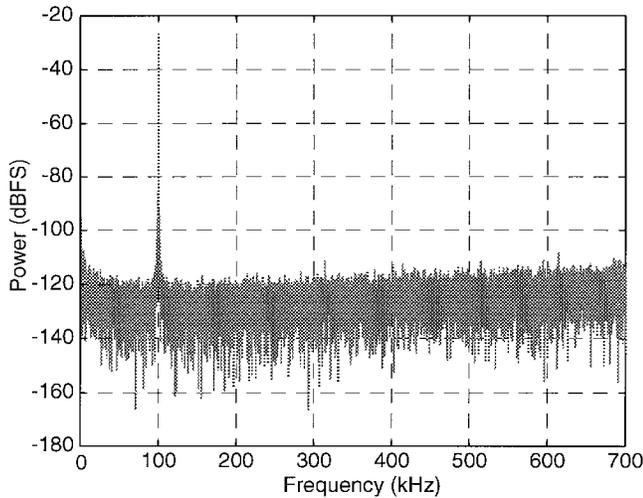
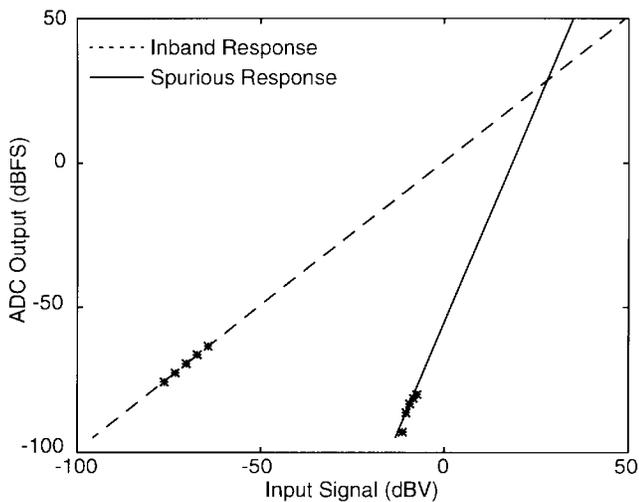


Fig. 12. FFT of 700 kHz baseband.

Fig. 13. Measured out-of-band input-referred third-order intermodulation intercept (IIP_3).

Higher frequency channels will be attenuated significantly by the continuous-time antialiasing filter and will not appreciably desensitize the modulator.

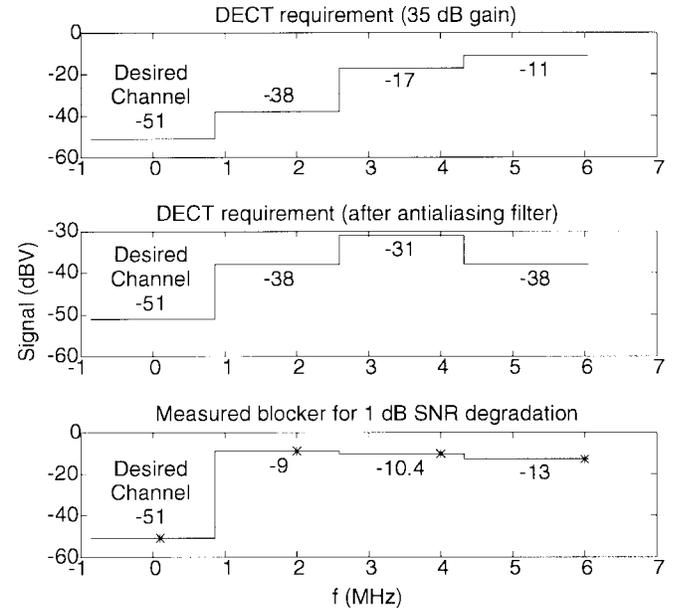


Fig. 14. Blocking performance.

TABLE I
PERFORMANCE SUMMARY

Technology	0.72 μm DPDM CMOS
Active area	2.7 x 1.3 mm^2
Power supply	3.3 V
Power dissipation	81 mW
Nyquist rate	1.4 MS/s
Sampling rate	22.4 MS/s
Dynamic range	77 dB
Peak SNR	72 dB
Peak SNDR	71 dB
Out-of-band IIP_3	28 dBV

VII. CONCLUSION

This paper presented a 13-bit, 1.4-MS/s sigma-delta modulator that allows for programmable digital channel select filtering in the baseband path of direct-conversion and wide-band IF with double-conversion RF receivers. The modulator meets the dynamic range, intermodulation, and blocking requirements of the DECT standard. A 2-2-2 cascade modulator oversampling at $16\times$ minimized power dissipation by providing the best tradeoff between driving parasitic capacitances at high speed and increased quantization noise at low oversampling ratios. Capacitor scaling to the minimum value required by kT/C noise considerations reduced power dissipation by $2.5\times$ as compared to the use of identical amplifiers in all stages of the cascade. A capacitive level shift between the stages of a two-stage amplifier reduced power dissipation as compared to conventional designs by allowing an all-NMOS signal path and reduced number of current legs. The modulator with performance summarized in Table I achieved 77 dB of dynamic range and dissipated 81 mW from a 3.3 V supply.

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