On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's

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***Abstract*— This paper presents a patterned ground shield inserted between an on-chip spiral inductor and silicon substrate. The patterned ground shield can be realized in standard silicon technologies without additional processing steps. The impacts of shield resistance and pattern on inductance, parasitic resistances and capacitances, and quality factor are studied extensively. Experimental results show that a polysilicon patterned ground shield achieves the most improvement. At 1–2 GHz, the addition of the shield increases the inductor quality factor up to 33% and reduces the substrate coupling between two adjacent inductors by as much as 25 dB. We also demonstrate that the quality factor of a 2-GHz LC tank can be nearly doubled with a shielded inductor.**

***Index Terms*— Inductor, inductor model, patterned ground shield, quality factor, self-resonance, substrate loss, substrate noise coupling.**

I. Introduction

RECENTLY, interest in on-chip spiral inductors has surged with the growing demand for radio frequency integrated circuits (RF IC's) [1]. For silicon-based RF IC's, the inductor quality factor (Q) degrades at high frequencies due to energy dissipation in the semiconducting substrate [2]. Noise coupling via the substrate at gigahertz frequencies has been reported [3]. As inductors occupy substantial chip area, they can potentially be the source and receptor of detrimental noise coupling. Furthermore, the physical phenomena behind the substrate effects are complicated to characterize. Therefore, decoupling the inductor from the substrate can enhance the overall performance: increase Q, improve isolation, and simplify modeling.

Some approaches have been proposed to address the substrate issues; however, they are accompanied by drawbacks. Ashby *et al.* [4] suggested the use of high-resistivity (150–200 Ω·cm) silicon substrate to mimic the low-loss semi-insulating GaAs substrate, but this is an uncommon option for current silicon technologies. Chang *et al.* [5] demonstrated that etching a pit in the silicon substrate under the inductors can remove the substrate effects. However, the etch adds extra processing cost, and is not readily available. Moreover, it raises reliability concerns such as packaging yield and long-term mechanical stability. For low-cost integration of inductors, the solution to substrate problems should avoid increasing process complexity.

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In this paper, we present a patterned ground shield, which is compatible with standard silicon technologies, to reduce the unwanted substrate effects. To provide some background, Section II presents a discussion on the fundamental definitions of an inductor Q and an LC tank Q. Next, a physical model for spiral inductors on silicon is described. The magnetic energy storage and loss mechanisms in an on-chip inductor are discussed. Based on this insight, it is shown that energy loss can be reduced by shielding the electric field of the inductor from the silicon substrate. Then, the drawbacks of a solid ground shield are analyzed. This leads to the design of a patterned ground shield. Design guidelines for parameters such as shield pattern and resistance are given. In Section III, experiment design, on-wafer testing technique, and parasitic extraction procedure are presented. Experimental results are then reported to study the effects of shield resistance and pattern on inductance, parasitic resistances and capacitances, and inductor Q. Next, the improvement in Q of a 2-GHz LC tank using a shielded inductor is illustrated. A study of the noise coupling between two adjacent inductors and the efficiency of the ground shield for isolation are also presented. Lastly, Section IV gives some conclusions.

II. Design Considerations

A. Definitions of Quality Factor

The quality of an inductor is measured by its Q which is defined as [6]

$$Q = 2\pi \cdot \frac{\text{energy stored}}{\text{energy loss in one oscillation cycle}}. \qquad (1)$$

Interestingly, (1) also defines the Q of an LC tank. The definition in (1) is fundamental in the sense that it does not specify what stores or dissipates the energy. The subtle distinction between an inductor Q and an LC tank Q lies in the intended form of energy storage. For an inductor, only the energy stored in the magnetic field is of interest. Any energy stored in the inductor's electric field, because of some inevitable parasitic capacitances in a real inductor, is counterproductive. Hence, Q is proportional to the net magnetic energy stored, which is equal to the *difference* between the peak magnetic and electric energies. An inductor is at self-resonance when the peak magnetic and electric energies are equal. Therefore, Q vanishes to zero at the self-resonant frequency. Above the self-resonant frequency, no net magnetic energy is available from an inductor to any external circuit. In contrast, for an LC tank, the energy stored is the

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sum of the average magnetic and electric energies. Since the energy stored in a (lossless) LC tank is constant and oscillates between magnetic and electric forms, it is also equal to the peak magnetic energy, or the peak electric energy. The rate of the oscillation process is the tank's resonant frequency at which Q is defined. For a lossless LC tank, Q is infinite.

To illustrate the distinction between these two cases, consider a simple parallel RLC circuit first as an inductor model, then as an LC tank model. The expressions for the energies and the resonant frequency ω_0 are:

$$E_{\text{peak magnetic}} = \frac{V_0^2}{2\omega^2 L} \tag{2}$$

$$E_{\text{peak electric}} = \frac{V_0^2 C}{2} \tag{3}$$

$$E_{\text{loss in one oscillation cycle}} = \frac{2\pi}{\omega} \cdot \frac{V_0^2}{2R} \tag{4}$$

$$E_{\text{average magnetic}} = \frac{V_0^2}{4\omega^2 L} \tag{5}$$

$$E_{\text{average electric}} = \frac{V_0^2 C}{4} \tag{6}$$

and

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{7}$$

where V_0 denotes the peak voltage across the circuit terminals. In terms of an inductor model, C is regarded as the parasitic capacitance of the inductor. The inductor Q is shown in (8), found at the bottom of the page, which equals zero at $\omega = \omega_0$, and is less than zero beyond ω_0. It is worthwhile to mention that the result in (8) can also be obtained using the ratio of the imaginary to the real part of the circuit impedance. The circuit impedance is inductive below ω_0 and capacitive above ω_0. In terms of an LC tank model, C is regarded as the tank capacitance of the LC tank. The tank Q is defined at ω_0 and is expressed in (9), shown at the bottom of the page. The same result can also be derived using a more well-known relationship: the ratio of the resonant frequency to the −3-dB bandwidth.

Both Q definitions discussed are of importance, and their applications are determined by the intended function in a circuit. When evaluating the quality of an on-chip inductor as a single element, the definition in (8) is more appropriate. In Section III, when LC tanks are studied, the definition in (9) will be used.

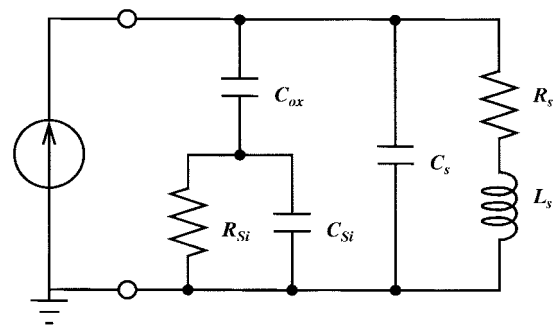


Fig. 1. Lumped physical model of a spiral inductor on silicon.

B. Understanding of Substrate Effects

The physical model of an inductor on silicon with one port and the substrate grounded is shown in Fig. 1 [2]. An on-chip inductor is physically a three-port element including the substrate. The one-port connection shown in Fig. 1 avoids unnecessary complexity in the following analysis and at the same time preserves the inductor characteristics. In the model, the series branch consists of L_s, R_s, and C_s. L_s represents the spiral inductance which can be computed using the Greenhouse method [7]. R_s is the metal series resistance whose behavior at radio frequency (RF) is governed by the eddy current effect. This resistance symbolizes the energy losses due to the skin effect in the spiral interconnect structure, as well as the induced eddy current in any conductive media close to the inductor. The series feedforward capacitance C_s accounts for the capacitance due to the overlaps between the spiral and the center-tap underpass [8]. The effect of the interturn fringing capacitance is usually small because the adjacent turns are almost equipotential and therefore it is neglected in our model. The overlap capacitance is more significant because of the relatively large potential difference between the spiral and the center-tap underpass. The parasitics in the shunt branch are modeled by C_{ox}, C_{Si}, and R_{Si}. C_{ox} represents the oxide capacitance between the spiral and the substrate. The silicon substrate capacitance and resistance are modeled by C_{Si} and

$$Q_{\text{inductor}} = 2\pi \cdot \frac{\text{peak magnetic energy} - \text{peak electric energy}}{\text{energy loss in one oscillation cycle}} = \frac{R}{\omega L} \cdot \left[1 - \left(\frac{\omega}{\omega_0}\right)^2\right] \tag{8}$$

$$\begin{aligned} Q_{\text{tank}} &= 2\pi \cdot \left.\frac{\text{average magnetic energy + average electric energy}}{\text{energy loss in one oscillation cycle}}\right|_{\omega=\omega_0} \\ &= 2\pi \cdot \left.\frac{\text{peak magnetic energy}}{\text{energy loss in one oscillation cycle}}\right|_{\omega=\omega_0} = \frac{R}{\omega_0 L} \\ &= 2\pi \cdot \left.\frac{\text{peak electric energy}}{\text{energy loss in one oscillation cycle}}\right|_{\omega=\omega_0} = \omega_0 RC \\ &= \frac{R}{\sqrt{L/C}} \end{aligned} \tag{9}$$

$R_{\rm Si}$, respectively, [9], [10]. The ohmic loss in $R_{\rm Si}$ signifies the energy dissipation in the silicon substrate.

In Fig. 2, the combined impedance of $C_{\rm ox}$, $C_{\rm Si}$, and $R_{\rm Si}$ is substituted by R_p and C_p, which are therefore frequency dependent, while L_s, R_s, and C_s remain unchanged as in Fig. 1. The reason for this substitution is twofold: it facilitates the analysis of R_p's effect on Q and the extraction of the shunt parasitics from measured S parameters (see Fig. 8). In terms of the circuit elements in Fig. 2, the energies can be expressed as

$$E_{\text{peak magnetic}} = \frac{V_0^2 L_s}{2 \cdot [(\omega L_s)^2 + R_s^2]} \tag{10}$$

$$E_{\text{peak electric}} = \frac{V_0^2 (C_s + C_p)}{2} \tag{11}$$

and

$$E_{\text{loss in one oscillation cycle}} = \frac{2\pi}{\omega} \cdot \frac{V_0^2}{2} \cdot \left[\frac{1}{R_p} + \frac{R_s}{(\omega L_s)^2 + R_s^2}\right] \tag{12}$$

where

$$R_p = \frac{1}{\omega^2 C_{\rm ox}^2 R_{\rm Si}} + \frac{R_{\rm Si}(C_{\rm ox} + C_{\rm Si})^2}{C_{\rm ox}^2} \tag{13}$$

$$C_p = C_{\rm ox} \cdot \frac{1 + \omega^2 (C_{\rm ox} + C_{\rm Si}) C_{\rm Si} R_{\rm Si}^2}{1 + \omega^2 (C_{\rm ox} + C_{\rm Si})^2 R_{\rm Si}^2} \tag{14}$$

and V_0 denotes the peak voltage across the inductor terminals. The inductor Q can be derived by substituting (10)–(12) into (8):

$$\begin{aligned} Q &= \frac{\omega L_s}{R_s} \cdot \frac{R_p}{R_p + [(\omega L_s/R_s)^2 + 1] R_s} \\ &\quad \cdot \left[1 - \frac{R_s^2 (C_s + C_p)}{L_s} - \omega^2 L_s (C_s + C_p)\right] \\ &= \frac{\omega L_s}{R_s} \cdot \text{substrate loss factor} \cdot \text{self-resonance factor} \end{aligned} \tag{15}$$

where $\omega L_s/R_s$ accounts for the magnetic energy stored and the ohmic loss in the series resistance. The second term in (15) is the substrate loss factor representing the energy dissipated in the semiconducting silicon substrate. The last term is the self-resonance factor describing the reduction in Q due to the increase in the peak electric energy with frequency and the vanishing of Q at the self-resonant frequency. Hence, the self-resonant frequency can be solved by equating the last term in (15) to zero.

Fig. 3 shows the measured frequency behavior of Q and the degradation factors for a typical on-chip inductor. At 1 GHz, the measured element set $\{L_s, R_s, C_s, C_p, R_p\}$ is equal to $\{$8.2 nH, 13.4 Ω, 26 fF, 102.7 fF, 1.7 kΩ$\}$. A detailed comparison between modeled and measured values for a wide variety of spiral inductors can be found in [2]. In Fig. 3(a) at low frequencies, Q is well described by $\omega L_s/R_s$ when both degradation factors have values close to unity. As frequency increases, the degradation factors decrease from unity, as shown in Fig. 3(b). This illustrates that the reduction of Q at high frequencies is a combined effect of substrate loss and self-resonance. In particular, the substrate loss alone causes 10–30% reduction from $\omega L_s/R_s$ at 1–2 GHz. Physically, the substrate loss stems from the penetration of electric field into the silicon. As the potential drop in the semiconductor, i.e., across $R_{\rm Si}$ in Fig. 1, increases with frequency, the energy dissipation in the substrate becomes more severe.

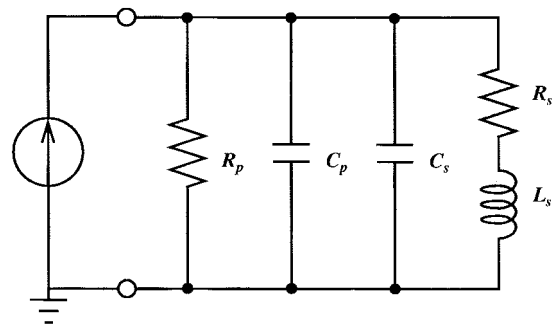


Fig. 2. Equivalent model with the combined impedance of $C_{\rm ox}$, $C_{\rm Si}$, and $R_{\rm Si}$ in Fig. 1 substituted by R_p and C_p.

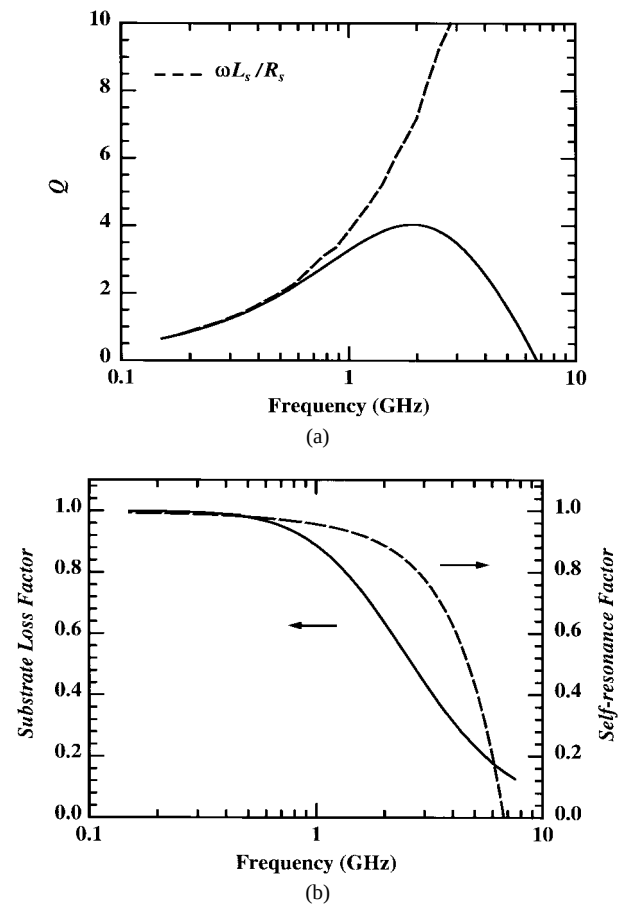


Fig. 3. Typical frequency behavior of (a) Q and (b) the degradation factors.

From (15), it can be seen that the substrate loss factor approaches unity as R_p approaches infinity. In other words, by increasing R_p to infinity, we can reduce the substrate loss. From (13), it can be shown that R_p approaches infinity as $R_{\rm Si}$ goes to zero or infinity. This is an important observation because it implies that Q can be improved by making the silicon substrate either a short or an open, thereby eliminating

energy dissipation. Using high-resistivity silicon or etching away the silicon is equivalent to making the substrate an open circuit. In this paper, we explored the option of shorting the substrate to eliminate the loss. The approach is to insert a ground plane to block the inductor electric field from entering the silicon.

C. Drawback of Solid Ground Shields

The effectiveness of solid ground shield for reducing silicon parasitics has been reported [11], [12]. Rofougaran *et al.* used metal one as ground shields for metal-two bond pads to improve the input impedance matching of a low-noise amplifier fabricated in a CMOS process. Tsukahara *et al.* used a similar technique with a polysilicon layer as ground shields for metal–insulator–metal capacitors in a bipolar process. The polysilicon ground shields eliminated the silicon parasitics associated with the bottom plate of the capacitors. At 1 GHz, 30-dB reduction in substrate crosstalk was reported.

A solid conductive ground shield can be inserted between the inductor and the substrate to provide a short to ground. This is equivalent to placing a small resistance in parallel with $C_{\rm Si}$ and $R_{\rm Si}$ of the circuit model in Fig. 1. Physically, the electric field of the inductor is terminated before reaching the silicon substrate. One of the serious drawbacks with this approach is that the solid ground shield also disturbs the inductor's magnetic field. According to Lenz's law, image current, also known as loop current, will be induced in the solid ground shield by the magnetic field of the spiral inductor. The image current in the solid ground shield will flow in a direction opposite to that of the current in the spiral. The resulting negative mutual coupling between the currents reduces the magnetic field, and thus the overall inductance.

Using an equivalent circuit model, one can treat the inductor with the ground shield as a transformer. In Fig. 4, the primary and secondary circuits represent the spiral and the solid ground shield, respectively. The induced current flowing in the secondary inductor will impose a counter electromotive force on the primary inductor. This effect can be accounted for by adding a reflected impedance $\boldsymbol{Z}_r$ in series with the impedance of the primary circuit [13]. $\boldsymbol{Z}_r$ can be expressed in terms of the mutual inductance M and the series impedance of the secondary circuit as

$$\boldsymbol{Z}_r = \frac{(\omega M)^2}{R_2 + j\omega L_2}. \tag{16}$$

Therefore, the input impedance seen by the source is

$$\boldsymbol{Z}_{\rm in} = R_1 + j\omega L_1 + \boldsymbol{Z}_r. \tag{17}$$

Note that the imaginary part of $\boldsymbol{Z}_r$ is negative, which signifies the reduction in the overall inductance. Also of importance is the increase in the overall resistance due to the real part of $\boldsymbol{Z}_r$, which denotes the additional energy loss due to the ground shield conductor. From (16) and (17), one can easily show that the effect of $\boldsymbol{Z}_r$ on $\boldsymbol{Z}_{\rm in}$ diminishes as R_2 approaches infinity. An infinite R_2 can be achieved by inserting features in the ground shield that oppose the flow of the image current.

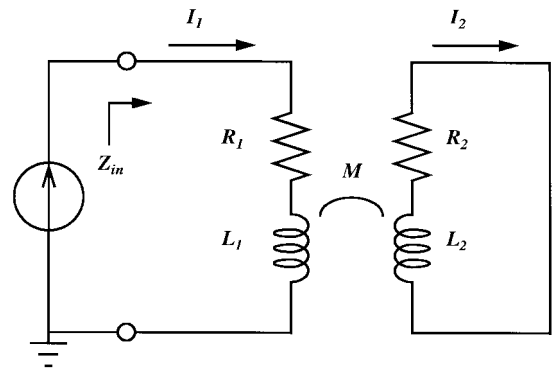


Fig. 4. Circuit model for illustrating the effects of negative mutual coupling between a spiral inductor and a solid ground shield.

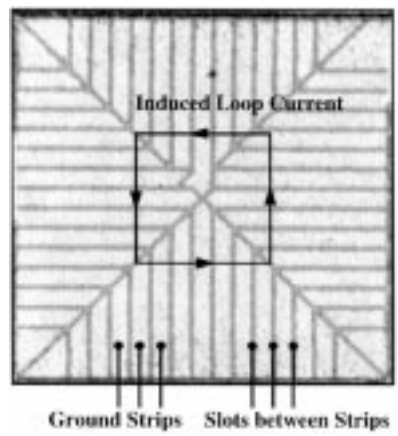


Fig. 5. Close-up photo of the patterned ground shield.

D. Design of Patterned Ground Shields

To increase the resistance to the image current, the ground shield is patterned with slots orthogonal to the spiral as illustrated in Fig. 5. The slots act as an open circuit to cut off the path of the induced loop current. The slots should be sufficiently narrow such that the vertical electric field cannot leak through the patterned ground shield into the underlying silicon substrate. With the slots etched away, the ground strips serve as the termination for the electric field. The ground strips are merged together around the four outer edges of the spiral. The separation between the merged area and the edges is not critical. However, it is crucial that the merged area does not form a closed ring around the spiral since it can potentially support unwanted loop current. The shield should be strapped with the top layer metal to provide a low-impedance path to ground. The general rule is to prevent negative mutual coupling while minimizing the impedance to ground.

The shield resistance is another critical design parameter. The purpose of the patterned ground shield is to provide a good short to ground for the electric field. Since the finite shield resistance contributes to energy loss of the inductor, it must be kept minimal. Specifically, by keeping the shield resistance small compared to the reactance of the oxide capacitance, the voltage drop that can develop across the shield resistance is small. As a result, the energy loss due to the shield resistance is insignificant compared to other losses. A typical

on-chip spiral inductor has parasitic oxide capacitance between 0.25–1 pF depending on the size and the oxide thickness. The corresponding reactance due to the oxide capacitance at 1–2 GHz is on the order of 100 Ω and, hence, shield resistance of a few ohms is sufficiently small not to cause any noticeable loss.

As the magnetic field passes through the patterned ground shield, its intensity is weakened due to the skin effect [14]. This directly causes a decrease in the inductance since the magnetic flux is lessened in the space occupied by the ground shield layer. To avoid this attenuation, the shield must be significantly thinner than the skin depth at the frequency of interest. For example, the skin depth of aluminum at 2 GHz is approximately 2 μm, which is only 3–4 times the typical metal-one thickness. This implies that using a typical metal-one layer for the shield may result in reduction of the magnetic field intensity and, hence, the inductance.

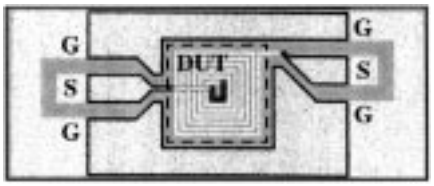
III. Experimental Results

A. Experiment Design

In Fig. 6, the test structures are shown for the inductors studied in this work: (a) no ground shield (NGS); (b) solid ground shield (SGS); and (c) patterned ground shield (PGS). Each spiral is fabricated using 2-μm-thick aluminum with 12 m$\Omega/\square$ sheet resistance. A 1-μm-thick underpass is used to contact the center of the spiral. The spiral and the ground shield are separated by 5.2 μm of oxide. The ground shield is separated from the silicon substrate by 0.4 μm of oxide. The inductors are fabricated on 10–20 $\Omega \cdot$ cm bulk silicon substrates. Each inductor has seven turns, 15-μm line width, and 5-μm line space. The outer dimension of the spirals is 300 μm. The spiral layout is optimized for the unshielded inductor to achieve maximum Q at about 1.5 GHz. The same layout is used for the shielded inductors to demonstrate the general advantage of inserting the PGS beneath an inductor without deliberate optimization. This implies that further improvement for the shielded inductor is attainable with layout optimization accounting for the parasitics of the shield.

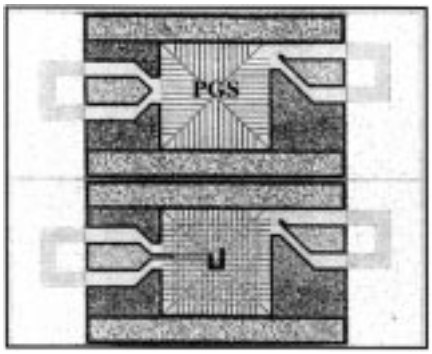
To investigate the effect of shield pattern, ground shields with different slot widths (1.5 and 2.5 μm) and pitches (5 and 20 μm) are fabricated. To study the effect of shield resistance, 0.5-μm aluminum (64 m$\Omega/\square$) and 0.5-μm doped polysilicon (12 $\Omega/\square$) are used to implement the shield. The polysilicon sheet resistance is chosen to be similar to that of MOSFET gates or BJT emitters. In technologies with silicided gate or emitter, the sheet resistance of the polysilicon layer can be as low as a few ohms per square, which is more suitable for our purpose. Nevertheless, the measured results will reveal that the doped polysilicon is conductive enough not to cause any observable loss.

Noise coupling between inductors is also studied. Crosstalk was measured between two adjacent unshielded inductors on substrate with different resistivities. The test structure is shown in Fig. 7. Each inductor has one end grounded, and the metal ground rings surrounding the inductors are not connected. The efficiency of the ground shield for isolation is evaluated using the same test structure with shields inserted underneath the inductors.



(a)

(b)



(c)

Fig. 6. Die photos of ground–signal–ground (GSG) test structure and the inductors: (a) spiral inductor with no ground shield (NGS), (b) solid ground shield (SGS) shown without spiral, and (c) patterned ground shield shown without and with spiral.

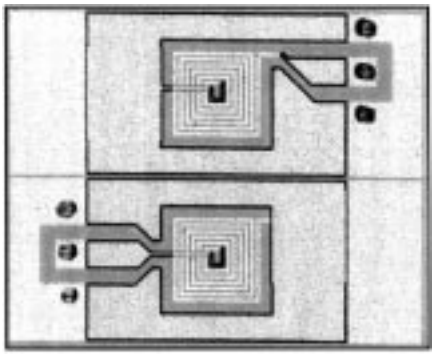


Fig. 7. Two-port test structure for measuring crosstalk via substrate between two adjacent inductors (shown with unshielded inductors).

B. Testing and Extraction Techniques

On-wafer testing was performed with an HP8720B Network Analyzer and Cascade Microtech coplanar ground–signal–ground (GSG) probes. During measurements, the substrate was grounded from the wafer back side through the testing chuck. The shunt parasitics of the test structure were de-embedded using open calibration structures fabricated next to the device under test (DUT). Two-port S parameters

were measured, instead of a one-port parameter, to allow extraction of the inductance and other parasitics without curve fitting. The extraction procedure is summarized in Fig. 8. From the de-embedded S parameters, the complex propagation constant and characteristic impedance are computed. Then, the lumped elements in the series and shunt branches of the inductor model (the model from Fig. 2 in its two-port configuration) are solved using the relationships shown in the bottom block of Fig. 8. To extract L_s, R_s, and C_s from the real and imaginary parts of the measured series impedance, some assumptions about L_s and C_s need to be made. L_s and R_s are subject to skin effect, which governs the magnetic field intensity and current density in the conductor at high frequencies [14]. As frequency increases, the penetration of the magnetic the field into the conductor is attenuated, which causes a reduction in the magnetic flux internal to the conductor. However, L_s does not decrease significantly with increasing frequency because it is predominantly determined by the magnetic flux external to the conductor. Thus, L_s can be approximated as constant with frequency. The skin effect on R_s is much more pronounced because R_s is directly affected by the nonuniform current distribution in the conductor. C_s is considered independent of frequency since it represents the metal-to-metal overlap capacitance between the spiral and the center tap. At low frequencies, the reactance is dominated by ωL_s because ωL_s is much greater than $1/\omega C_s$. C_s is extracted using the low-frequency L_s value and the resonant frequency of the series branch. Then, with C_s held constant, L_s and R_s are solved using the real and imaginary parts of the series impedance at each measurement frequency. In the shunt branch, R_p and C_p can be extracted readily from the real and imaginary parts of the shunt admittance, respectively. The extraction technique described has been confirmed with experimental and published data of inductors having different geometric and process parameters [2].

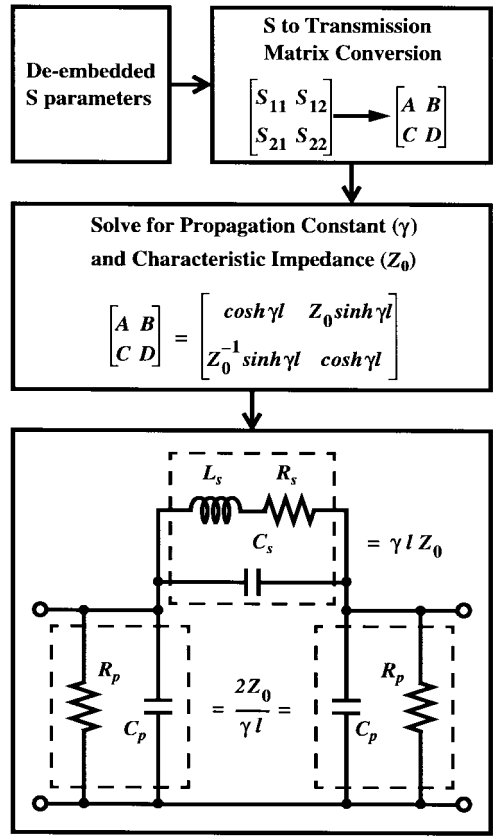


Fig. 8. Parameter extraction procedure for the lumped elements in the inductor model shown in Fig. 2 (l is the overall length of a spiral inductor).

C. Results and Discussion

In Fig. 9(a), measurement results for the effect of aluminum ground shields on L_s are plotted. Two inductors with NGS on 11 and 19 $\Omega \cdot$ cm substrates are included for comparison. The extracted L_s's are about 8 nH: the slight decrease with frequency justifies the assumption that L_s is almost frequency invariant. Furthermore, no noticeable difference in the L_s's is observed for the two cases, confirming that the magnetic fields of the inductors do not interact strongly with the substrates. The extracted C_s's are 18 fF: both inductors have the same C_s since the layout and process parameters are identical except for the substrate resistivity. In the shielded inductors, however, L_s can no longer be assumed as frequency invariant due to the induced loop current and attenuation of the magnetic flux in the shield layer. The extraction of L_s, consequently, is more difficult. In contrast, it is reasonable to expect C_s to remain the same with the introduction of the shield. Therefore, L_s of the shielded inductors are extracted with C_s equal to 18 fF. For the inductor with SGS, the extracted L_s decreases significantly as the frequency increases. This is caused by the negative mutual coupling between the spiral and the SGS, as explained in Section II-C. With the PGS, most of the inductance is recovered, which confirms the effectiveness of the slot pattern for stopping the image current. Close inspection reveals that the inductance for the PGS case is lower than the two NGS cases, and the difference increases with frequency. This suggests that aluminum is too conductive to be optimal as the ground shield layer. In Fig. 9(b), the extracted R_s of the inductors with NGS increases with frequency due to the skin effect of the spiral conductor. The SGS case has a significantly higher R_s due to the image current. On the other hand, the inductor with PGS has the same R_s as the inductors with NGS because there is no image current. For the shunt parasitics shown in Fig. 9(c)–(d), the two NGS cases show a strong frequency dependence. The frequency behaviors of C_p and R_p are governed by $C_{\rm ox}$, $C_{\rm Si}$, and $R_{\rm Si}$. At low frequencies, the electric field terminates at the oxide–Si interface, and C_p is primarily determined by $C_{\rm ox}$. Since almost all electric energy is stored within the oxide layer along the spiral, little conduction current flows in the silicon substrate, and thus R_p is large. As frequency increases, the electric field starts to penetrate into the silicon substrate, which reduces C_p because of the series connection of oxide and silicon substrate capacitances. The roll-off in R_p signifies increasing energy dissipation in the silicon substrate. For the shielded inductors, C_p's are determined by the oxide capacitance between the spiral and the ground shield, which is slightly higher than the unshielded cases because of a thinner oxide. R_p's of the shielded inductors are very large, indicating that there

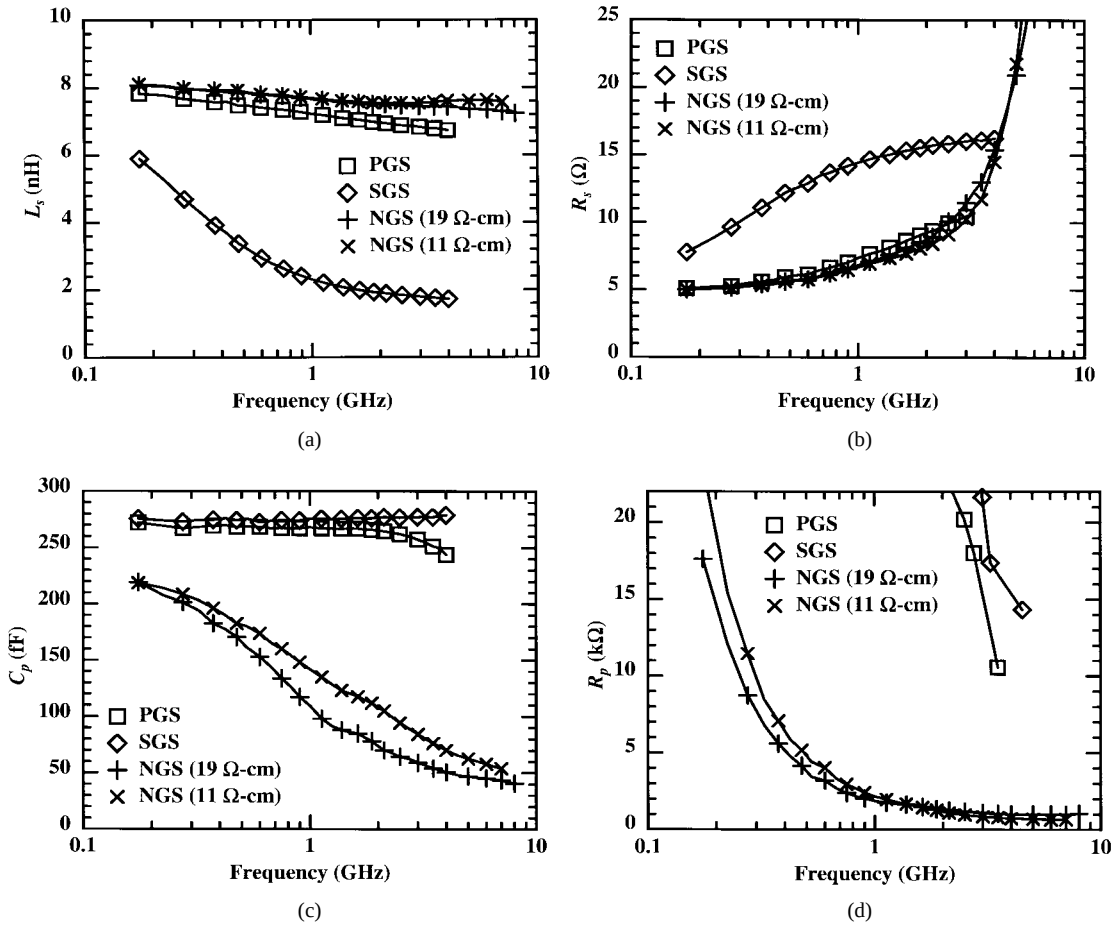


Fig. 9. Effect of aluminum ground shields on: (a) spiral inductance (L_s), (b) series resistance (R_s), (c) parasitic capacitance (C_p), and (d) parasitic resistance (R_p).

is essentially no energy loss in the ground shields. Although lower C_p's for the NGS cases would seem more desirable, they imply the existence of the lossy R_p's. It will be shown that eliminating the substrate loss, i.e., making R_p approach infinity, is more important for improving the inductor Q. That is, the PGS eliminates the lossy frequency-variant capacitance with a slightly larger lossless frequency-invariant one.

In Fig. 10(a)–(d), the measured results for inductors with polysilicon ground shields are plotted against the same unshielded inductors. In the SGS case, the image current starts to build up above 1 GHz. Although it does not lead to noticeable reduction in L_s, it causes R_s to increase more rapidly than the NGS cases. On the other hand, the polysilicon PGS does not deteriorate L_s or R_s, and terminates the inductor's electric field to provide the desired shielding from the substrate. For both aluminum and polysilicon PGS's, the measurement results show no variation for the different slot widths and pitches.

Figs. 11 and 12 show the effects of aluminum and polysilicon ground shields on Q. The inductor with aluminum SGS has the lowest Q because of its lowest L_s and highest R_s. In Fig. 12, the polysilicon SGS yields a Q similar to those of the NGS cases, indicating that it is resistive enough to prevent most of the image current from flowing. Finally, the polysilicon PGS, which combines the appropriate sheet resistance and pattern, yields the most improvement in Q (ranges from 10 to 33%) between 1–2 GHz. Note that the inclusion of the ground shields increases C_p, which causes a fast roll-off in Q above the peak-Q frequency and a reduction in the self-resonant frequency. Comparison between the inductor parameters for the NGS (11 $\Omega \cdot$ cm) and polysilicon PGS cases is shown in Table I. The results at 2 GHz are compared to emphasize the relative importance of the degradation mechanisms near the peak-Q frequency. In particular, the unshielded inductor suffers greatly from substrate loss with nearly 50% reduction from $\omega L_s/R_s$. Although the shielded inductor has a lower self-resonance factor, it is almost free of substrate loss. The overall effect is a 33% improvement in Q at 2 GHz with the addition of polysilicon PGS. Further optimization of the shielded inductor layout to decrease the self-resonance factor and to increase the Q is possible.

In RF circuits, an inductor is often used to form an LC tank. Fig. 13 plots the frequency behavior of the tank impedance for two 2-GHz LC tanks to demonstrate the impact of the 8-nH inductor with polysilicon PGS on the tank quality factor, Q_{tank}. The tuning capacitances for the shielded and unshielded cases are 0.5 and 0.7 pF, respectively, to account for the difference in the inductors' parasitic capacitance. As mentioned in Section II-A, Q_{tank} can be determined by ratio of the resonant frequency, at which the tank impedance is

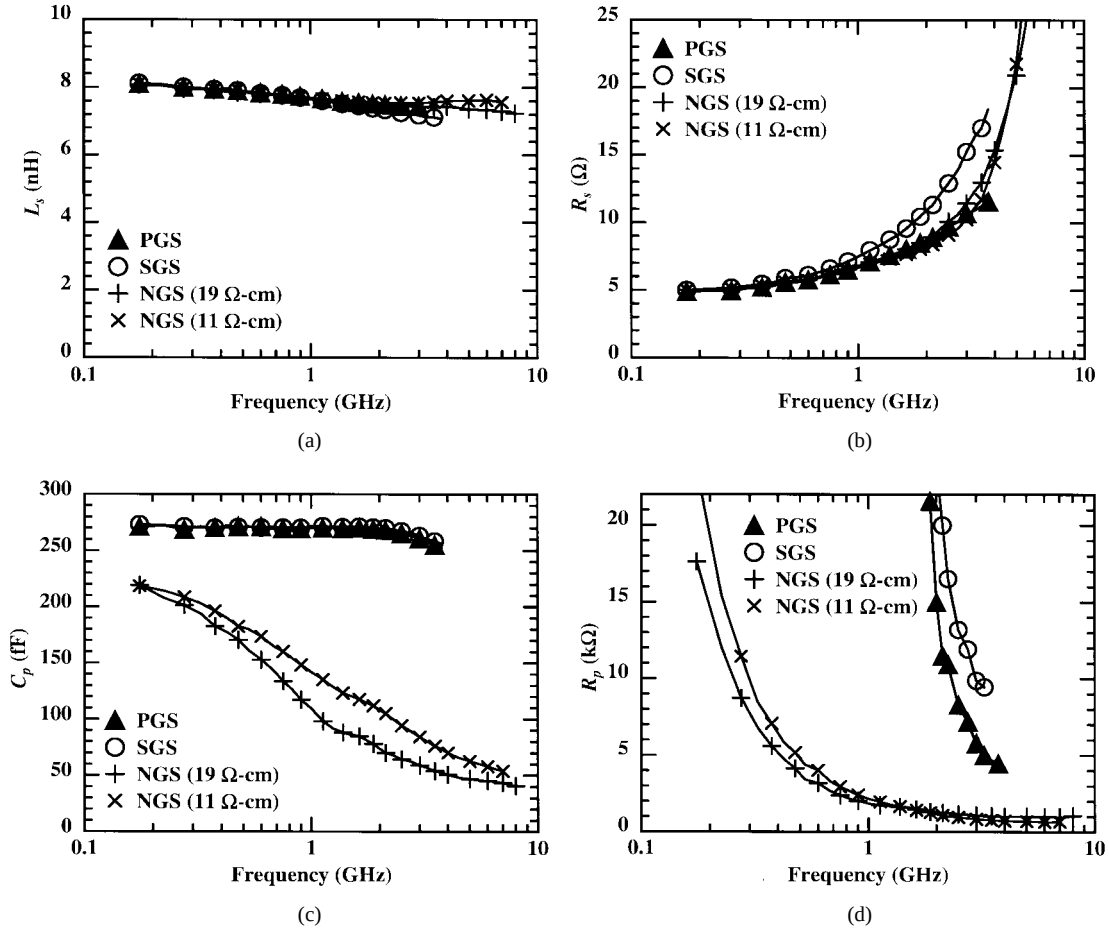


Fig. 10. Effect of polysilicon ground shields on: (a) spiral inductance (L_s), (b) series resistance (R_s), (c) parasitic capacitance (C_p), and (d) parasitic resistance (R_p).

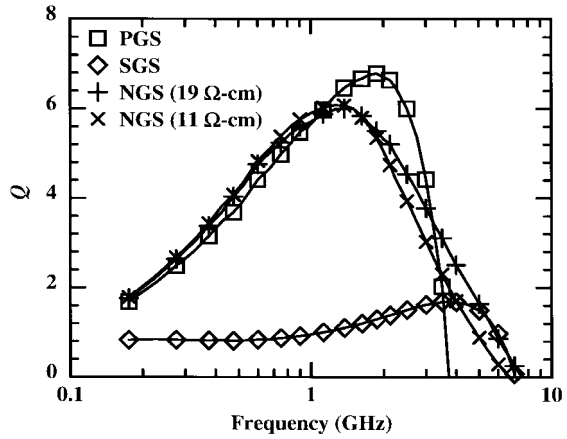


Fig. 11. Effect of aluminum ground shields on Q.

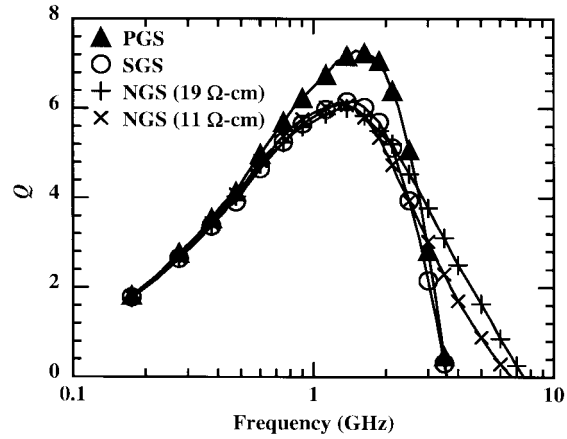


Fig. 12. Effect of polysilicon ground shields on Q.

maximum, to the −3-dB bandwidth. Even though the parasitic capacitances of both inductors are incorporated as part of the tank capacitance, the tank with the unshielded inductor suffers from a lossy R_p. As a result, Q_{tank} is improved from 6.0 for the tank with the unshielded inductor to 10.2 for the one with the shielded inductor. It is important to note that Q_{tank} exceeds the inductor Q for both inductors at 2 GHz (see Table I). This can be attributed to the fact that the reduction of the inductors' Q caused by their parasitic capacitances becomes irrelevant as the capacitances are "absorbed" by the LC tanks.

Substrate noise coupling between two adjacent inductors is measured by the magnitude of the transmission coefficient $|S_{21}|$. Fig. 14 shows that for the unshielded inductors, the one on a more conductive substrate (11 $\Omega \cdot$ cm) has stronger coupling due to the higher substrate admittance. The peaks in $|S_{21}|$ for the NGS cases correspond to the onset of significant electric field penetration into the silicon substrate, and hence more coupling. In contrast, the inductors shielded by the polysilicon PGS's show significantly better isolation, up to 25 dB, at gigahertz frequencies. It should be noted that, like any

TABLE I
COMPARISON OF MEASURED INDUCTOR PARAMETERS FOR THE NGS (11 Ω · cm) AND POLYSILICON PGS CASES AT 2 GHz

	NGS	Polysilicon PGS
L_s (nH)	7.5	7.4
R_s (Ω)	8.2	8.5
C_s (fF)	18.0	18.0
C_p (fF)	108.1	268.2
R_p (kΩ)	1.2	15.0
$\omega L_s/R_s$	11.5	10.9
Substrate Loss Factor	0.52	0.94
Self-resonance factor	0.85	0.66
Q	5.08	6.76
Self-resonant Frequency (GHz)	6.8	3.6

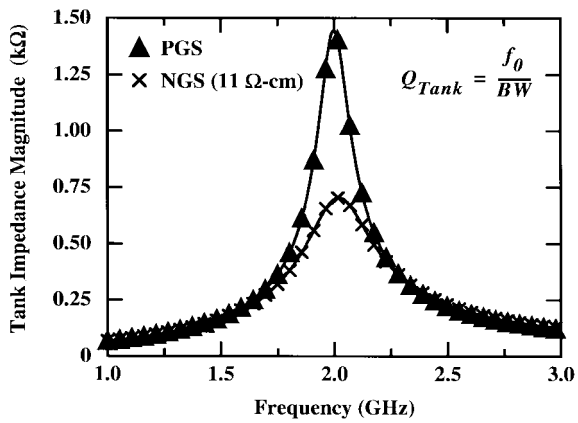


Fig. 13. Effect of polysilicon patterned ground shield on Q of a 2-GHz LC tank.

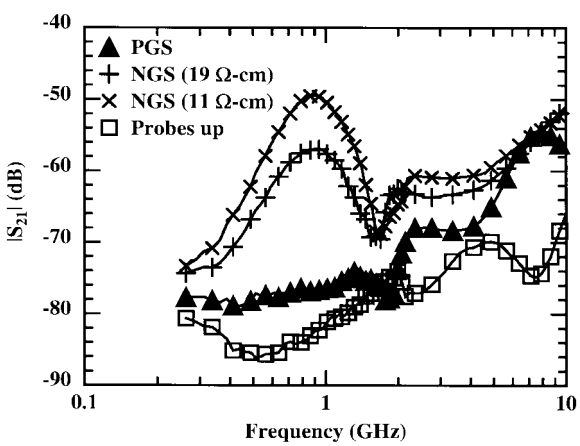


Fig. 14. Effect of polysilicon patterned ground shield on substrate coupling between two adjacent inductors.

other isolation structure, such as a guard ring, the efficiency of the PGS is highly dependent on the integrity of the ground connection. Designers often need to make a tradeoff between the desired isolation level and the chip area that is required for a low-impedance ground.

IV. CONCLUSIONS

On-chip spiral inductors with patterned ground shields are presented. The parasitic effects of an inductor on silicon are analyzed with the aid of a physical model. A patterned ground shield is devised to eliminate the silicon parasitics of the on-chip spiral inductor. The effects of shield resistance and pattern are studied both theoretically and experimentally. Measurement results confirmed that a patterned ground shield improves the Q and isolation of an on-chip inductor. Furthermore, with the addition of the ground shield, an inductor's characteristics are less dependent on substrate variation, and hence are easier to model. The implementation of the ground shield is compatible with standard silicon IC technology. The experimental results presented in this work are exclusively based on lightly doped (10–20 Ω · cm) substrates. Given the increasing interest in CMOS RF IC's, investigation on the effects of heavily doped (10–20 mΩ·cm) substrates on shielded inductors are underway, and will be reported in the near future.

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