SOLDER JOINTS IN ELECTRONICS:

DESIGN FOR RELIABILITY

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ABSTRACT

The emerging new technologies provide ever more challenges to assure the reliability of electronic products. The ever increasing demands in electronic products for higher performance, lower cost, less space (weight) is leading to ever denser interconnection needs.

This makes solder joint reliability an even more important issue with the advent of new surface mount packages and the use of surface mounted electronics in such hostile environments as the automobile and space. The new packages are characterized by larger sizes, finer pitches, and/or problematic materials which require an up-front Design for Reliability (DfR) to meet reliability requirements. The hostile environments can include thermal excursions over temperature ranges in which multiple interactive damage mechanisms are operative.

The reliability of electronic assemblies requires a definitive design effort that has to be carried out concurrently with the other design functions during the developmental phase of the product. There exists a misconception in the industry, that quality manufacturing is all that is required to assure the reliability of an electronic assembly.

While of course, consistent high quality manufacturing and all that this implies is a necessary prerequisite to assure the reliability of the product, only a DfR-procedure can assure that the design manufactured to good quality will be reliable in its intended application.

Explicit DfR-procedures need to be employed to account and compensate, at least in part, for the prevalent damage mechanisms. This needs to be complemented with Design for Manufacturability (DfM) which widens the process windows and takes into account the manufacturing capabilities. These demands put an increasing burden on the designers who will require a heightened technical understanding of the underlying issues and more sophisticated design tools.

It is for this reason that IPC-D-279, *Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies*, has been developed. The Design for Reliability (DfR) for solder attachments in electronic interconnections will be the emphasis of this paper.

1. INTRODUCTION

The reliability of electronic assemblies requires a definitive design effort that has to be carried out concurrently with the other design functions during the developmental phase of the product. There exists a misconception in the industry, that quality manufacturing is all that is required to assure the reliability of an electronic assembly.

While of course, consistent high quality manufacturing and all that this implies in terms of Design for Manufacturability (DfM), Design for Assembly (DfA), Design for Testability (DfT), etc. is a necessary prerequisite to assure the reliability of the product, only a Design for Reliability (DfR) can assure that the design manufactured to good quality will be reliable in its intended application.

Thus, adherence to quality standards is necessary but not sufficient. For example, solder joint quality in the U.S. is generally measured against criteria in both IPC-A-620, *Acceptability of Electronic Assemblies with Surface Mount Technologies,* for overall workmanship and ANSI/J-STD-001, *Requirements for Soldered Electrical and Electronic Assemblies*. However, meeting these criteria does not assure reliable solder connections, only quality solder connections.

To clarify the difference between the two requires an explanation and a definition of reliability. Reliability is defined in IPC-SM-785, *Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments*, by:

> Reliability is the ability of a product to function under given conditions and for a specified period of time without exceeding acceptable failure levels.

In the short term, reliability is threatened by infant mortality failures due to insufficient product quality; these infant mortalities caused by defects can be eliminated prior to shipping by the use of appropriate screening procedures. Long term failures are the result of premature wear-out damage caused by inadequate designs of the assembly.

It is for this reason that IPC-D-279, *Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies*, has been

developed.

2. DAMAGE MECHANISMS AND FAILURE OF SOLDER ATTACHMENTS

The reliability of electronic assemblies depends on the reliability of their individual elements and the reliability of the mechanical thermal, and electrical interfaces (or attachments) between these elements. One of these interface types, surface mount solder attachment, is unique since the solder joints not only provide the electrical interconnections, but are also the sole mechanical attachment of the electronic components to the PWB and often serve critical heat transfer functions as well.

A solder joint in isolation is neither reliable nor unreliable; it becomes so only in the context of the electronic components that are connected via the solder joints to the PWB. The characteristics of these three elements component, substrate, and solder joint together with the use conditions, the design life, and the acceptable failure probability for the electronic assembly determine the reliability of the surface mount solder attachment.

2.1 Solder Joints and Attachment Types

Solder joints are anything but a homogeneous structure. A solder joint consists of a number of quite different materials, many of which are only superficially characterized. A solder joint consists of (1) the base metal at the PWB, (2) one or more intermetallic compounds (IMC) solid solutions of a solder constituent typically tin (Sn) with the PWB base metal, (3) a layer from which the solder constituent forming the PWB-side IMC(s) has been depleted, (4) the solder grain structure, consisting of at least two phases containing different proportions of the solder constituents as well as any deliberate or inadvertent contaminations, (5) a layer from which the solder constituent forming the component-side IMC(s) has been depleted, (6) one or more IMC layers of a solder constituent with the component base metal, and (7) the base metal at the component.

The grain structure of solder is inherently unstable. The grains will grow in size over time as the grain structure reduces the internal energy of a fine-grained structure. This grain growth process is enhanced by elevated temperatures as well as strain energy input during cyclic loading. The grain growth process is thus an indication of the accumulating fatigue damage. At the grain boundaries contaminants like lead oxides are concentrated; as the grains grow these contaminants are further concentrated at the grain boundaries, weakening these boundaries. After the consumption of ~25% of the fatigue life micro-voids can be found at the grain boundary intersections; these micro-voids grow into micro-cracks after ~40% of the fatigue life; these micro-cracks grow and coalesce into macro-cracks leading to total fracture as is schematically shown in Figure 1.

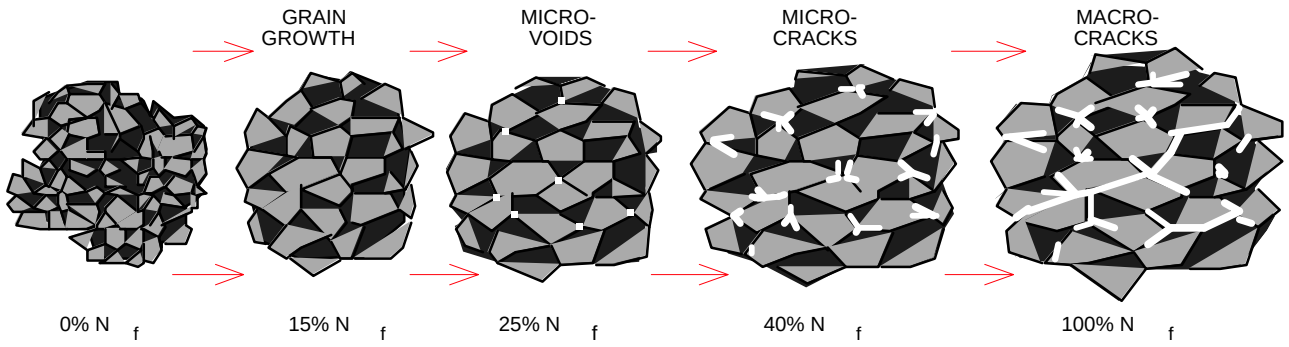

Figure 1: Depiction of the Effects of the Accumulating Fatigue Damage in Solder Joint Structure [1].

Surface mount solder attachments exist in a wide variety of designs. The major categories are leadless and leaded solder attachments. Among the leadless solder joints a differentiation has to be made between those without fillets, e.g., Flip-Chip C4 (Controlled Collapse Chip Connection) solder joints, BGAs with C5 (Controlled Collapse Chip Carrier Connection) solder attachments, BGAs with high-temperature solder (e.g., 10Sn/90Pb) balls, and CGAs with high-temperature solder columns; and solder joints with fillets, e.g., chip components, Metal Electrode Face components (MELFs), and castellated leadless chip carriers. The leaded solder attachments differ primarily in terms of their compliancy and can be roughly categorized into components with super-compliant leads {lead stiffness K_D<~5 N/mm (~30 lb/in), compliant leads ~5 N/mm<K_D<~90 N/mm, and non-compliant leads K_D>~90 N/mm (~500 lb/in)}.
The different surface mount solder attachment types can have significantly different failure modes. Solder joints with essentially uniform load distributions, e.g., Flip-Chip, BGA, CGA, show behavior as illustrated in Figure 1. Solder joints with non-uniform load distributions, e.g., those on chips components, MELFs, leadless chip carriers, and all leaded solder joints, show localized damage concentrations with the damage shown in Figure 1 preceding an advancing macro-crack.

The solder joints frequently connect materials of highly disparate properties, causing global thermal expansion mismatches [1,2,3,4,5,6], and are made of a material, solder, that itself has often properties significantly different than the bonding structure materials, causing local thermal expansion mismatches [4, 7].

The severity of these thermal expansion mismatches, and thus the severity of the reliability threat, depends on the design parameters of the assembly and the operational use environment. In Table I guidelines as to the possible use environments

for nine of the more common electronic applications are illustrated [8, 9]. However, it needs to be emphasized, that the information in Table I should serve only as a general guideline; for some use categories the description of the expected use environment can be rather more complex [9].

Table I. Realistic Representative Use Environments, Service Lives, and Acceptable Failure Probabilities for Surface Mounted Electronics by Use Categories [10].

USE CATEGORY		REALISTIC USE ENVIRONMENTS						Accept.
		Tmin °C	*Tmax* °C	ΔT_{max} (1) °C	t_D hrs	Cycles/ year	Years of Service	Failure Risk, %
1	CONSUMER	0	+60	35	12	365	1-3	~1
2	COMPUTERS	+15	+60	20	2	1460	~5	~0.1
3	TELECOMM	-40	+85	35	12	365	7-20	~0.01
4	COMMERCIAL AIRCRAFT	-55	+95	20	12	365	~20	~0.001
5	INDUSTRIAL & AUTOMOTIVE -PASSENGER COMPARTMENT	-55	+95	20 &40 &60 &80	12 12 12 12	185 100 60 20	~10	~0.1
6	MILITARY GROUND & SHIP	-55	+95	40 &60	12 12	100 265	~5	~0.1
7	SPACE leo geo	-40	+85	35	1 12	8760 365	5-20	~0.001
8	MILITARY AVIONICS a b c	-55	+95	40 60 80	2 2 2	365 365 365	~10	~0.01
	Maintenance			&20	1	365		
9	AUTOMOTIVE -UNDER HOOD	-55	+125	60 &100 &140	1 1 2	1000 300 40	~5	~0.1

& = in addition

(1) ΔT represents the maximum temperature swing, but does not include power dissipation effects for components; for reliability estimations the actual local temperature swings for components and substrate, including power dissipation should be used.

2.2 Global Expansion Mismatch

The global expansion mismatches result from differential thermal expansions of an electronic component or connector and the PWB to which it is attached via the surface mount solder joints. These thermal expansion differences result from differences in the coeficients of thermal expansion (CTEs) and thermal gradients as the result of thermal energy being dissipated within active components.

Global CTE-mismatches typically range from $\Delta\alpha$~2 ppm/°C (1 ppm=1x10^{-6}) for CTE-tailored high reliability assemblies to ~14 ppm/°C for ceramic components on FR-4 PWBs or plastic components on ceramic substrates (C-MCM). CTE-mismatches of $\Delta\alpha$<2 ppm/°C are not achievable in reality as a consequence of the variability of the CTE values of the materials involved on both components and PWBs. Global thermal expansion mismatches typically are the largest, since all three parameters determining the thermal expansion mismatch the CTE-mismatch, $\Delta\alpha$, the temperature swing, ΔT, and the acting distance, L_D can be large.

This global expansion mismatch will cyclically stress, and thus fatigue, the solder joints. The cyclically cumulative fatigue damage will ultimately cause the failure of one of the solder joints, typically a corner joint, of the component causing functional electrical failure that is initially intermittent.

2.3 Local Expansion Mismatch

The local expansion mismatch results from differential thermal expansions of the solder and the base material of the electronic component or PWB to which it is soldered. These thermal expansion differences result from differences in the CTE of the solder and those of the base materials together with thermal excursions [4, 7].

Local CTE-mismatches typically range from Δa~7 ppm/°C with copper to ~18 ppm/°C with ceramic and ~20 ppm/°C with Alloy 42 and Kovar . Local thermal expansion mismatches typically are smaller than the global expansion mismatches, since the acting distance, the maximum wetted area dimension, is much smaller in the order of hundreds of μm (tens of mils).

2.4 Internal Expansion Mismatch

An internal CTE-mismatch of ~6 ppm/°C results from the different CTEs of the Sn-rich and Pb-rich phases of the solder. Internal thermal expansion mismatches typically are the smallest, since the acting distance, the size of the grain structure, is much smaller than either the wetted length or the component dimension in the order of less than 25 μm (<1 mil) [11].

2.5 Solder Attachment Failure

The failure of the solder attachment of a component to the substrate to which it is surface mounted is commonly defined as the first complete fracture of any of the solder joints of which the component solder attachment consists.

Given that the loading of the solder joints is typically in shear, rather than in tension, the mechanical failure of a solder joint is not necessarily the same as the electrical failure. Electrically, the mechanical failure of a solder joint results, at least initially, in the occasional occurrence of a short-duration (<1 μs) high-impedance event during either a mechanical or thermal disturbance. From a practical point of view, the solder joint failure is defined as the first observation of such an event.

For some applications this failure definition might be inadequate. For high-speed signals with sharp rise times signal deterioration prior to the complete mechanical failure of a solder joint might require a more stringent failure definition. Similarly, for applications which subject the electronic assemblies to significant mechanical vibration and/or shock loading, a failure definition that considers the mechanical weakening of the solder joints as the result of the accumulating fatigue damage might be necessary.

3. RELIABILITY PREDICTION MODELING

3.1 Creep-Fatigue Modeling

It has been experimentally shown [2,4,[12][13]-[14]] that the fatigue life of surface mount solder joints can be described by a power law of some damage term or descriptor, similar to the fatigue of the more typical engineering metals.

The most general fatigue life relationship is the strain-energy relationship of Morrow [15]

$$N_f(50\%) = \frac{1}{2}\left[\frac{2e_f'}{\Delta W}\right]^{-\frac{1}{c}} \qquad (1)$$

where
e_f' = fatigue ductility coefficient,
ΔW = the cyclic visco-plastic strain energy, which simply stated is the area of the cyclic hysteresis loop in the stress-strain diagram, described by one fatigue cycle,
c = the fatigue ductility exponent, -0.5 to -0.7 for common engineering metals.

The Coffin-Manson low-cycle fatigue equation [16] is perhaps the most well known of the fatigue life relationships.

$$N_f(50\%) = \frac{1}{2}\left[\frac{2e_f'}{\Delta g_p}\right]^{-\frac{1}{c}} \qquad (2)$$

where
Δg_p = the cyclic plastic strain range.
For solder joints, power laws frequently referred to as modified Coffin-Manson equations are commonly used. However, the terminology modified Coffin-Manson equations is in most cases inappropriate, because those equations where not derived from a modification of the Coffin-Manson equation, but naturally developed by correlating the results from fatigue tests as did the Coffin-Manson equation. Furthermore, the specialized case of the Coffin-Manson equation is itself a modification of the more general strain-energy relationship of Morrow [15]. The simplification to the Coffin-Manson equation is possible, because for non-creeping metals a fixed relationship between stress and strain the stress-strain curve exists and therefore the strain range is an adequate descriptor of the visco-plastic strain energy.

The damage terms, ΔW and Δg_p, describe cyclically occurring damage due to plastic deformations. If the plastic deformations of the solder, resulting from both plastic yielding and creep deformations, can adequately be quantified, Eqs 1 or 2 can serve solders as well as the other metals.

However, the time-dependent stress-relaxation/creep behavior of the solder at typical use environments (see Table I), makes it very difficult to assess the true cyclic plastic deformation of the solder in a Design for Reliability (DfR) process at the design of products.

Practical reasons strongly suggest the use of a damage term , ΔD, that is based on the total thermal expansion mismatch whether or not the stress-relaxation/creep process had sufficient time for completion. The total thermal expansion mismatch can readily be determined without the need for special expertise and without having to make assumptions.

Fortunately, it has experimentally been shown that the fatigue life correlates equally as well to the applied cyclic total strain range as to the cyclic plastic strain range [12]. The difference is that in this case the fatigue ductility exponent is a function of temperature and time to provide a measure of the completeness of the stress-relaxation process. The Engelmaier-Wild solder creep-fatigue equation [1-6, 9, 12] relates the cyclic total strain energy, represented by the cyclic fatigue damage term, ΔD, to the median cyclic fatigue life for both isothermal-mechanical and thermal cycling [17]

$$N_f(50\%) = \frac{1}{2}\left[\frac{2\varepsilon_f'}{\Delta D}\right]^{-\frac{1}{c}} \qquad (3)$$

where

ε_f' = fatigue ductility coefficient, 0.325 for eutectic and 60/40 Sn/Pb solder (for other solders the value of ε_f' is expected to be somewhat different).

ΔD = the cyclic total strain energy; for cycles with sufficient half-cycle dwell times to result in complete stress-relaxation/creep, $\Delta D = \Delta W$,

c = the fatigue ductility exponent resulting from Eq. 4,

$$c = -0.442 - 6\text{x}10^{-4}\bar{T}_{SJ} + 1.74\text{x}10^{-2}\ln\left(1 + \frac{360}{t_D}\right) \qquad (4)$$

where

T_{SJ} = mean cyclic solder joint temperature,

t_D = half-cycle dwell time in minutes.

The half-cycle dwell time relates to the cyclic frequency and the shape of the cycles and represents the time available for the stress-relaxation/creep to take place.

Equations 3 and 4 come from a generic understanding of the response of SM solder joints to cyclically accumulating fatigue damage resulting from shear displacements due to the global thermal expansion mismatches between component and substrate. These shear displacements cause time-independent yielding strains and time-, temperature-, and stress-dependent creep/stress relaxation strains. These strains, on a cyclic basis, form a visco-plastic strain energy hysteresis loop which characterizes the solder joint response to thermal cycling and whose area, given as the damage term ΔD, is indicative of the cyclically accumulating fatigue damage. Hysteresis loops in the shear stress-strain plane have been experimentally obtained [13, 18-19-20].

3.2 Damage Modeling

The assessment of the cyclically cumulating fatigue damage is not a straight-forward task. While the reliability models in Eqs. 1 through 3 are widely used, the question of how to best quantify the cyclic fatigue damage is still hotly debated.

There are a number of ways to determine the damage terms for creep-fatigue models. These different methods have their merits depending on their purpose and trade-offs include accuracy, precision, applicability, cost, ease of use and expertise required. They have been categorized as requiring efforts characterized as being Calculator-, PC-, Workstation, and Supercomputer-based [21]; while the increasing required effort gives greater details, including second-order effects, and allows assessment of complex structures beyond the simpler methods, it also requires increasing modeling complexities with more necessary frequently not fully-supported [22] assumptions.

Closed-form empirically-based relationships of the first-order design parameters cannot include second-order effects and have use limitations due to their simple nature. However, due to their simple form, they allow a direct assessment of the impact of the primary design parameters as well as design trade-offs.

The following cyclic fatigue damage terms are of the simplified closed-form type and should be utilized with the application caveats that follow [1-6, 9, 12, 17, 23].

The cyclic fatigue damage term for leadless SM solder attachments, for which the stresses in the solder joints exceed the solder yield strength and cause plastic yielding of the solder, is

$$\Delta D(\text{leadless}) = \left[\frac{FL_D\, Da\, \Delta T_e}{h}\right] \qquad (5)$$

and for SM solder attachments with compliant leads the cyclic fatigue damage term is

$$DD\,(leaded) = \left[\frac{FK_D\,(L_D\,Da\,DT_e)^2}{(133\text{ psi})Ah} \right] \qquad (6)$$

where for metric units the scaling coefficient is 919 kPa instead of 133 psi. Equations 5 and 6 contain the design parameters that have a first-order influence on the reliability of SM solder attachments. They are

A = effective minimum load bearing solder joint area;

F = empirical "non-ideal" factor indicative of deviations of real solder joints from idealizing assumptions and accounting for secondary and frequently intractable effects such as cyclic warpage, cyclic transients, non-ideal solder joint geometry, different solder crack propagation distances, brittle IMCs, Pb-rich boundary layers, and solder/bonded-material expansion differences, as well as inaccuracies and uncertainties in the parameters in Eqs. 3 through 6; 1.5>F>1.0 for ball/column-like leadless solder joints (C4, C5, BGAs, CGAs), 1.2>F>0.7 for leadless solder joints with fillets (castellated chip carriers and chip components), F□1 for solder attachments utilizing compliant leads;

h = solder joint height, for leaded attachments h≡1/2 of solder paste stencil depth as a representative dimension for the average solder thickness;

K_D = diagonal" flexural stiffness of unconstrained, not soldered, corner-most component lead, determined by strain energy methods [see [24][25][26][27]] or FEA, leads fall into groups of super-compliant leads K_D<~5 N/mm (~30 lb/in), compliant leads ~5 N/mm<K_D<~90 N/mm, and non-compliant leads K_D>~90 N/mm (~500 lb/in);

L_D = maximum distance between component center and the most remote component solder joint measured from the component solder joint pad center; L_D is sometimes referred to as the distance from the neutral point (DNP);

T_C, T_S = steady-state operating temperature for component, substrate (T_C>T_S for power dissipation in component) during high temperature dwell;

$T_{C,0}$, $T_{S,0}$ = steady-state operating temperature for component, substrate during low temperature dwell, for non-operational (power off) half-cycles $T_{C,0}$ =$T_{S,0}$;

ΔT_e = $\Delta(a\Delta T)/\Delta a$, effective cyclic temperature swing;

$\grave{T}_{SJ}$ = $(1/4)(T_C+T_S+T_{C,0}+T_{S,0})$, mean cyclic solder joint temperature;

a_C, a_S = coefficients of thermal expansion (CTEs) of component, substrate;

ΔT_C = T_C-$T_{C,0}$, cyclic temperature swing for component;

ΔT_S = T_S-$T_{S,0}$, cycling temperature swing for substrate (at component);

$\Delta(a\Delta T)$ = $|a_S\Delta T_S - a_C\Delta T_C|$, absolute cyclic expansion mismatch, accounting for the effects of power dissipation within the component as well as temperature variations external to the component;

Δa = $|a_C - a_S|$, absolute difference in CTEs of component and substrate, CTE-mismatch, because of the inherent variability in material properties Δa<2x10^{-6} should not be used in calculating reliability.

3.3 CAVEAT 1 Solder Joint Quality

The solder joint fatigue behavior and the resulting reliability prediction models, were determined from thermal cycling results of solder joints that failed as a result of fracture of the solder, albeit sometimes close to the IMC layers. For solder joints for which layered structures are interposed between the base material and the solder joints, these equations could be optimistic upper bounds if the interposed layered structures become the weakest link in the surface mount solder attachments. Such layered structures could be: metallization layers that have weak bonds to the underlying base material, or are weak themselves, or dissolve essentially completely in the solder; oxide or contamination layers preventing a proper metallurgical bond of the solder to the underlying metal; brittle IMC layers too thick due to too many or improperly long high temperature processing steps.

Solder joints which have solder joint heights (gaps) of h<50 µm (2 mils) also require special attention. For solder joints that thin, the gap is essentially filled with intermetallic compounds and those solder metals that do not go into solution with the base metals to form the IMCs. Therefore modeling based on solder behavior does not apply because these gaps are not filled with solder [28]. These materials do not creep as readily, if at all, at the prevailing temperatures and are typically more brittle, but much stronger than solder. Thus, fatigue lives are longer than would be predicted from Eqs. 1 through 3 unless overstress conditions occur.

On the other hand, the fatigue lives of solder attachments can be underestimated by Eqs. 1 through 3 if the component is underfilled with a load-bearing substance, e.g., epoxy [29]. Components that are glued-down to the substrate result in higher solder joint fatigue reliability, since the solder joints are loaded in compression when the adhesive contracts on cooling from the solder reflow temperatures. Covercoats can either increase or decrease solder joint fatigue lives depending on the properties of the covercoat and when and how it is applied. Parylene has been found to increase the solder joint fatigue live by about a factor of three.

Whether the solder pads are solder-mask define (SMD) or non-solder-mask-defined (NSMD) also influences the actual cycles to failure.

In general, caution might be indicated in all instances were the predicted life is less than 1000 cycles, because the severe loading conditions producing such short lives are likely to produce different damage mechanisms or/and failure modes.

3.4 CAVEAT 2 Large Temperature Excursions

Solder joints experiencing large temperature swings which extend significantly both below and above the temperature region bounded by -20°C to +20°C, in which the change from stress- to strain-driven solder response takes place, do not follow the damage mechanism described in Eqs. 1 and 2 [30]. The damage mechanism is different than for more typical use conditions and is likely dependent on a combination of creep-fatigue, causing early micro-crack formation, and stress concentrations at these micro-cracks causing faster crack propagation during the high stress cold temperature excursions, as well as recrystallisation considerations.

3.5 CAVEAT 3 High-Frequency/Low-Temperatures

For high-frequency applications, f>0.5 Hz or t_D<1 s, e.g., vibration, and/or low temperature applications, T_C<0°C, for which the stress relaxation and creep in the solder joint is not the dominant mechanism, the direct application of the Coffin-Manson [15] fatigue relationship might be more appropriate.

For loading conditions of this character, it is possible that high-cycle fatigue behavior may be observed.

3.6 CAVEAT 4 Local Expansion Mismatch

For applications for which the global thermal expansion mismatch is very small, e.g. ceramic-on-ceramic or silicon-on-silicon (flip-chip solder joints), the local thermal expansion mismatch becomes the primary cause of fatigue damage. Equations 5 and 6 do not address the local thermal expansion mismatch.

For leaded surface mount components with lead materials that have CTEs significantly lower than copper alloy materials, e.g. Kovar or Alloy 42, the results from the model will be optimistic, since the fatigue damage contributions from the solder/lead material CTE-mismatch, the local thermal expansion mismatch, are not included.

It has been shown that the interfacial stresses resulting from the local expansion mismatch follow [31]

$$t \propto L\,(\alpha_{Solder} - \alpha_{Base})(T_{max} - T_{min}) \qquad (7)$$

where L is the wetted length of the solder joint.

In addition, besides substantial shear stresses at the interface between the solder joint and the base material to which it is wetted, even larger peeling stresses occur. Both of these stresses are proportional to the parameters given in Eq. 7.

In most applications, the local expansion mismatch results in contributory damage to the more important damage caused by the global expansion mismatch.

From the available experimental data, the damage term, to be used in Eq. 3, for the local expansion mismatch alone is

$$DD(local) = \left[\frac{L\,D\alpha\,DT_e}{L_0}\right] \qquad (8)$$

where the parameters are the same as in Eq. 6 and L_0=0.1 mm (4 mils), a scaling wetted length.

From Eqs. 7 and 8 it is quite clear, that for leads consisting of Alloy 42, the wetted length of the solder joint, that is the length of the lead foot should be minimized to reduce interfacial stresses. That, of course, is contrary to the good practice that the foot length should be at least three times the lead width for optimum solder joint quality. However, since in most applications, the local expansion mismatch results in contributory damage to the more important damage caused by the global expansion mismatch, this contra-indication can be ignored without suffering catastrophic consequences.

The local expansion mismatch is than treated as an additional loading condition in Eq. 3 under the assumption that the two damage terms are directly additive. If this assumption is not fully appropriate, it is at least conservative.

3.7 Statistical Failure Distribution and Failure Probability

While the physical parameters define the median cyclic fatigue life from physics-of-failure considerations, solder attachment failures for a group of identical components will follow a distribution like all fatigue results which typically is best described by a Weibull statistical distribution [32]. Given the statistical distribution, the fatigue life at any given failure probability can be predicted as long as the slope of the Weibull distribution is known. Thus, the fatigue life of surface mount solder attachments at a given acceptable failure probability, x, is assuming a two-parameter (2P) Weibull statistical distribution given by

$$N_f(x\%) = N_f(50\%)\left[\frac{\ln(1-0.01x\,\%)}{\ln(1-0.5)}\right]^{\frac{1}{b}} \qquad (9)$$

where
b = Weibull shape parameter or slope of the Weibull probability plot; typically $b \approx 3$ for fatigue tests, from low-acceleration tests of stiff leadless solder attachments $b \approx 4$ and ≈ 2 for compliant leaded attachments.

The value of b has a significant impact on the design requirements to meet reliability goals calling for low failure probabilities; low values of b indicate a wide distribution and make meeting reliability goals more difficult. Experimentally, b can be found to be quite variable with more severely accelerated reliability tests resulting in tighter failure distributions and thus giving larger values for b. Typically $b \approx 3$ is given for fatigue tests of structural metals; values of b in the range of 1.8 to 10 have been observed. Evidence exists that shows an inverse relationship between b and the number of cycles to failure.

There is some, unfortunately as yet inadequate, evidence that for lower failure probabilities a three-parameter (3P) Weibull distribution, postulating a failure-free period prior to first failure [28,[33]] may be applicable. From physics-of-failure and damage mechanism considerations, a failure threshold as provided by a 3P-Weibull distribution makes sense, since the fatigue damage in the solder joints has to accumulate to crack initiation and complete crack propagation. While the 2P-Weibull distribution may be overly conservative for designs to very small acceptable failure probabilities ($\sim x < 0.1\%$), a too liberal choice of the failure-free period is definitely non-conservative. From most of the available data reported failure-free periods as large as $0.46\,N_f(50\,\%)$ need to be questioned [33]. This area requires more work.

Also, when designing to low failure probabilities, the variability in the quality of the solder joints may no longer be negligible; also solder joints with latent defects that made it into the field will have in impact on the actual failure experience of a product in the field.

3.8 Multiple Cyclic Load Histories

The loading histories over the life of a product frequently includes many different use environments and loading conditions [[34], [35]]. Multiple cyclic load histories (e.g., "Cold" temperature fatigue cycles combined with higher temperature creep/fatigue cycles (see Table I) combined with vibration and local expansion mismatches) all make their contributions to the cumulative fatigue damage in solder joints. Under the assumption that these damage contributions are linearly cumulative this assumption underlies Eqs. 1 through 3 as well and that the simultaneous occurrence or the sequencing order of these load histories makes no significant difference, the Palmgren-Miner's rule [[36]] can be applied.

Frequently the initial reliability objective is stated as an allowable net cumulative damage ratio (CDR). The CDR is calculated as the sum of the ratios of the number of occurring load cycles to the fatigue life at each loading condition and is

$$\text{CDR} = \sum_{j=1}^{j} \frac{N_j}{N_{f,j}} < 1 \qquad (10)$$

where
N_j = actually applied number of cycles at a specific cyclic load level j,
$N_{f,j}$ = fatigue life at the same specific cyclic load level j alone.

The fatigue life is frequently not completely specified and is normally taken to be the mean cyclic fatigue life. Equation 10 has to be used with the allowable CDR significantly less than unity to provide margins of safety, or more accurately, margins of ignorance.

Because the failure of solder joints results from wearout due to fatigue, the failure rate is continuously increasing. This is in stark contrast to the reliability design philosophy of MIL-HDBK-217 [[37]] which presumes a constant failure rate. These increasing failure rates are properly represented by an appropriate statistical failure distribution.

Thus, to assure low failure risks, the fatigue life should be specified at the acceptable cumulative failure probability at the end of the design life as per Eq. 9. Thus, Eq. 10 is more appropriately written as

$$\text{CDR}(x\%) = \sum_{j=1}^{j} \frac{N_j}{N_{f,j}(x\%)} = 1 \qquad (11)$$

where
CDR(x%) = cumulative damage ratio resulting in a cumulative failure probability of x%,
$N_{f,j}(x\%)$ = fatigue life at the cyclic load level j and a failure probability of x%.

This approach works very well for the design of the solder attachment for a single component. However, it is inadequate for a reliability analysis of a the whole assembly.

3.9 System Reliability Evaluation

Equations 1 through 9 address the reliability of the SM solder attachment of individual components. Systems consist of a variety of different components most of which occur in multiple quantities. Further, as shown in Table I, many use environments cannot and should not be represented by a single thermal cyclic environment, and accumulating fatigue damage from other sources, such as cyclic thermal environments as described in Caveats 2 to 4 as well as vibration, needs to be included also.

For a multiplicity of components, i, in the system, the effect of the various components on the system reliability can be determined from

$$F_S(N) = 1 - \exp\left\{\ln(1-0.01x)\sum_{i=1}^{i} n_i\left[\sum_{j=1}^{j}\frac{N_{i,j}}{N_{f,i,j}(x\%)}\right]^{b_i}\right\} \quad (12)$$

where
$F_S(N)$ = system cumulative failure probability after N total cycles,
n_i = number of components of type i,
$N_{i,j}$ = actually number of cycles applied to component i at a specific cyclic load level j,
$N_{f,i,j}(x\%)$ = fatigue life of solder attachment of component i at load level j at x% failure probability,
b_i = Weibull slope for SM solder attachment of component i.

4. DfR-PROCESS

The aim for any DfR-procedure is the reduction of the damage terms given in Eqs. 5, 6 8 to levels that will assure the long-term reliability of the solder attachments of the product in the field. The DfR-process needs to emphasize a physics-of-failure perspective without neglecting the statistical distribution of failures.

From these equations the possible DfR-measures are very obvious. Appropriate DfR-measures to reduce the global expansion mismatch are best employed in combination for improved reliability margins. These measures are:

1) Reduction of component size, e.g., fine pitch and area arrays;
2) CTE-tailoring of components and substrates, e.g., low CTE substrates for ceramic components and parts with Alloy 42 leadframes, and use of Cu leadframes and soft die attach for components on FR-4 substrates;
3) Reduction of temperature swings, e.g., heat transfer measures, satellite rotation, independent heaters;
4) Increasing attachment compliancy, e.g., by increasing the solder joint height (high melt solder balls, solder columns), and compliant leads;
5) Reduction in strain concentrations, e.g., non-uniform solder joint cross-sections, solder-mask-defined soldering pads;

DfR-measures to reduce the local expansion mismatch are:

1) Avoiding base materials that have a large a CTE-mismatch with solder, e.g., silicone, Alloy 42, ceramic;
2) Reduction of the continuous wetted length of solder joints to reduce interfacial stresses, e.g., flip-chip.

DfR-measures to assure solder attachment reliability to low failure probabilities are:

1) Avoiding the use of the high Weibull distribution slopes, b, that result from highly accelerated test programs, e.g., from low-acceleration reliability test the recommendation can be made for $b \square 4$ for leadless solder attachments and $b \square 2$ for compliant leaded attachments;
2) Avoiding the use of 3-P Weibull distributions unless good evidence for a failure-free period exists.

Global Expansion Mismatch. CTE-tailoring involves choosing the materials or material combinations of the MLB and/or the components to achieve an optimum ΔCTE. An optimum ΔCTE for active components dissipating power is ~1-3 ppm/°C (depending on the power dissipated) with the MLB having the larger CTE, and 0 ppm/°C for passive components. Of course, since an assembly has a multitude of components, full CTE-optimization cannot be achieved for all components it needs to be for the components with the largest threat to reliability. For military applications with the requirement of hermetic and thus ceramic components, CTE-tailoring has meant the CTE-constraining of the MLBs with such materials as Kevlar and graphite fibers, or copper-Invar-copper and copper-molybdenum-copper planes.

Such solutions are too expensive for most commercial applications for which glass-epoxy or glass-polyimide are the materials of choice for the MLBs. Thus, DfR-measures have to take the form of avoiding larger size components that are either ceramic (CGAs, MCMs), plastic with Alloy 42 leadframes (TSOPs, SOTs), or plastic with rigid bonded silicon die

(PBGAs).

Increasing attachment compliancy for leadless solder attachments means increasing the solder joint height (C4, C5, shimming, gluing [38, 39], 10Sn/90Pb balls, 10Sn/90Pb columns) or switching to a leaded attachment technology. For leaded attachments increasing lead compliancy can mean changing component suppliers to those having lead geometries promoting higher lead compliancy or switching to fine-pitch technology.

For Flip Chip and Chip Scale technologies the biggest reliability concern is the large expansion mismatch between the chip silicon and the polymeric substrate. This either means relatively small chips or the use of organic underfill materials which relieve the solder joints from most of the thermal expansion mismatch loads. The underfill material does however make repairs difficult if not impossible.

Grid array components (GACs) come in a variety of styles and materials. The major variations are BGAs, available with plastic bodies as PBGAs or ceramic bodies as CBGAs, and solder attached with either the C5-process or with solder joints containing 10Sn/90Pb solder balls; and CGAs with 10Sn/90Pb solder columns.

The long-term reliability of the solder attachments to FR-4 PCBs is a big concern with GACs. The global thermal expansion mismatch between the GACs and the PCB can be quite large as the result of the combination of large GAC sizes, large differences between the thermal expansion coefficients of the GACs and the PCB (ΔCTE), and the power dissipation within the GACs. Further, depending on the die attach and the GA material, a large localized global thermal expansion mismatch underneath the die and a not insignificant local thermal expansion mismatch between the solder itself and the GA surface can increase the threat to reliability. In addition, the implementation of the Government-mandated Energy Star -program, the number of thermal cycles could be a multiple of the once-a-day diurnal/on-off cycles.

The solder attachments of GACs vary depending on the loading conditions to which the solder joints are subjected to and the reliability requirements for the product. As mentioned earlier, BGAs are attached with either the C5-process or with 10Sn/90Pb solder balls. The C5-process, similar to the C4- or flip-chip-process, results in solder joints heights that are less controlled and lower {(h~400 to 640 µm (~16 to 25 mils)}, while the 10Sn/90Pb solder balls typically with diameters of 760 to 890 µm (30 to 35 mils) result in uniform solder joint heights of the same dimension since the 10Sn/90Pb solder has a liquidus temperature significantly above the near-eutectic Sn/Pb solders and does not melt during a typical reflow process. The solder columns, which currently are only used for ceramic GACs, are 10Sn/90Pb columns with lengths of 1.27 to 2.29 mm (50 to 90 mils) that are either cast onto the CGA or are wires soldered to both the CGA and the substrate with near-eutectic Sn/Pb solder. The ratios of fatigue lives, all parameters other than the solder joint height being equal, are CBGA(0.41 mm/16 mils) : CBGA(0.76 mm/30 mils) : CGA(2.29 mm/90 mils) = 1 : 4 : 45. The height of the solder columns is limited by the requirement that the column height-to-diameter aspect ratio does not produce slender columns thus changing the loading conditions; cast columns can accommodate larger aspect ratios.

It is also of importance for PBGAs, how the silicon chips are attached to the BGA body. For cavity-up components, only a thin plastic layer separates the solder joints from the die attach. As a consequence, the CTE underneath a rigid die attach can be as low as 6 to 8 ppm/°C (very similar to ceramic) locally raising the CTE-mismatch between the PBGA and the FR-4 PCB from ~2 to 10 ppm/°C. Thus, the die size can only be ~$^1/_5$ the size of the BGA to not negatively affect the reliability. Typically, die sizes are significantly larger than that, with the result that the solder joints at the corners of the die fail before the outermost BGA corner joints. The larger the die, the worse the solder attachment reliability [40, 41]. Thus, the trend towards Perimeter-PBGAs, where solder joints exist only on the package perimeter with the possible exception of some thermal solder balls and vias in the package center for routing reasons, is beneficial for reliability [42].

Of not insignificant influence on the reliability is the geometry of the solder joints as well as the solder pad metallization. Especially the solder masks can have a negative influence if they are used for solder-mask-defined (SMD) pads with the solder mask on the metallization pads affecting the solder joint geometries. Stress concentrations created by the SMD-solder joint geometries can be the origin of solder joint failures and reduced reliability. For equal solder joint height, increases in fatigue life by factors of about 1.25 to 3 can be anticipated with the use of non-solder-mask-defined (NSMD) vs. SMD pads with the larger improvements for solder joints with the more severe loading conditions [14, 41, 43-444546].

Local Expansion Mismatch. Solder joint fractures for BGAs are typically near the interface between the BGA and the barrel-shaped solder joints; this is a consequence of the contribution to the solder joint loading of the local expansion mismatch between the solder and the die-constraint BGA body [41] in addition to solder ball geometry effects. Substantial increases in fatigue life have reported with a soft die attach [43].

Large power diodes frequently have Alloy 42 leads with large solder attachment areas. This can lead to premature solder joint failures.

Component Warpage. Some components are constructed with substantial asymmetries. The Super-BGA, having a copper heat-spreader plane, is such a component. Solder joint fractures as the result of component warpage due to asymmetric thermal expansion mismatches within BGAs with high power dissipation have been reported.

Statistical Considerations. The temptation exists to use a large value for b , since that indicates low failure probabilities without significant design efforts. The temptation is fueled by the experimentally obtained large values for b in highly accelerated reliability tests. Values of b as low as 1.8 have been observed in low-accelerated tests mimicking actual use conditions, whereas highly accelerated tests have yielded b s in excess of 9.0. Evidence exists that shows an inverse

relationship between *b* and the number of cycles to failure. Choosing high *b*-values is non-conservative.

Using a 3-P Weibull distribution is also tempting, since low failure probabilities are easier obtained. The results of low-acceleration tests show that the failure-free period can not last longer than perhaps 0.001 to 0.005 N_f(50 %).

Other Failure Sources. For PBGAs the additional reliability issue of via and trace failures has surfaced [47]. The former issue is addressed in Reference 48 and the latter can be remedied by wider traces and/or better copper foil [49].

5. SUMMARY

From this paper it is clear that a Design for Reliability can assure the reliability of the surface mount solder attachments. The DfR-methodology described has been experimentally verified for many components, including BGAs and CGAs, by work at AT&T Bell Laboratories.

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