ABSTRACT

Fault simulation is the problem of finding all single stuck at faults in a circuit which are detected by a given input set of test vectors. One of the most efficient schemes for performing fault simulation is propagating the effect of single stuck-at faults one at a time [9], hence the term single fault propagation.

In this paper we propose the use of efficient data structures and graph algorithms to improve the efficiency of single fault propagation. We give an efficient event driven single fault propagation algorithm which uses a priority queue. We then show how the use of dominators in directed graphs [11] [6] can speed up single fault propagation algorithms for fault simulation. We developed algorithms both for the special case of a single test vector, and for the general case which is useful when fault dropping is relevant.

Our major result is that dominators coupled with efficient priority queues provide a very clean as well as efficient framework for minimizing the effort involved in single fault propagation. Our algorithm subsumes the heuristics proposed by [2] as special cases of a more uniform framework, and supercedes them in that we show cases that can be handled by dominators and not by partitioning into fanout free regions alone.

References

A Demand Driven Multi-Word Parallel Fault Simulator

Steven P. Smith, Richard G. von Blucher
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ABSTRACT

A fault simulation algorithm is presented which combines multi-word parallel fault simulation with a new concept of logic simulation called demand driven simulation. Where traditional event driven simulation propagates signal values forward through a circuit in response to input pin events, demand driven simulation propagates requests for simulation values backwards both through the circuit and through time. In this manner, only those evaluations required to obtain "watched" signal values are performed. This technique extends directly to strobe signals and strobe times during fault simulation, with the result being notably superior performance over a comparable event driven parallel fault simulator. Empirical results for both an event driven and a demand driven three valued multi-word parallel fault simulator are presented for ten test cases.

REFERENCES

High-Speed Fault Simulation Using a Vector Processor

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Abstract

In this paper, we describe a new approach to accelerating fault simulation using a vector processor. We discuss the gate-level fault simulation of combinational circuits. As a vector processor oriented simulation technique, we propose a dynamic two-dimensional parallel simulation technique. In this technique, 1) we obtain large vector length by utilizing both fault and pattern parallelism, and 2) efficiently exploit fault dropping by adjusting the two parallelism factors complementarily from pass to pass. We further reduce the computation time by combining this technique with selective tracing under the notion of multiple fault propagation. The experiments on the Fujitsu FACOM VP-200 vector processor tell us that the simulation speed is accelerated by 10 \~ 15 times through vectorization.

References

MUSTANG: State Assignment of Finite State Machines for Optimal Multi-Level Logic Implementations

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Abstract

We address the problem of state assignment for synchronous finite state machines (FSM), targeted towards multi-level combinational logic and feedback register implementations. Optimal state assignment aims at a minimum area implementation. All previous work in automatic FSM state assignment has been directed at Programmable Logic Array (PLA) i.e. two-level logic implementations. In practice, most large FSM's are not synthesized as a single PLA for speed and area reasons - multi-level logic implementations are generally used for smaller delay and area. In this paper, we present algorithms which produce a state assignment that minimizes the number of literals in the resulting combinational logic network after multi-level logic optimization. We present results over a wide range of benchmarks which prove the efficacy of our techniques. Literal counts averaging 25-40% less than other state assignment programs have been obtained.

REFERENCES

New State Assignment Algorithms for Finite State Machines Using Counters and Multiple-PLA/ROM Structures

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ABSTRACT

The objective of our work was to derive regular digital control structures for full-custom VLSI chips and to synthesize them logically and physically on a minimum of silicon area. In this paper a new design method is presented which allows to synthesize finite state machines (FSM) using multiple-PLA/ROM structures and loadable counters for the FSM's states. It is shown that the new state assignment algorithms lead to significantly smaller areas on a VLSI chip than conventional designs.

REFERENCES

An Efficient Microcode-Compiler for Custom DSP-Processors

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ABSTRACT

In this paper, a microcode compiler for custom DSP-processors is presented. This tool is part of the CATHEDRAL II silicon compiler. Two optimization problems in the microcode compilation process are highlighted: microprogram scheduling and memory allocation. Algorithms to solve them, partly based on heuristics, are presented. Our compiler successfully handles repetitive programs, and is able to decide on hardware binding. In most practical examples, optimal solutions are found. Whenever possible, indications of the complexity are given.

References
ABSTRACT

A new routing system for the general custom building block layout style is presented. The main features of the system are: construction of a floor plan topology by slicing, global routing by means of a steiner tree heuristic and gridless channel routing with rigorous contour compaction, which allows variable width wires and easy adaptation to the design rules. The router handles arbitrarily sized blocks and takes advantage of irregular channel boundaries. Power and ground lines are routed planarly with variable width. An O(n log n) algorithm for making contours irreduntant is given. Benchmarks of the channel router and application to a small chip are included.

REFERENCES

ABSTRACT

The next generation of building block layout system, named BEAR (Building-block Environment Allocation and Routing system), is being developed at U. C. Berkeley. A new routing scheme for achieving feasible routing order in a non-slicing structured placement is presented and its superiority is demonstrated. We have unified topological and geometrical representations, and developed efficient methods to update topological information (eg., global routing information) after geometrical operations (eg., block movement). Also, we address the issue of performance optimization by including a scheme for timing-driven layout that spans the entire layout process. This approach is based on the intelligent generation of spatial constraints from timing constraints as opposed to simple-minded net weighting. Finally, a practical approach to the problem of power and ground routing is proposed to include such thing as multiple pads, loops and constraints due to electromigration and voltage drops.

References

A New Area-Efficient Power Routing Algorithm for VLSI Layout

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Abstract

A new graph algorithm to route non-crossing VDD and GND trees on one layer is developed for VLSI designs. The algorithm finds trees with as small area as tractably possible under metal migration and voltage drop constraints. Experimental results show that the power wire area is considerably smaller than a previously developed method for single-layer routing.

References
Efficient Algorithms for Solving the False Path Problem in Timing Verification

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Abstract

In this paper we propose two algorithms for solving the problem of false paths in timing verifiers. The algorithms are built on top of the SLOCOP timing verifier which is characterized by the modeling of both the logic and the timing behavior of the analyzed circuit. This model allows to automatically verify that the propagation conditions of the sub-circuits present in a path are not violated. A first analysis of the circuit by the PERT algorithm guides the critical path search and allows to prune sub-graphs that cannot lead to the solution. In addition, the two algorithms continuously update bounds on the length of the critical path, thus allowing the user to interrupt the search as soon as a sufficiently accurate estimate has been obtained. The results obtained by a first implementation are presented and show a gain in accuracy of as much as 50% for optimized circuits. Furthermore, the observed run times prove that the combinatorial explosion associated with the search is successfully curbed by our technique.

References

A Timing Error Corrector for VLSI Synchronous Path Circuits

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ABSTRACT

In synchronous VLSI circuits, the detection and correction of timing errors due to clock skew requires accurate simulation of clock waveforms in addition to data path waveforms. Previous approaches to searching all the paths require the execution time of $O(N^L)$, where $N$ is the average fanout of gates and $L$ is the number of logic levels. This paper presents an efficient algorithm for detection and correction of timing errors between latch pairs in synchronous VLSI circuits. To detect timing errors the hold time and the set-up time of each latch are checked with realistic signal waveforms. To correct the timing errors two procedures are used: (1) resizing transistors in clock paths, and (2) resizing transistors in critical signal paths and shortest signal paths. This algorithm has been implemented in FRANZ LISP using a hierarchical programming and data-base structure to save memory space. A 160-transistor example demonstrates that the use of this program can significantly reduce the design time over the conventional manual approach.

REFERENCE
ABSTRACT

Many workstation simulators, and especially hardware accelerators, support only gate level models. Most do not support pin-to-pin timing [1] [2] [3] [4] [5]. This is a design tradeoff for very fast simulation.

While behavioral modeling languages allow for accurate pin-to-pin timing and good error detection, the problem is much more difficult for gate level models. This paper describes a program which derives a gate level model from a behavioral description of a standard cell, and which can support pin-to-pin timing even when the host simulator does not.

References.
A Robust Approach for Timing Verification

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Abstract

Based upon a newly introduced signal delay time and a signal delay potential concept, a novel technique called the nodal-delay-potential equation approach is presented in this paper. With this approach the signal delay can be calculated in a general RC network without any restrictions; floating capacitors, grounded resistors, no driving source, multiple sources, initial charges, arbitrary input signals and any other network configurations besides the five basic structures used previously can be included. In the special case of a RC tree network, results from this method are in agreement with those of previous researchers, and the computational efficiency is also the linear function of the number of nodes in the network. The algorithm and analysis techniques of a circuit simulation program can be adopted easily for use in the new delay analysis.

References

The Boulder Optimal Logic Design System

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Abstract

We introduce the BOLD (Boulder Optimal Logic Design) system. BOLD is a system for optimally mapping combinational logic into standard cell or CMOS complex gate technologies. BOLD features a new method for multilevel logic minimization, based on the ESPRESSO approach, but with the following new developments: 1) An almost complete re-implementation of the ESPRESSO algorithm suite, expressly redesigned for the context of a multilevel Boolean Network; 2) Introduction of a new multilevel minimization procedure, called Boolean Resubstitution, which has no analog in 2-level minimization; 3) A new method for multilevel tautology checking, which merges basic concepts from the areas of general equivalence checking and automatic test pattern generation, and is especially tailored to work in the logic minimization context. The new method is incorporated into a program package, called ESPRESSO_MLT, which is compared to a previously published program package ESPRESSO_MLD [1]. Additionally, we compare our results to those produced by YSC [7] and MIS [6]. Experimental results are given, which show our method gives results superior in optimization quality to all three of these methods, and with significantly lower computational expense than ESPRESSO_MLD. The Boolean Network produced by ESPRESSO_MLT is prime, irredundant, and 100% testable for single input stuck faults. The tests for these faults are returned as a byproduct of the minimization.

REFERENCES

Multi-Level Logic Optimization and The Rectangular Covering Problem

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Abstract

This paper describes a new approach to the problems of factorization and decomposition of logic functions which is an important part of multi-level logic optimization. The key concept is to formulate these problems as a rectangular covering problem. This new approach has the potential to provide better solutions as it relaxes some of the constraints of a purely algebraic approach. In this paper, we present an algorithm to solve the rectangular covering problem and formulate both factorization and common-cube extraction as rectangular covering problems.

References

A Design Automation Tool for Fast, Efficient Decomposition of Logical Functions

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ABSTRACT

Decomposition of a logical function can result in significant reduction in the complexity of its implementation. However, it is extremely hard to discover decompositions in the Boolean domain since it requires exhaustive searches. We present a novel algorithm for spectral domain decomposition that avoids exhaustive searches and is very efficient in storage and computational requirements.

References

An Algorithm for Multiple Output Minimization

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Abstract

A computer aided design procedure for the minimization of multiple-output Boolean functions as encountered in the synthesis of VLSI logic circuits is presented in this paper. A fast technique for the determination of essential prime cubes without generating all the prime cubes is among the salient features of the algorithm. The paper also describes a new class of selective prime cubes called valid selective prime cubes that has proved to be a very powerful tool inasmuch as it guides the algorithm to the minimal set of selective prime cubes while encountering either an independent chain or an interconnected chain of cyclic prime cubes. The algorithm does not generate either the complement or all the prime cubes of the functions. Therefore, it is well suited to minimize functions with large complement size and/or very high number of prime cubes. Results of comparison with ESPRESSO II [1] and McBOOLE [2] have also been presented.

References

Algorithm for Block Placement with Size Optimization Technique by the Linear Programming Approach

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ABSTRACT

This paper presents an algorithm called BSOLP for minimizing chip area within the constraints on block size, relative block position and width of inter-block routing space. To obtain sufficient accuracy for practical applications, appropriate block size is selected from among actual layout examples and routing space is estimated highly accurately using global routing. This algorithm uses a linear programming approach which minimizes chip width and height simultaneously. An automatic block layout system using BSOLP algorithm achieves 5-10% smaller chip layouts for 19K-gate chips than a comparable system without this algorithm, and achieves 6% smaller layouts than manual design.

REFERENCES
ATLAS - A Technique for Layout using Analytic Shapes

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Abstract

This paper reports a significant advancement of the analytical placement algorithm based on the modified rectangle definition. A more realistic objective function, which incorporates translation, rotation and mirror operations, is presented.

Two solution methods, the Penalty Function Method (PFM) and the Sequential Quadratic Programming (SQP) method are compared showing that the PFM consistently performs better. An analysis of the reasons for the observed results suggests the ability of PFM to achieve a good solution which is insensitive to the initial placement.

The numerical solution techniques and the simulated annealing approach are compared. Finally, comparative results on some industrial examples are presented. One example compares TimberWolf and ATLAS, which shows that ATLAS got better result in this example.

References
Circuit Placement for Predictable Performance

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ABSTRACT

This paper describes an approach to the problem of incorporating performance objectives in the physical design of integrated circuit gate array or standard cell chips. The approach develops precise bounds for the delays of each circuit in a design by using available timing analysis tools and a new procedure called the "Zero-Slack Algorithm". Since the delay of a circuit depends on its load capacitance, delay bounds can be translated to length limits, and then used as constraints on the placement of circuits on the chip. If a wirable placement meeting these objectives is found, the desired performance of the design is guaranteed. Preliminary results indicate that the use of these timing-derived net constraints produces a substantial improvement in timing without sacrificing wirability.

REFERENCES

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SPECS2: An Integrated Circuit Timing Simulator

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Abstract

SPECS2 is a prototype implementation of a new timing simulation and modeling methodology. SPECS2 (Simulation Program for Electronic Circuits and Systems 2) is a tree/link based, event-driven, timing simulator. A modeling technique, which is predicated on the conservation of charge and energy, is employed to produce table models for device evaluation. The tables may be constructed to model devices at any desired level of detail. Thus, SPECS2 is a variable accuracy simulator. Grossly differing accuracy requirements may be specified for different runs and also mixed over different parts of the same circuit. SPECS2 implements a novel oscillation detection and suppression scheme that prevents algorithmic oscillation, while leaving real circuit results undistorted. SPECS2 takes advantage of the tree/link formulation of the circuit equations to provide a formal and general approach to timing simulation. It encounters no special problems with floating capacitors or transmission gates. Further, SPECS2 provides the framework for a generalized macromodeling and simulation capability.

References
TALISMAN: A Piecewise Linear Simulator Based on Tree/Link Repartitioning

X. Huang, L.T. Pillage, R.A. Rohrer
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Abstract

This paper presents TALISMAN (Tree And Link based Implicit Solution Method for the Analysis of Networks), a piecewise linear circuit simulator. TALISMAN can simulate circuits containing resistors, capacitors, ideal switches, diodes, bipolar transistors and MOSFETs. TALISMAN uses tree/link based analysis to set up the equations that characterize the circuit. The tree/link equations are formed from optimal trees and maintained in such a manner that an iterative solution technique can be used to solve them efficiently. TALISMAN allows piecewise linear models ranging from the ideal switch to those of near analog accuracy.

References

Dynamic Partitioning Method for Piecewise-Linear MOS Digital Circuits

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Abstract

This paper presents a method for dynamically partitioning MOS digital circuits for relaxation-based solution techniques. The transistor characteristics are approximated by piecewise-linear (pwl) functions. The dynamic partitioning is carried out at every iteration during the solution process by comparing integers representing region numbers in the pwl functions. In many instances the circuit is automatically partitioned into completely disconnected subcircuits, thus allowing efficient application of parallel processing techniques. The approach has been implemented in a computer program for transient analysis of MOS VLSI circuits. Computational speeds of two orders of magnitude or more as compared to standard circuit simulation has been observed in solving small circuits without much loss in accuracy. The speed improvement is expected to be higher as the size of the circuit increases.

References

How to Use Underrelaxation to Improve Waveform Relaxation Convergence

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Abstract

This paper presents a way to use underrelaxation in Waveform Relaxation analysis in order to overcome a poor convergence rate that can occur for simple MOS circuits, even when the classical WR convergence conditions are met. Theoretical determination of a relaxation parameter, practical implementation of underrelaxation in the MOSART WR program and experimental results are presented. For example, a case when the classical WR analysis requires more than 1000 iterations to converge is treated in only 4 iterations with a correct use of underrelaxation.

References
Combining Multi-Level Decomposition and Topological Partitioning for PLAs

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ABSTRACT

PLAs are attractive for automatic synthesis and layout of logic, especially for controllers. Earlier studies have concentrated on logic minimization of PLA descriptions (e.g. espresso) and the topological partitioning of the resulting layout (e.g. pleasure). Our work is the first to combine the space-saving advantages of multi-level decomposition with logic minimization, topological partitioning and a compact PLA layout style. Rather than have the logic designer hand partition a large and slow monolithic PLA, our tool automatically generates area-efficient multi-level PLAs. This paper presents PLASTIC, an integration of PLA tools, that yields area-efficient multi-level PLA implementations. Initial results, using logic descriptions from several processor chips developed at Berkeley, show area savings of up to 40%.

REFERENCES

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[EECS86b] EECS CAD group documentation for OCT LOGIC, U.C. Berkeley.
Technology Mapping in MIS

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Abstract

This paper presents efficient methods of mapping a complex set of Boolean equations onto a given set of primitive cells to minimize a total given cost function. The problem is transformed into a covering problem. Two approaches are taken: tree covering of a forest of trees and graph covering of a directed acyclic graph. The methods were implemented as a part of MIS [2], UC Berkeley's logic synthesis system. The methods allow easy changes to the cell library. Tradeoffs on the size of the cell library are discussed. Results are shown and the methods are compared to to the methods used in Dagon [6].

References
Impact of Library Size on the Quality of Automated Synthesis

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Abstract

A standard cell library is a library of cells such as NAND, NOR, and AND-OR-INVERT (AOI) gates that are implemented in a given technology. These libraries serve as a common back end for automated synthesis tools such as CONES [1] or LSS [2]. Standard cell libraries greatly simplify the automated synthesis process because they free the synthesis system from layout concerns and present a simple model of circuit behavior to the system. A natural question to consider is what components should be included in the cell library. A criterion for inclusion is the impact that the additional cells will have on the quality, measured in terms of speed and area, of the resulting circuit. Reasons for exclusion are the costs of creating and maintaining a library.

To date little solid information has been available to aid one in reasoning about a good library size. In order to address this question, in this paper we use an automatic synthesis environment to generate circuits which implement a set of standard benchmarks. We use five different cell libraries in this experiment ranging in complexity from 2 to 125 gates. Our results show that on the designs considered, a greater number of cells in the target library can dramatically reduce the final chip area with comparable timing. While these results were derived in an automated synthesis environment they are applicable to other environments where standard cell designs are used.

References

A Control Logic Synthesis and Optimization Algorithm with an Overlap Degree Vector

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ABSTRACT

A logic synthesis algorithm, ASTRO, has been developed for designing of high-performance, pipeline architecture processors. ASTRO is based on the designers' empirical knowledge, and can create and minimize control logic for data path. The control logic is generated on the basis of extended functional operators, such as IRDY, ORDY, and EXEC, in a description language called B[sup.2]DL. This logic also enables the increased utilization of hardware components, which is essential in a pipeline machine. The processing time needed for logic optimization is reduced without loss of performance by the new feature; a candidate selection method with an overlap degree vector. This new algorithm promises to decrease the time and effort for developing high performance processors.

REFERENCES

An Efficient Algorithm for Generation of Constraint Graph for Compaction

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Abstract

An algorithm for fast generation of constraint graph for compaction within a cell has been
formulated. The algorithm uses BitMaps which are derived from the interaction of layout
layers. These BitMaps are used for speeding up graph generation and for avoiding
creation of most redundant edges.

References:
Electrical Engineering and Computer Science, Berkeley, CA (1979)
Compaction" Proc. of the WG '83, International Workshop on Graph theoretic Concepts in Computer
Abstract

The DASL split grid compactor allows the splitting apart of virtual grids containing distinct circuit groups. The new compactor is as fast as the virtual grid compactor in MULGA, while the compacted results are comparable to those achieved with a graph-based compactor. The speed of the compactor is primarily due to the use of a new data structure.

References

A Constraint Based Incremental Compactor

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Abstract

This paper describes a novel approach to the integrated circuits layout compaction problem. A constraint based incremental compactor generates, and resolves the design rule constraints incrementally. An incremental constraint generation algorithm and an incremental longest path algorithm are presented. Several heuristics were developed to reduce the computation time. A very efficient interactive compactor for symbolic layout was developed.

References

Abstract

Symbolic layout systems have shown their utility for quickly creating design-rule-independent designs. While the quality of layout and speed of compaction for single cells is quite good, composition of these cells is either not as compact as desired or else requires a large amount of CPU time to compute. These shortcomings become most evident in regular arrays of cells. To handle arrays more efficiently we compact the cell on the surface of a cylinder or toroid, and take into account, during compaction, the constraints generated by arraying the cell with itself. Toroidal compaction sufficiently reduces the cell-to-cell spacing that often the cells can overlap during composition. Toroidal compaction has been implemented as part of the Lava symbolic layout system.

References
Efficient Circuit Segmentation for Pseudo-Exhaustive Test

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ABSTRACT

One of the major problems in pseudo-exhaustive testing has been the efficient determination of a good circuit segmentation. Two methods of reducing segmentation complexity are presented. The first, Circuit Reduction for Efficient Segmentation (CRES), consists of techniques that reduce a circuit to a smaller circuit that is equivalent under segmentation, as well as heuristic techniques that reduce the circuit complexity further while removing undesirable segmentation points. This smaller, less complex circuit can be used as input to any segmentation algorithm, significantly reducing segmentation cost. The results can then be translated into a segmentation of the original circuit. The second method of reducing the complexity of segmentation is the use of the maximal fanout-free regions of the circuit as an efficient initial segmentation. These techniques can be used together yielding even greater complexity reductions.

REFERENCES

A note on Random versus Deterministic Testing of gate level Combinational Circuits

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Abstract

Three strategies for testing gate level combinational circuits that are popularly used are: deterministic testing, random testing and pseudorandom testing. We address the question: Is random testing "computationally harder" than deterministic testing? We show that "computationally" random testing is "harder" than deterministic testing.

References

Linear-Testable Counters for Multiple Faults

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University of Minnesota Computer Science Department

ABSTRACT

Unary counters are combinational circuits such that the output vector is the count of the 1 values in the input vector. A balanced counter is required to have a number of input lines of the form $2^k - 1$, where $k$ is an integer greater than 1. Balanced counters can be implemented using only 3-bit full adders as the basic building block, interconnected in iterative manner, defined recursively. Despite reconvergent fan-out and a more complex topological structure than trees and one-and two-dimensional ILA's, it is shown that an $N$-cell ($N > 1$) balanced counter can be tested for multiple faults with a test set of size at most $5/8 (9N + 5 \log_2 N)$ (linear testability). A recursive formula for the test set is also presented.

REFERENCES

Using Statecharts for Hardware Description

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ABSTRACT

Statecharts have been proposed recently [6] as a visual formalism for the behavioral description of complex systems. They extend classical state-diagrams in several ways, while retaining their formality and visual appeal. In this paper we argue that statecharts can be beneficially used as a behavioral hardware description language. We illustrate some of the main features of the approach, including: hierarchical decompositioning, flexible concurrency and synchronization capabilities, multi-level timing constraint specifications and high visuality.

Bibliography
Design Representation and Transformation in the System Architect's Workbench

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Abstract

This paper describes a portion of The System Architect's Workbench, a tool for high-level design transformation and synthesis. The Workbench is built around a new model of design representation, based on linked behavioral, structural, and physical domains at multiple levels of abstraction. The Workbench also supports a new set of high-level behavioral and structural transformations, and allows the designer to explore high-level design alternatives interactively, automatically maintaining links between the domains. Transformations supported include inline expansion of procedures, combination of nested decoding operations, code motion, and process and pipestage formation. An example describes the transformation of a behavioral description of the MOS Technology 6502.

References
A Gridless Schematic Editor with a Geometric Constraint Mechanism

Robert Melville
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Abstract

We present an interactive picture editor designed to generate book-quality pictures of small electronic diagrams. While a diagram is being drawn, the user may install geometric constraints to control the position and alignment of objects on the screen. When one component is moved, other components on the screen may also move to preserve any relevant constraints. This movement is fast enough to provide a simple form of animation. The final output is a file in a picture-description language which is easily incorporated into documents.

References

EXCELLERATOR: Automatic Leaf Cell Layout Agent

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Abstract

A program is described which automatically generates the symbolic layout of custom CMOS cells from an input netlist and constraints. Layouts are generated within constraints on size, aspect ratio, and I/O port positions. Port positions can be optimized. Multiple transistor rows are supported. Transistors are interconnected using a technique we call "recursive goal-directed maze routing". This method increases routability and finds near-optimal compromises between new connections and reroutings of previous connections. The router is capable of giving priority to critical nets. It is easily extensible to handle any number of routing layers.

REFERENCES
MLG - A Case for Virtual Grid Symbolic Layout without Compaction

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Abstract

This paper describes a virtual grid symbolic layout technique for designing VLSI circuits. The technique allows circuit designers to lay out circuits using rules that are far simpler than typical technology design rules. The representation of circuits in a symbolic form simplifies the tasks of keeping up with changes in technology design rules and of mapping designs from one technology to another. The use of compactors for this purpose is well-known and has been widely described in the literature. The technique to be described here does not involve compactors. We attempt to show that virtually all the productivity advantages inherent to a virtual grid symbolic system can be realized without the computational overhead of compaction. The additional benefits that accrue are also described. Reference is made to a system that has been implemented and is currently being used for designing chips at IBM.

References

Metal-Metal Matrix (M$^3$) CMOS Cell Generator with Compaction

P. Gee, M. Y. Wu, S. M. Kang, I. N. Hajj
Coordinated Science Laboratory and Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign

Abstract

Two symbolic compaction methods are introduced for the Metal-Metal Matrix (M$^3$) layout for high-speed VLSI circuits in single-poly and double-metal technology. The first method achieves a high packing density by reordering the rows of the node incidence matrix $A_a$ to reduce the number of columns and then columns are rearranged to reduce the number of tracks in M$^3$. The second method is based on PLA folding techniques. The conventional row-foldability graph is extended so that parallel transistor groups can be assigned to different columns in the M$^3$ layout. These methods in conjunction with the switching network logic (SNL) approach can be used for design automation of high-speed VLSI circuits.

References

Average Interconnection Length Estimation for Random and Optimized Placements

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Abstract

We present models and algorithms for accurately estimating the average interconnection length for both random \( \bar{E}_r \) and optimized \( \bar{E}_o \) placement models were developed for multi-cell nets, where the interconnection length for a net is assumed to be one-half of the perimeter of its bounding box. An exact random placement model was developed under the assumption of uniform cell sizes. Furthermore, for nine industrial circuits with widely varying cell shapes and sizes, the random placement model yielded \( \bar{E}_r \), which were typically within five percent of the measured values. The optimized placement model was used to derive theoretical values of \( \rho = \bar{E}_o / \bar{E}_r \), the expected reduction in average interconnection length after an optimized placement of the cells. The theoretical values of \( \rho \) were typically within seven percent of the measured values. The predicted results were obtained strictly from an analysis of the net list, with no a priori knowledge of the functionality of the circuit.

References

A Study of Automatic Placement Strategies for Very Large Gate Array Designs

Thomas Payne, Robert Wells, Werner Gundel
Silvar-Lisco

Abstract

This paper presents the results of an experimental study of the relative effectiveness and performance of various placement strategies for placement of very large gate array designs. The placement strategies studied were Pairwise Interchange with netlength optimization, Min-Cut Placement, and Hierarchical Placement. The experiments consisted of placing and routing several large gate array designs using several placement strategies and comparing the results. In this paper, the example designs are described, each of the placement strategies used is described, and results of the experiments are presented.

References
Layer Assignment of Functional Chip Blocks for 3-D Hybrid IC Planning

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ABSTRACT

This paper proposes two algorithms - Growing Box Scheme (GBS) and Reducing Box Scheme (RBS) - for layer assignment of functional chip blocks in 3-dimensional hybrid IC physical planning. Both GBS and RBS are considered to be more suitable for 3-D electronic packaging applications such as 3-D hybrid IC and WSI, compared to the traditional circuit partitioning and clustering methods which are good mainly for basically 2-D packaging problems such as single chip floor planning or multiple PCB system. To reduce the computation time, we exploited such techniques as quadrant folding, incremental coordinate-transformation. A test run for a 4-layer assignment of 80-block, 50-net circuit takes about 10 minutes using VAX 11/780 from 3-D relaxation, layer assignment and 2-D floor planning in each layer.

REFERENCES

The Meyer Model Revisited: Explaining and Correcting the Charge Non-Conservation Problem

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Abstract

The intrinsic capacitive behavior of the MOS transistor has been the focus of much attention lately. This attention was sparked by the startling discovery that the widely-used "Meyer" capacitance model fails to obey the charge conservation law! This flaw in the Meyer model was correctly attributed to the use of capacitance, rather than charge, as the fundamental model quantity and several charge-based models were proposed to solve the problem. Unfortunately, the developers of these new models failed to separate the sound mathematical notion of using charge rather than capacitance from the physical assumptions underlying their models. Thus, while the new generation of models do conserve charge, a certain amount of confusion concerning the root cause of charge non-conservation in the Meyer model still lingers on, and the Meyer model continues to survive. In this paper we show that the charge non-conservation in the Meyer model is not due to any physical assumptions. Rather, it is caused by the mathematical error of characterizing a multi-dimensional function (the stored charge on the four terminals of a MOSFET) by an incomplete subset of its partial derivatives (the partial derivatives of the gate charge.) This conclusion is supported by developing and implementing a correct mathematical characterization of the MOS charges based on the same physical assumptions used in the Meyer model. One important outcome of this exercise is that the non-reciprocal nature of MOS capacitive coupling is evident even in a first-order physical model of the device.

References

On the Channel Charge Division in MOSFET Modelling

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Introduction

In the literature on MOS modelling several models have been proposed for the transient behaviour of intrinsic MOSFET's. These models are composed of a dc model and a charge model. In the first MOS model the charge behaviour was modelled by means of non-linear capacitors between gate and drain, gate and source and gate and bulk (Meyer, [1]). As is known, this model suffers from non conservation of charge. This problem can be overcome by modelling the charges themselves instead of modelling the capacitances (Ward and Dutton, [2]). In the modeling of the charges it is clear how the gate charge, the bulk charge and the channel charge should be determined because they are clearly located in the device. In a circuit simulation environment however, we need charges defined on the terminals of the device. The charge as present on the physical gate should be assigned to the gate terminal since that is the only terminal through which the amount of charge on the physical gate can be altered. In the depletion approximation the charge in the depletion layer below the gate can be assigned to the bulk terminal since that is the only terminal through which the depletion charge can be modified. The channel charge can be altered through both the drain and source terminals and should be divided between these two terminals. How this division is to be carried out can not be seen immediately. In the literature (Oh, Ward and Dutton, [3]) a method has been given which is based on the current-continuity principle when applied to the channel and which results in a weighting procedure. In this procedure the channel charge is weighted with a function which varies linearly with the position in the channel. Recently, (Fossum, Jeong and Veeraraghavan, [4]) an interpretation of this method in terms of transit delay and transient currents has been given.

In this paper a different course is taken. A partition of the channel charge is derived which is based on the differential conductances towards drain and source. These conductances are derived from the dc model. In this way the relation between the charge model and the dc model is made more explicit. Moreover, the conductance principle is easily generalized to more complex situations. For a particular case it is shown that this partition yields the same results as the partition based on the current-continuity principle.

References.
Efficient Modeling of Small-Geometry MOSFETs

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Abstract

In the device modeling spectrum, there exists a need for accurate yet efficient physically-based VLSI MOSFET models. Two such models are presented here, which predict device model parameters and I-V characteristics from the device doping and layout. A quasi-analytical model for the threshold voltage and associated body-bias dependence has been developed. This parameter-based approach to device modeling can be applied to circuit simulation, IC optimization and process monitoring. An efficient formulation of the current-voltage characteristics is also described. With its physical modeling approach, this method can be used to extract device model parameters or explore the internal operating conditions of the device. Both of these modeling techniques are useful in the development of circuit-level device models which more accurately reflect measured bias dependencies. A special focus of the work is the modeling of VLSI devices, i.e. devices with small geometries, nonuniformly-doped channels and/or lightly-doped source/drain regions.

References

Movie - an Interactive Environment for Silicon Compilation Tools

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Abstract

Movie is a special purpose environment for silicon compilation tools, providing services in the same way that an operating system does to application programs. An internal specification language has been developed that allows a combination of hierarchically parameterized module generators, symbolic layout, and interactive graphical editing. A set of instantiation mechanisms will ensure certain correctness of the result independently of the tools and close the design-verification loop. Movie has been designed to take advantage of fast color graphics, special purpose data structures and incremental updating to achieve interactivity with immediate visual feedback by real time animation. By integrating high-level tools, a hierarchy of levels of abstraction can be maintained. Silicon compilation systems based on Movie will be open-ended, transparent and highly interactive.

References
A Design Data Management System for CAD

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ABSTRACT

An efficient data management system is essential to the success of a VLSI CAD system. The process of chip design is evolutionary in nature. It involves refining existing designs, and redoing simulation and layout with different options before selecting one that satisfies the specifications. In order to do this in an organized fashion, the designer needs to maintain and store design data according to different activities and iterations, share data across activities and associate design files with the corresponding tasks. This paper describes two simple mechanisms, viz. Design States and Design File Tracking, that we have developed for providing the designer with the above functionality. Design States provide the designer with a comprehensive design version and data management scheme. The Design File Tracking mechanism keeps track of the relationship of design files with the tasks that generated them and provides the designer with a set of suitable commands to query the history of the design process. Circuit designers have started using the Design Data Management System (DMS) in their designs and this system has enabled them to produce correct designs efficiently and easily.

REFERENCES

ABSTRACT

In this paper we present an automated methodology called the Virtual Gate Array (VGA) that is intended to provide a fast turnaround, high quality design capability for standard cell design. An initial implementation of this methodology was realized using IDEAS, which is a system that provides mechanisms for the description, control, documentation and automation of a design process. VGA automates the design of low complexity, synchronous standard cell chips. We have implemented a generic process for this class of designs as a Design Thread in IDEAS and have developed a Process Specification Agent to allow customization of the process for dealing with the requirements of a specific design. All the customization information is provided by the designer only once and is reused, thereby minimizing design errors.

We have run several encouraging experiments with IDEAS that demonstrate the effectiveness of these concepts in a production IC design environment. We detail this work and our plans for future development in the paper.

References

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Increased Throughput for the Testing and Repair of RAMs with Redundancy

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Abstract

We consider algorithms for the problem of determining whether a redundant random-access memory (RRAM) containing faulty memory cells can be repaired with spare rows and columns. We argue that the focus should be on increasing the number of working chips manufactured per unit time, rather than per wafer and we present two on-line algorithms that can detect unrepairable RRAMs during memory testing and hence abort unnecessary testing or find a suitable repair if one exists.

References
On the Repair of Defective Field Programmable Logic Arrays to Increase Yield

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Newly manufactured Field Programmable Logic Arrays (FPLA) often contain crosspoint defects. Due to the inherent sparsity (absence of devices at crosspoints) of PLAs, it is highly probable that certain types of faults within the unprogrammed FPLAs can be masked out without any additional hardware, leading to the reclaim of the previously discarded chips. In this paper, we first discuss a technique to locate the faults within an unprogrammed FPLA. We then present a new technique to program the FPLA around these faults. Our approach is new in that the programming of an FPLA is formulated as a matrix problem to obtain a polynomial time solution. Computer studies have shown that FPLAs with even a large number of defects can successfully be repaired, thereby increasing the yield.

References
The Design of Fault Tolerant Arrays of Integer Arithmetic Multipliers

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ABSTRACT

We consider the design of fault secure and fault masking processor arrays composed of N integer arithmetic multipliers. We derive totally self checking circuits (TSCC) for a high level multiplier fault model that can be used for concurrent error detection (CED), error location, or error correction. This analysis and design methodology can be the basis for compiler/module generation systems for special purpose TSCC. Since general techniques lead to hardware or time overheads, \( \mu \), greater than one, we use the method of Algorithm Based Fault Tolerance (ABFT) [1] [2]. We show that only distance two (\( d = 2 \)) checksum codes achieve \( \mu < 1 \). We propose \( v \)-dimensional checksum codes of distance \( d' = 2^v \), which reduce the probability of undetected errors from \( N \rho \) for an unprotected array to \( N^2 \rho^{2v}/2^v \) for an array with \( \mu \approx vN^{-1/v} \). By checking implicit scalar vector products we extend ABFT to algorithms for banded matrices and also reduce the error rate for matrix products. We find improved architectures for: linear filtering, linear transformations, matrix products, and many others.

References

Effect of Byzantine Hardware Faults on Concurrent Error Checking

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ABSTRACT

A new fault model for temporary failures is presented. This model is motivated and supported by recent experimental studies on a type of temporary failure which cannot be explained by existing models. This new fault is called a Byzantine fault in analogy with the well-known Byzantine Generals Problem in distributed systems. Effects of Byzantine faults on concurrent error checking circuits are discussed. Design techniques to eliminate the effects of Byzantine faults are presented.

REFERENCES

A Deep Decision Tree Approach to Modeling Submicron Silicon Technologies

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ABSTRACT

A robust, accurate process simulator, PREDICT 1.1\textsuperscript{TM}, has been written which is based on tightly coupled simulation models. Model coupling is accounted for by using an internal decision tree that activates models based upon prior wafer processing. Thus, residual damage or dopants created by previous steps are accounted for and are important in the selection of appropriate process models. Submicron technology modeling demands this kind of attention to detail with crystal damage being the major new process variable. Activated damage removal is calculated during the simulation so that self-interstitial-rich or vacancy-rich regions can be monitored for their impact on dopant diffusion.

The PREDICT\textsuperscript{TM} program (PRocess Estimator for the Design of Integrated Circuit Technologies) is a robust design tool based on tightly coupled simulation models [1]. The goal in developing PREDICT was to couple physical models together, verify the coupling with a large measured data base, and reduce the need for model parameter adjustment by the user. In other words, the models are "hardwired" into the program as material specific and physically accurate. This approach is diagrammed in Fig. 1 and compared with the approach used in SUPREM.

REFERENCES
Modeling and Simulation of Hot Electron Effects for VLSI Reliability

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ABSTRACT

This paper presents a new method for simulating the threshold voltage shift in MOS transistors due to hot electron effects. The method is based on Avalanche Electron Injection (AEI) and Fowler-Nordheim Tunneling Electron Injection (FN-TEI) models. It employs an empirical relationship between the injected and the trapped charge densities in the gate oxide and takes into account the localized charge trapping. The effect of circuit configuration on transistor aging is also investigated to provide a guideline for the VLSI design-for-reliability. A simple recursive formula is derived for inverter circuits to estimate the threshold voltage shift and thus the circuit failure time without extensive circuit simulation.

REFERENCES
HOTRON - A Circuit Hot Electron Effect Simulator

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ABSTRACT

Hot electron effects resulting from high electric fields in typical VLSI MOSFET's can severely degrade device characteristics. Threshold voltage shifts and reduced current drive capability are typical. As a result, severe performance degradation can occur at the circuit level. This paper discusses a method which predicts circuit level performance degradation and can identify which devices are responsible for the degradation. Two components of performance degradation have been identified and these are the amount of stress each device is subjected to, and the sensitivity of circuit performance on the degradation of the individual devices. A heavily stressed device will itself be degraded but may not cause any performance degradation in the circuit; conversely, a mildly stressed device may cause much performance degradation due to circuit sensitivity. This effect is demonstrated with a real example in the paper. The simulator has proved very useful in understanding when hot electron problems will occur and how they effect actual performance.

References
Reevaluating the Design Space for Register-Transfer Hardware Synthesis

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ABSTRACT

This paper describes an experiment that challenges the conventional formulation of register-transfer level hardware synthesis. RT-level synthesis is typically viewed as a translation from a functional specification to a set of interconnected modules plus a control sequencer to drive those modules. The cost of a design is taken to be either the number of modules used or the sum of the costs of the individual modules. This view is inadequate when the target technology is VLSI because it ignores interconnect and other factors related to layout, which have a significant effect on the cost of the hardware. The experiment described here shows that including these layout-related factors results in a very different evaluation of the possible designs for a given functional specification and often leads to different design choices in synthesis.

REFERENCES

Allocation of Multi-Port Memories in Data Path Synthesis

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Abstract

All the present data path synthesis techniques produce a design with a large number of single isolated registers. In most synthesis systems, allocation of memory modules (or register file) to implement these registers is left to the designer, whereas in CMU-DA a single-port memory is allocated for registers with disjoint access requirements. This paper presents an algorithm to synthesize registers using multi-port memories during data path synthesis. The proposed approach not only considers the access requirements of registers but also their interconnection to operators in order to minimize required interconnections. The same approach can be applied to select optimum number of buses in a multi-bus architecture. The method is illustrated with an example.

References
Automatic Synthesis of Data Paths based on the Path-Search Algorithm

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ABSTRACT

An efficient method to synthesize data-paths of digital system from behavioral description is presented. This method is based on a path-search algorithm that finds a set of compatible variable groups (CVG's) which are existing along the paths in the modified data-dependency graph (MDDG). For each CVG, the single memory component can be assigned to all elements of that group to store their values without resource conflicts among those elements when it will be implemented with real hardware. By applying the path-search algorithm to input code sequences of behavioral description we can deal effectively the inter-communication problems between closely coupled synthesis phases. This algorithm allows an efficient allocation of resources for data paths of digital systems and reduces exploration of the search-space of the synthesis process extensively. A design example for this procedure is shown.

REFERENCES

Synthesis and Optimization of Interface Transducer Logic

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ABSTRACT

The automatic synthesis of interface transducers, the logic circuitry that connects the interface of a custom chip to that of a system bus, is important to the rapid integration of custom chips into computer systems. In general, a transducer includes both synchronous and asynchronous components and must satisfy the timing constraints of both interfaces. This paper describes the synthesis and optimization algorithms used in Janus, an interface transducer generator. A methodology, based on formalized timing diagrams, is used for the abstract specification of interfaces. The synthesis algorithms transform event graphs derived from the timing diagrams into a logic specification for the transducer. The circuitry is then optimized using cross-operation merging and multi-level logic minimization. A practical example demonstrates that the synthesized circuitry is comparable in performance and size to human-generated designs.

References

Test Generation for Embedded PLA's

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Abstract

This paper presents a conditional stuck-at fault model in a two-level gate model of PLA's to show that all single stuck-at faults, single cross-point faults, and single bridging faults in a PLA can be covered by this new fault model. In the new model each stuck-at fault on a line might have associated with it a condition which requires that a test pattern for this fault should, in addition to testing this fault, produce a specific binary value on another specified line in the gate model. Our results therefore allow one to solve the problem of test generation for PLAs by using the classical stuck-at ATPG tools and without any additional gates in the model. Moreover, our results will enable one to generate tests for embedded PLAs without requiring any additional controllability/observability or built-in self-test schemes. Some simulation results are included to demonstrate the viability of the conditional stuck-at fault model.

References

An Automatic Test Pattern Generator for the Detection of Path Delay Faults

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Abstract

Details of an implementation of a test pattern generator of robust tests to detect path delay faults in combinational logic circuits and results of experiments run on ten example circuits are given. A new class of tests called validatable non-robust test are defined that allow reliable detection of some path delay faults for which robust fault-detecting tests do not exist. The extended fault coverage provided by these non-robust tests is used to develop procedures to design path delay fault testable two-level logic circuits.

References
Test Generation for Sequential Finite State Machines

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Abstract

We present a novel approach to test pattern generation for synchronous sequential finite state machines. Our approach involves first extracting part of the State Transition Graph (STG) of the finite state machine, a Moore or a Mealy machine, using purely structural information, i.e. the gate-level description of the sequential circuit. The construction of the partial STG is based on an efficient state-enumeration algorithm that aims at finding paths from the reset state to different valid states (states reachable from the reset state) in the STG. For circuits with relatively few states, a partial STG including all the valid states is built. For circuits with a large number of states, only a subset of states is included in the partial STG. We show how test sequences for line stuck-at faults can be efficiently generated using the partial STG in conjunction with fault excitation-and-propagation and state justification algorithms based on the concept of state enumeration. We have successfully generated tests for finite state machines with a large number of states using reasonable amounts of CPU time and obtained close to maximum possible fault coverages.

REFERENCES


Knowledge Based Test Generation for VLSI Circuits

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Abstract

Test generation for a VLSI circuit is a complex problem. Previous attempts to use hierarchical representations have not been able solve the complexity problem in search, and they have been unable to use appropriate knowledge embedded in the hierarchical design of the circuit. This paper introduces an algorithm for test generation which differs from previous approaches in two ways: (1) The hierarchical representation of the circuit stores the knowledge of how to backtrace and propagate signals through a component of the circuit. This permits us to fully exploit the hierarchical structure of the device to reduce the search space, and (2) The components and their interconnections are separated into data and control types, and the algorithm uses different heuristics to propagate and backtrace faults in the control and data components and thus reduces the search space.

Keywords: Test generation, Knowledge based system, hierarchical, propagation, backtracing.

References

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LARC2: A Space-Efficient Design Rule Checker

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ABSTRACT

LARC2 is a new mask level design rule checker for integrated circuits. Evolved from GOALIE, it is both space and time efficient and has powerful features to perform complex (conditional and conjunctive) design rule checking. It outperforms its predecessor LARC significantly in speed (14 times faster), disk usage (65% less), and memory requirement (94% less) for VLSI layouts of current interest.

REFERENCES

The Multiple Storage Radix Hash Tree: An Improved Region Query Data Structure

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Abstract

This paper describes a region query data structure with improved performance characteristics when compared to other recently developed structures such as the Multiple Storage Quad Tree and the Multi-dimensional Binary of K-d Tree. For VLSI CAD tool applications, in which fast region query is essential, the Multiple Storage Radix Hash Tree offers improved performance by significantly reducing tree scan overhead. Both theoretical and experimental performance data on retrieval time and memory utilization are provided. The data structure and supporting algorithms are well suited for design viewing, design rule checking, cell compaction, circuit connectivity extraction, and circuit extraction.

References
Functional Recognition of Static CMOS Circuits

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Abstract

Recognizing logic components of a VLSI circuit is a crucial step toward symbolic circuit verification. A new method for recognizing the functionality of logic components such as gates and flip-flops in a static CMOS circuit is proposed. Based on novel logical circuit expressions and functional expansions, this approach can be applied to various static CMOS logic families, such as fully complementary CMOS, pseudo-nMOS, pass transistor logic, and DCVS structures. In addition to combinational circuits, static sequential elements can also be recognized.

REFERENCES
Efficient Circuit Re-extraction For Yield Simulation Applications

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Abstract

This paper presents a methodology for efficient circuit re-extraction of process deformed layouts for yield simulation applications. Our methodology has been implemented in a software tool called PRICE. PRICE performs a circuit extraction of only those layout regions where topological circuit changes have occurred using the technology independent circuit extractor ENTICE. When no topological circuit changes are present, the layout dimensions are adjusted to account for the disturbances. We present several results from PRICE used in a yield simulation environment.

References

Don't Care Conditions in Top Down Synthesis

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Abstract

In this paper we present a theory of don't care conditions in a recursive top down synthesis paradigm. These conditions expand upon the work presented in [BBH86] in two ways. First, we clearly discuss the types of don't cares that can be extracted from a behavioral model. Second, we develop a top down recursive synthesis paradigm and discuss the propagation of don't cares through the top down synthesis process. Third, because it is sometimes important to combine, at a lower level, components with don't cares, we discuss the bottom up combination of system components with specified don't cares and present conditions under which they make sense in terms of model consistency and correctness. Finally, we describe a mechanism of minimizing subnetworks of large combinational logic networks, which might, as a whole, be too large to minimize in one piece.

In addition to the theoretical developments concerning the hierarchical don't cares we present an algorithm for verifying a model at one level in the hierarchy with that at the next level in the synthesis process. We term this behavioral verification.

References

Column Compaction and Its Application To The Control Path Synthesis

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Abstract

The idea of column compaction on the cubical representation of a combinational logic function is presented. The problem of column compaction with don't-cares can be related to the problem of maximum clique partitioning and is NP-complete. Column compaction has a more profound impact on the area of logic implementation, particularly PLA, than row and literal minimization which are the goals of most logic minimization programs. It is most useful when there exists extensive output don't-cares. We present a method for full column compaction, i.e., a column can be inverted if doing so will increase compaction. We also apply column compaction to control path synthesis in a high-level synthesis environment and describe techniques for maximal extraction of output don't-cares for a control path. Experimental data are presented and show a substantial reduction in the number of control output lines.

REFERENCES

Partitioning Before Logic Synthesis

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ABSTRACT

Two algorithms for the partition of combinational logic are presented. They are based on clustering of operations. The second algorithm considers also semantic information from a behavioral specification. It is shown that for small designs partitioning allows to effectively trade logic synthesis time for size of the resulting circuits. Both algorithms produce similar results. For the large circuits exercised so far, partitioning before logic synthesis produces results not worse than logic synthesis of the unpartitioned circuit, using less computer time. In this case taking into account semantic information from a behavioral specification greatly improves the results.

REFERENCES
Combined Synthesis of Control Logic and Data Path

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ABSTRACT

In the Yorktown Silicon Compiler, a new approach is chosen for the generation and implementation of control logic. A Boolean specification describes the control as a collection of small blocks, distributed between and indistinguishable from the data path logic. Multi-stage logic synthesis minimizes the control and the data path together producing a highly compact result.

REFERENCES
Efficient Scan Path Testing Using Sliding Parity Response Compaction

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ABSTRACT

This paper describes a new linear response compaction technique, called Sliding Parity Response Compaction (SPRC), that has various testing applications in scan designs. SPRC requires a small area overhead to implement and has no impact on the operational speed of scan designs. SPRC can reduce the amount of response data that needs to be stored by a factor of m, where m is the number of outputs of the Circuit Under Test (CUT). In situations where the rate of generating new test vectors is faster than that of scanning the response out serially, using SPRC can potentially reduce test time by a factor of m. The aliasing probability of the new structure, using the standard error model, is \( \approx 2^{-\left(kT+m-k\right)} \), where T is the number of test vectors applied to the CUT and 1/k is the test vectors application rate in vectors/clock cycle. For typical values of T, k and m, this probability is infinitesimal. Applications of SPRC in deterministic testing scan environments as well as in pseudo random or pseudo exhaustive (LFSR-based) self-testing scan environments are described.

References
Concurrent Comparative Testing Using Bist Resources

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ABSTRACT

A method for the testing of a digital circuit concurrently with normal operation is presented. In our approach the built-in self-test resources ordinarily inserted in the circuit for off-line testing are modified and used in comparison mode to perform the concurrent on-line testing. A technique is given for computing the length of time required to concurrently test a circuit when the off-line testing method consists of exhaustive tests. A number of alternative approaches for reducing the testing time are identified and the design of a concurrent comparative tester introduced.

References
Improving Memory Subsystem Availability Using BIST

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Abstract

A strategy that increases system availability by delaying the repair process of a memory system that supports error correcting codes (ECC) and BIST in its memory chips is presented. This strategy uses the on-chip BIST to convey to the system some additional information about the faults in the memory chip. Based on this information and the capability of the error correcting codes, the system can decide whether an immediate replacement of the faulty chip is necessary, or the repair process can be delayed and done at some convenient time, thus reducing the down time of the system.

Bibliography
Floorplanning by Annealing on a Hypercube Multiprocessor

Rajeev Jayaraman, Rob A. Rutenbar
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Abstract

This paper describes the design, parallel implementation and performance evaluation of annealing-based floorplanning algorithms on a hypercube multiprocessor. New partitioning strategies are developed to efficiently map an annealing algorithm onto a hypercube topology. Because the state of the evolving floorplan configuration is distributed across the processors of the hypercube, updating the views of this global system state seen by individual processors requires expensive interprocessor message traffic. Hence, we tolerate errors in these locally held views of the system state to reduce the frequency of expensive global updates. We introduce new parallel state updating schemes that permit fast partial updates to be interleaved with expensive, complete updates. Results from experiments on an Intel iPSC hypercube show relative speedups between 4 and 7.5 for 16 processors, with solutions of comparable quality to those produced by a serial version of the floorplanner.

References

Placement of Standard Cells Using Simulated Annealing on the Connection Machine

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Abstract

A Simulated Annealing algorithm for the placement of standard-cells is proposed on a massively parallel computer, the Connection Machine. The parallel algorithm is compared to the sequential version implemented in the program "TimberWolf". Experimental results are presented.

References

Concurrent ESP (Evolution-based Standard cell Placement) is a program package designed to perform standard cell placement. It uses the new heuristic method of simulating an evolutionary process in order to minimize the cell interconnection wire length. The program is designed to run on a network of loosely coupled processors such as workstations connected via ETHERNET. The workload partitioning and job scheduling algorithms are adapted to the host system characteristics to minimize the computational and communication overheads. For medium to large circuits (> 250 cells per processor), linear speedup is achieved and the quality of the resulting placement is as good as in the uniprocessor case. In general, the quality of the resulting placement is comparable to results obtained from Simulated Annealing (SA) algorithms.

REFERENCES
Abstract

As greater numbers of processors are applied to a problem, the algorithm used must have sufficient parallelism if continued reductions in run times are to be achieved. In this paper, the performance of waveform relaxation for the simulation of digital MOS circuits on multiprocessors is investigated. The extra parallelism of the Gauss-Jacobi method is shown to result in faster run times than the Gauss-Seidel method when sufficiently many processors are used. A simple speedup estimation formula is given to select between the two methods for a given number of processors and a given circuit. The time-point pipelining approach is generalized and applied to the Gauss-Jacobi method to produce a highly parallel algorithm in which all subcircuits in all iterations can be solved concurrently.

References

A Multiprocessor System for Modular Circuit Simulation

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Abstract

A multiprocessor system dedicated to large scale integrated circuit simulation is described. The hierarchical modular simulation algorithm based on the tearing decomposition preserves simulation reliabilities and promises full parallelism both in the input-linkage phase and in the simulation phase, making it possible to incorporate the algorithm into a multiprocessor system quite naturally. The prototype system consists of four MC68020's (12.5MHZ) equipped with floating point processor MC68881 and 4 MB of memory. For the prototype four processor system, a speed up of 3.3 has been attained for the input phase, and a speed up of 3.9 for the actual simulation phase. In order to study the feasibility of realizing a larger multiprocessor system, the relationship between the size of the serial tasks on the interconnection network and the number of subcircuits has been investigated. The results give rises to the strategies for the product system design aiming at gaining high parallelism even for fine data granularities.

References

SUPPLE: Simulator Utilizing Parallel Processing and Latency Exploitation

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ABSTRACT

A new program, SUPPLE, has been developed for enhanced performance in the simulation of digital, memory, and analog integrated circuit designs: no circuit restrictions are required for either accuracy or convergence. SUPPLE utilizes a direct simulation algorithm with local time step control which takes advantage of time domain latency to reduce the simulation time by 5 to 10X relative to SPICE. This is achieved without the use of relaxation approaches and thus is applicable to general classes of circuits. Overall speed advantages of 10X over SPICE have been demonstrated on a uniprocessor system. The algorithm is structured to take advantage of parallel processing. Over 90% processor utilization has been obtained for a four processor system. Overall speed advantages of 30X SPICE have been demonstrated.

REFERENCES
A Contour-Based Variable-Width Gridless Channel Router

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ABSTRACT

A new channel routing algorithm is presented in which the grid-based routing framework that most channel routers use is replaced by a set of contours. For each of the three interconnection layers, a separate contour covers the previously laid wires. A new wire is bend around the contour at a minimum distance. In this way spacing constraints are satisfied and a dense packing of variable width wires can be achieved. Within certain limitations, the contour-based routing framework allows horizontal as well as vertical wire segments in all layers. This enables the algorithm to avoid most 'vertical constraints' and to reduce the number of vias drastically. The algorithm, which has been coded in C, is now in use in two routing systems. Very competitive results have been achieved for uniform- as well as variable-wire width channels. The well known benchmark channel "Deutsch's difficult example" was routed using only 263 vias and in 15.1 to 20.4 tracks, depending on the design rules used.

REFERENCES
A New Approach to the Three Layer Channel Routing Problem

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Abstract

We present in this paper a new approach to the three layer channel routing problem. Since the two layer channel routing problem has been studied extensively, there are several two layer routers which can produce optimal or near optimal solution for almost all the practical problems. We develop a general technique which transforms a two layer routing solution systematically into a three layer routing solution. The solution transformation approach is different from previous approaches for three layer and multi-layer channel routing. Our router performs well in comparison with other three layer channel routers. In particular, it provides a 10-track solution for the famous Deutsch's difficult example and thus achieves its theoretical lower bound. We also extend our approach to four layer channel routing. Given any two layer channel routing solution without unrestricted dogleg that uses w tracks, our router can provably obtain a four layer routing solution using no more than $\lceil w/2 \rceil$ tracks.

REFERENCES
A New Three-Layer Detailed Router For VLSI Layout

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ABSTRACT

This paper presents a 3-layer detailed router which is capable of routing a rectilinear wiring area containing obstacles such as prerouted pins. It supports pins fixed on all sides of the area. A new routing methodology is developed, it is basically a divide-and-conquer which partitions routing area into subones by specially chosen cut lines, then uses concurrently bidirectional column scanning approach to route each subregion. In each column, a signal column maze router with backtracking is developed. This router consistently outperforms several known routers in quality of wiring. For example, it found an 10-row solution for the 3-layer Deutsch's difficult example, whereas all other known routers required 11 or more rows. For 2-layer Burstein's difficult switch-box unusing the rightmost column (the third layer is set as an obstacle) the router routed it with 100% routability. It also routed 2-layer Deutsch's difficult example in density.

REFERENCES
DRAFT: An Efficient Area Router Based on Global Analysis

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ABSTRACT

A new area router -- DRAFT is presented. Based on a global optimal analysis of nets, DRAFT is capable of routing switchboxes and channels. It partitions the detailed routing into two steps: directional routing and final routing. Directional routing functions as a loose routing in the routing area, evaluates the ideal position of each net. Its results will guide the final routing procedure. Final routing actually routes the area. DRAFT is a grid-based router using two interconnection layers, it relaxes the unnecessary constraints of assigning different layers to different directions. Experimental results are quite encouraging, optimal results are obtained in most cases for both switchbox and channel routing in published literatures.

References
**Incremental Functional Simulation of Digital Circuits**

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**Abstract**

Simulation is one of most effective tools for functional verification of hardware design. In an effort to speed up the simulation of hardware design, a new simulation algorithm, incremental simulation, is proposed. Incremental simulation implies a simulator that runs in time proportional to the size and implications of design changes instead of the size of the circuit under simulation. Directed by net change tokens, incremental simulation evaluates the circuit components affected directly or indirectly by design changes, using the information generated during previous simulation to reduce the number of evaluations over the entire design to a minimum.

This presentation describes the design and implementation of the incremental algorithm for functional/behavioral simulation of digital circuits, which substantially improves the run-time performance over existing simulators by exploiting the incrementalness of the hardware design process.

**References**

A New Implementation Technique for the Simulation of Mixed (Digital-Analog) VLSI Circuits.

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ABSTRACT

To accomplish the desired trade off between accuracy and cost in the simulation of VLSI circuits and to simulate the mixed analog-digital circuits the mixed-mode simulator is essential. In this paper a new simplified technique for efficient simulation of VLSI circuits is described. This technique is based on the direct interface of functional and electrical analysis in the same simulation environment, which is electrical to ensure a simple and accurate interface between the two types of analysis. The performance of our simulator allowed us to simulate accurately large mixed analog-digital circuits.

REFERENCES

**SISYPHUS -- An Environment for Simulation**

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**Abstract**

Sisyphus is a mixed-mode, hierarchical simulation environment for VLSI circuits. Sisyphus develops a new hierarchical, typed wire model based on translators, which facilitates the accurate simulation of incompletely specified designs. Sisyphus provides an event-based simulation kernel which supports a wide range of simulation algorithms, including: Iterated Timing Analysis, Mossim, ELogic, gate-level, and behavioral modelling. In essence, Sisyphus provides a testbed for new simulation algorithms.

**References**


The Complexity of Accurate Logic Simulation

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Abstract

The complexity of logic simulation is popularly supposed to be close to a linear function of the number of gates in a circuit. However, "unknown" values are necessary in a logic simulation to define the uninitialized states for sequential devices and also for the detection of races and hazards. This paper shows that it is an NP-complete problem to accurately simulate a circuit with the existence of unknown values. Also, it is demonstrated that current gate-level simulators cannot handle unknown propagation properly, causing pessimistic results. A set of algorithms, based on high-level descriptions of functions, has been developed for accurate logic simulation. Experiments on large benchmark functions show the advantage of using high-level descriptions, and provide empirical rules for when approximate simulation would provide satisfactory results.

REFERENCES
An Efficient Design Correctness Checker Of Finite State Machines

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Abstract

In the hierarchical design/verification paradigm, the submodules of lower levels of abstraction are often finite state machines. In this case, the verification problem is to check the correctness of the design with respect to the specification rather than to check the equivalence of two machines. Most previous work for finite state machine verification deals with equivalence checking and few of these techniques have been widely used due to their low efficiency. In this paper, an efficient algorithm for the verification of the design correctness of finite state machines is presented. The experimental results show that the approach is promising in terms of speed.

References
A Verifier Tightly Connected to Synthesis Expert System

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Abstract

A verifier which is tightly connected to the synthesis expert system, DDL/SX, was developed to check the logical equivalence of designs before and after changes. As DDL/SX cannot completely handle timing problems such as critical-path problems, designers must sometimes change the synthesis results for delay correction and logical errors may occur in design. When modifying circuit, designers often change the logic of only a small number of nets, leaving other nets unaffected. Our verification algorithm first filters out the unchanged nets, then verifies the logical equivalence of the modified net only. This reduces verification time and enables us larger hardware to be processed. This paper tells how management data is incorporated for verification, explains filtering and the comparison algorithm, and presents some experimental results.

References

VAL: An Annotation Language For VHDL

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Abstract

VAL (VHDL Annotation Language) uses a small number of unique language constructs to annotate VHDL hardware descriptions. VAL annotations added to the VHDL entity interface in the form of formal comments express intended behavior common to all architectural bodies of the entity. Annotations are expressed as parallel processes that accept streams of input signals and generate constraints on output streams. VAL views signals as streams of values ordered by time. Generalized timing expressions allow the designer to refer to relative points on a stream. No concept of preemptive delayed assignment or inertial delay are needed when referring to different relative points in time on a stream. The VAL abstract state model realizes history dependent device behavior. The VAL Transformer translates VAL formal annotations into VHDL code permitting automatic checking of the VHDL simulation. VAL also provides a basis for applying mathematical consistency proofs to VHDL architectural descriptions.

References
Abstract

This paper presents a class of parallel algorithms for answering the tautology question for Boolean Networks (defined in [6]). The members of this algorithm class are characterized by whether the Boolean network is single level (PLA case) or multilevel (random) logic, and by the algorithm used to assign computational work to the individual processors (static or dynamic scheduling). All algorithms presented in this paper derive from a single algorithm frame, derived as discussed in [5] from the tautology algorithm presented in [2]. The work required by this algorithm to answer the tautology question in a multiprocessor environment is recursively bipartitioned and assigned to the available processors. The results from the implementation on a network of Sun 3 workstations, on an Encore Multi-Max multiprocessor and on an Intel hypercube computer are presented. A model for predicting speedups in a general divide and conquer setting, is developed, which includes communication delays and start up costs of the host multiprocessor system. This model accurately predicts speedups for problems with balanced recursion trees and can be used to characterize the parallelization potential of the host systems. For the specific context of Boolean tautology checking, this model can be used to show that unit parallel efficiency (i.e., linear speedup) is indeed possible, but that parallel efficiency is limited in the PLA case by tree imbalance and by size. In the multilevel case similar difficulties occur but can be overcome for a significant problem class by an appropriate dynamic processor scheduling algorithm.

References

ABSTRACT

This contribution presents a software system for the automatic generation of layout modules of medium complexity from multi-level logic expressions. The basic building blocks of the system are given by automatically generated combinational or sequential cells that are assembled in a hierarchical, top-down fashion. A new algorithm based on the PQ-tree algorithm for graph planarity testing calculates the gate order for every cell such that cells may be connected by abutment. The system has been implemented in LISP and OPS5. Designs of medium complexity (several hundred transistors) can be generated in a reasonable amount of CPU time.

References
A Method to Reduce the Surrounding Area of PLA Layouts

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ABSTRACT

A new method which reduces significantly the layout area in PLA-based designs is described. The basic idea is to replace the empty positions of the PLA personality matrix by wires transforming the the AND/OR plane into a cell-wire plane. Since cells are much wider than wires, the rows will be individually compacted and have different lengths. However, a routing scheme is required to connect the PLA because the connecting column lines are no longer parallel. The major contribution of this project is to develop an efficient channel routing scheme to effect these surrounding connections. The scheme has been evaluated using numerous examples and it achieves substantial compaction even when the original PLA density is greater than 50%. The scheme has been also compared to other PLA reduction techniques, with significant success.
A New Module Generator with Structural Routers and a Graphical Interface

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Abstract

This paper presents a new module generator for generating functional modules with structural regularity. Unlike most module generators, which are only able to place cells, the proposed generator can generate functional modules with structural routers for regular-structure layouts. Graphical layout description tools used to describe correct layout structure easily on graphic displays are also proposed. Experimental results show that several modules, such as Multipliers and RAMs, are generated in a very short time with the same performance as fully manually designed layouts.

References

A Parallel 3-D Poisson Solver on a Hypercube Multiprocessor

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ABSTRACT

A parallel Poisson solver for three dimensional semiconductor structures has been developed on an Intel iPSC/MX™ hypercube multiprocessor. The assembly of the finite difference equations is done by cubes which allows easy incorporation of non-planar structures and near perfect parallel speedup. A concurrent implementation of the Incomplete Cholesky Preconditioned Conjugate Gradient (ICCG) algorithm is presented and shown to offer greater throughput than concurrent Gaussian elimination. An overall speedup of 9.8 has been achieved with 16 processors. The solution time for an example with 132651 variables is approximately 27 minutes.

References
Three-Dimensional Capacitance Evaluation on a Connection Machine

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Abstract

Accurate capacitance evaluation is necessary to predict the performance of integrated circuits. Since analytical techniques are not satisfactory for minimal feature wires in the micrometer range, a numerical approach is needed. Depending on the complexity of the domain where the simulation has to be performed, a three-dimensional approach may be essential in order to model the properties of the interconnections. However, the computational cost associated with this numerical problem can be very large, if the simulation has to be performed on serial architectures.

For this reason, we propose an algorithm for 3-dimensional capacitance evaluation suitable for parallel computers and describe its implementation on a massively parallel architecture: the Connection Machine. Experimental results show that this approach allows fast and efficient solution for this type of problems.

References
Learning Selection Rules in a Circuit Redesign Environment

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Abstract

The paper presents a learning component which is incorporated into TLTS, a knowledge-based tool that is used for the evaluation and redesign of printed circuit boards that have signal integrity problems. The component learns knowledge for selecting between different solutions to a signal integrity problem. It does this by recording and analyzing: the knowledge that TLTS uses when it identifies a signal integrity problem and its causes, the constraints that the user places on the pc boards, and the choices the user makes during the redesign phase. The learning component can also partially solve the problem of acquiring new solutions to signal integrity problems. In doing so it records the plans that the user constructs during the redesign phase. These plans can later be chosen by the user and replayed by TLTS. The paper discusses how problem solving knowledge is recorded as well as the methods for forming, using, and modifying selection rules. It also discusses our work to date on the area of capturing new solutions.

References
A New Knowledge Based Approach to Circuit Design

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Abstract

This paper proposes a new knowledge-based approach to VLSI circuit design. Given a set of circuit specifications, the proposed system, called Expert Essence, determines the most appropriate circuit-block among various alternatives. Differing from the conventional knowledge-based approaches, Expert Essence interprets design rules in a flexible way. The system automatically relieves given constraints and assumes a set of additional conditions unless a feasible solution is found. The proposed system carries out an intelligent circuit design, while maintaining "design trade-off" and "additional conditions" through the design process. Experimental results showed that the proposed system is quite applicable to assisting VLSI circuit design.

References

Modified Sequential CMOS Circuit Design

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Abstract

A modified circuit design is introduced in this paper, which will reduce the number of MOSFETs of sequential CMOS circuits. Based on the short-cut method and the switching network logic (SNL) design, a new method is developed to design such kind of circuits, which can be applied to both asynchronous and synchronous circuits.

References

On the Mincut Bipartite Arrangement Problem

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Abstract

The placement problem that minimizes the channel density in the standard cell (polycell) layout is considered. This problem is formalized as a mincut arrangement problem for a given bipartite graph $G = (A,B,E)$, where the vertices of $A$ and $B$ are placed on two different rows. We show that this problem is NP-hard even when the positions of the vertices in $A$ are fixed. In this restricted version, an $O(n \log n)$ optimal algorithm is given for 3-regular bipartite graphs. We also give a 3-approximation algorithm for regular bipartite graphs, i.e., an algorithm whose answer is guaranteed not to be more than a factor of 3 of the optimal solution, and a $(d+1)$-approximation algorithm for bipartite graphs with degree at most $d$.

Only results are stated in this summary, proofs of the theorems are provided in the full version of the paper [BL].

References


Improvements of A Mincut Partition Algorithm

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ABSTRACT

The performance of Kernighan-Lin-Fiduccia-Mattheyses (KLFM) partition improvement algorithm is erratic. An effective partition procedure is the selection of the best partition among the many partitions resulted by applying KLFM to many randomly generated starting partitions. A procedure is proposed to compute the minimum number of randomly generated starting partitions required to achieve a given level of confidence and optimality. A clustering algorithm based on Rent rule is proposed. This technique improves the quality of the partition and reduces the run time significantly.

REFERENCES
Quadrisection: A New Approach to Standard Cell Layout

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Abstract

Min Cut Bisection has been extensively used as a placement methodology for VLSI circuits. However, it suffers from the disadvantage that it essentially adopts a one-dimensional approach to a two-dimensional problem. In this paper we describe a two dimensional partitioning approach to placement and routing called Quadrisection. The method combines the placement and routing stages by constructing the connection trees for routing, during placement. Placement and tree construction are done hierarchically. A linear time heuristic for min cut quadrisection is presented. Results compare favorably with the simulated annealing code Timber Wolf.

References
An Improved Simulated Annealing Algorithm for Row-Based Placement

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Abstract

An improved simulated annealing algorithm for row-based placement has been developed. The new placement algorithm, part of TimberWolfSC version 4.2, requires 9 to 48 times less cpu time than version 3.2, while still achieving placements of equal or better quality. In fact, it is now possible to use the flexible and powerful simulated annealing algorithm for row-based placement on a MicroV AX II desktop workstation for circuits containing up to 3000 cells with a run time of less than 24 hours. On two circuits used for a benchmark competition at the 1987 Design Automation Conference, version 4.2 yielded total wire length values which were approximately 20 percent less than the best of the other algorithms. The main features of the new algorithm are problem normalization and negative-feedback control of the key simulated annealing parameters. In particular, we have attempted to optimize the relative weighting between the primary objective term and the penalty function terms in the cost function. Furthermore, the temperature profile has been effectively replaced by a controlled acceptance rate profile which assures excellent performance. We have placed emphasis on selecting new configurations which have a reasonable chance of acceptance. Moves which yield large penalty increases are rejected early, before cpu time is wasted evaluating the change in the primary objective term.

References

[7] The maximum possible value of $P_o$ is asymptotically $2$ times $L_R$. This can be seen from Equation 5. Suppose that all bins except one are empty, and therefore that all cells are in that one bin. The penalty applied to the aggregate empty bins is asymptotically $L_R$ as is the penalty applied to the excessively filled single bin.
[8] The residual overlap penalty at the end of the simulated annealing run is removed by sorting the cells and packing them adjacent to one another starting from the left end of the rows. This step results in some increase in the value of $W$. We have observed that there is an optimum amount of this jump in $W$ at the end of the run. If the overlap is severely penalized, then the amount of the jump is very small. However, we observed that the final values of $W$ are usually quite far from the lowest obtainable. On the other hand, if the overlap is very lightly penalized, then the amount of the jump is quite large leading to poor final values.
of W. We consistently observed the best performance when the final value of $P_\alpha$ was approximately 1/4 of $L_R$.

[9] This is derived by establishing a maximum row length $p$ and the number of rows having this length $k$, and then simply enumerating the number of possible configurations. However, some configurations are invariably counted twice, leading to subtraction and furthermore, to a recurrence relation.

[10] Then the centers of one or more cells hash to this bin.


[13] 24th Design Automation Conference, June 29 - July 1, 1987, Miami Beach, FL. The results on the two benchmarks were published in a document entitled Place-Off Participant Results From Ken Roberts. All entries were routed by the UTMC Highland system.
Simulation Processor SP

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Hiroshi Hamamura, Keiichiro Uchida
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ABSTRACT

We have developed a high-speed, large-capacity logic simulation engine, a simulation processor (SP), as a logic verification tool for FUJITSU large digital system design. It employs event driven simulation in a multi-processor configuration, using a multi-stage switching network with an attached buffer memory to minimize interprocessor communications and reduce bottleneck. It handles logic and memory primitives with an accuracy of 16 signal values and unit/zero delay, and can simulate 4M primitives and 32 Mbyte memory at a maximum speed of 0.8G active primitive evaluations per second.

References
A Pipelined Event-Driven Mixed-Mode Simulator

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ABSTRACT

This paper describes how event-driven logic and circuit simulation algorithms can be mapped concurrently onto a pipeline of transputers. The mapping of an event-driven circuit simulator onto a pipeline of processors in this manner has not previously been described. The interface between the two event-driven algorithms is efficient and allows different sections of a design to be conveniently simulated at different levels in parallel. The approach we have used to maximise the performance gain obtained from multiple processors is discussed.

REFERENCES
Modeling Circuits in the MARS Hardware Accelerator

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ABSTRACT

MARS (Microprogrammable Accelerator for Rapid Simulations) is an exploratory hardware accelerator designed at AT&T Bell Laboratories. This paper will concentrate on a tool, MCC (MARS Circuit Compiler), that generates logic models for the MARS accelerator from a transistor level description of the circuit. The characteristics of MCC are: 1. The logic models are generated on the fly without recourse to any libraries. 2. The models are accurate to the extent that the results of simulation by MARS match fully with an MOS multiple delay simulator, 3. a large variety of technologies (we have correctly modeled even certain situations involving ratioed logic and resistors in MOS circuits) are supported and 4. MCC is extremely fast in compiling large VLSI circuits. This paper emphasizes on the extraction of MARS primitives from the MOS device level circuit descriptions, handling of special elements such as transmission gates and buses and functional modeling of memories. MCC generated logic models are superior, in their generality, simplicity and accuracy, to any of the previously reported logic models for MOS circuits.

References

Special Purpose Hardware for Algorithmic Level Simulation

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Abstract

Our research explores the use of special purpose hardware to accelerate algorithmic level simulation. Several different existing computer architectures are being evaluated and the results of these evaluations will be used to propose an architecture for algorithmic level simulation. The architectures being evaluated include a general purpose uniprocessor, a logic simulation engine which uses a non-event driven algorithm, a logic simulation processor which uses an event driven algorithm, and a data flow processor. This paper covers our work to translate an algorithmic description so it can be simulated on a logic simulation engine and initial results of simulation performance on a non-event driven machine.

References
[4] "Logic Evaluator, ZYCAD Corporation Sales Literature, June 1985".
Automatic Synthesis of Operational Amplifiers Based On Analytic Circuit Models

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Abstract

An automatic synthesis tool for CMOS op amps (OPASYN) has been developed. The program starts from one of a number of op amp circuits and proceeds to optimize various device sizes and bias currents to meet a given set of design specifications. Because it uses analytic circuit models in its inner optimization loop, it can search efficiently through a large part of the possible solution space. The program has a SPICE interface that automatically performs circuit simulations for the candidate solutions to verify the results of the synthesis and optimization procedure. The simulation results are also used to fine-tune the analytic circuit descriptions in the database. OPASYN has been implemented in Franz Lisp and demonstrated for three different basic circuits with a conventional 3 µm process and a more advanced 1.5 µm process. Experiments have shown that OPASYN quickly produces practical designs which will meet reasonable design objectives.

References

ABSTRACT

This paper presents an advanced methodology and details for designing switched capacitor circuits using computer generated synthesis and layout of an analog transfer function. Fully automated design yields a correct by construction, compact layout with virtually no sacrifice in silicon area. The software package, FIDES, runs on a personal computer and allows the user to synthesize the transfer function, perform all the necessary analysis in the frequency domain (gain, phase, group delay), perform sensitivity analysis simulating random variations of wafer processing, modify circuit properties interactively, calculate automatically switched capacitor circuit electrical topology, and finally create an optimal circuit layout. Optimization is performed on both silicon area and circuit performance.

REFERENCES

An SC Filter Compiler: Fully Automated Filter Synthesizer and Mask Generator for a CMOS Gate - Array - Type Filter Chip

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Abstract.

A complete development system for up to 12th order semi-custom switched-capacitor filters is presented that allows filter performance comparable to full custom implementations. This system employs a unique synthesis and unitized filter cell technique to allow automated design and data-base creation for nearly any filter type.

REFERENCES

Asynchronous Logic Synthesis for Signal Processing from High Level Specifications

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ABSTRACT

As we build faster digital switching circuits, the ability to accomplish global synchronization with a high speed clock becomes a limiting factor to system throughput. We circumvent this problem by using asynchronous processing blocks, that is, processors that do not require an external clocking signal. To facilitate design of circuits which use fully asynchronous processing, a logic synthesis algorithm is developed, providing a systematic way to design correct asynchronous logic with the weakest possible constraints and minimal overhead from high level specifications. The algorithm is deterministic so that the design process can be easily automated. The synthesized logic is hazard-free and guaranteed to have the shortest response time according to a behavioral specification. This paper concentrates only on the synthesis of non-metastable circuits. A high level description is employed in specifying circuit behavior, not only for a simpler input format, but also as a basis for determining the final optimum designs. It is shown that asynchronous circuit design is not difficult; it can be automatically synthesized from a specification at the structural level as is commonly done in synchronous design.

References
Floorplan Design for Rectangular and L-Shaped Modules

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Abstract

We present in this paper an algorithm to produce floorplans for rectangular and L-shaped modules. This algorithm uses Polish expressions to represent floorplans and the method of simulated annealing to search for an optimal floorplan. In the case where all the modules are rectangular, our algorithm will, in general, be able to produce non-slicing floorplans.

REFERENCES

An Enhanced Bottom-Up Algorithm for Floorplan Design

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Abstract

We describe in this paper a fast algorithm for the design of floorplans. The algorithm can be used to carry out the complete design of a floorplan or to improve an existing floorplan. It is based on an enhanced bottom-up iterative improvement technique, and is capable of obtaining good solutions with an increase in speed of approximately two orders of magnitude over an algorithm using the method of simulated annealing.

REFERENCES
Hercules: A Power Analyzer for MOS VLSI Circuits

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Abstract

We present new accurate slope based models for efficient computation of both the switching and direct currents in nMOS and CMOS. These models, along with the depth-first search of stages, are incorporated into a power analysis CAD tool Hercules. In addition to the current levels in a circuit, Hercules reports the worst case voltage drops from the power pin to the device drain/source validating the power bus design. The metal segments in the power/ground bus having potential electromigration problem are flagged. All the cascaded drivers whose size ratio deviates significantly from the ideal ratio based on the power consumption are also detected.

References

Estimating Dynamic Power Consumption of CMOS Circuits

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Abstract

We present a new statistical method for deriving internal switching rates of CMOS circuits from internal controllabilities. A new algorithm for estimating the internal controllabilities from external controllabilities is developed. Application of the results to dynamic power consumption of CMOS circuits is discussed.

References

ZSIM: A Nonlinear Z-Domain Simulator for Delta-Sigma Modulators

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ABSTRACT

In this paper we present ZSIM, a nonlinear Z-domain SIMulator for sampled data systems, specifically for Delta-Sigma Modulators. ZSIM integrates analytic tools, a difference equation simulator, a novel table-based nonlinear Z-domain simulator, and digital signal processing into a workstation environment. The primary goal of ZSIM is development of a fast and accurate simulator for Delta-Sigma Modulators. The use of table-based simulation allows for simulation of circuit nonidealities including clock feed-through, nonlinearities, and hysteresis. We present high-level and low-level comparisons of difference-equation simulations and circuit-level simulations to verify the table-based ZSIM simulator. Simulations are presented for Delta-Sigma Modulators used in voiceband CODECs and in the U-interface of an ISDN network terminator.

REFERENCES