

# OUTPUT TRANSITION TIME MODELING OF CMOS STRUCTURES

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## ABSTRACT

Non zero signal rise and fall times contribute significantly to CMOS gate performances such as propagation delay or short circuit power dissipation. We present a closed form expression to model output rise and fall times in deep submicron CMOS structures. The model is first developed for inverters considering fast and slow input ramp conditions. It is then extended to gates through a reduction procedure considering the maximum current available in the serial transistor array. Validation of this modeling is obtained by comparing calculated gate output transition time to simulated ones (HSPICE level and foundry card model on 0.18 $\mu$ m process).

## 1. INTRODUCTION

The use of safe gate level characterization of performances over the full design space is the only way to maintain timing relationships between functional blocks when designs approach complexity of millions of transistors. To control or drive design alternatives, technology migration, as well as process variation it appears necessary to get available design oriented models to evaluate the performances of specific structures. The traditional representation of delay associates a constant "inertial" delay characteristic of the cell to an output load dependent delay characterizing the cell size and structure.

However input-to-output coupling effects associated to speed saturation of the carriers induce non linearity for the propagation delays which are important enough to be considered for accurate cell delay-performance characterization. Great sensitivity of the delay to the edge of the input controlling signal has been observed in submicron processes. These edges are generally defined as the controlling gate output-voltage transition time measured between appropriate voltage levels. These signal rise and fall times contribute significantly to the delay and are responsible of the nonlinear variation of real delay values. As a result, gate delay characterization implies consideration of propagation and output transition times.

The modeling of the gate output transition time has been the object of numerous works. Due to the difficulty in solving the complete differential equation representing the discharge (charge) of the gate output node, various attempts have been done to characterize this output transition time, including step [1], ramp [2] and exponential models [3]. In [4], a submicron delay and output slope modeling is given, still limited to fast input transitions. Recently, as an extension of the work proposed in [4], S. Dutta [5], considered very slow input ramp

effects. Both the delay and the output ramp duration are obtained by curve fitting between two extreme points corresponding to infinitely fast and infinitely slow inputs. As an improvement of his initial work Sakurai [6] considered extremely fast and slow ramp conditions and solved intermediate cases from smooth interpolation between the two extremes. In [7] Bisdounis proposed a fast and slow input slope definition from the operating mode of the switching transistor however, no clear design oriented definition of both fast and slow input transition range, based on the size and the load of the switching and controlling devices appears available. Hirata in [8] proposed a piece wise linear representation of the current available in the switching structure. This approach necessitates a great number of calibrations on Spice simulations of the different technological parameters used in the representation.

In fact the output ramp duration of a CMOS structure depends on its current possibility ( $I_{MAX}$ ) and of the amount of charge to be transferred ( $C.V_{DD}$ ). As proposed in [9] it can be obtained from:

$$\tau_{OUT} = \frac{C_L \cdot V_{DD}}{I_{MAX}} \quad (1)$$

where  $V_{DD}$  represents the node voltage variation and  $C_L$  its output loading capacitance.

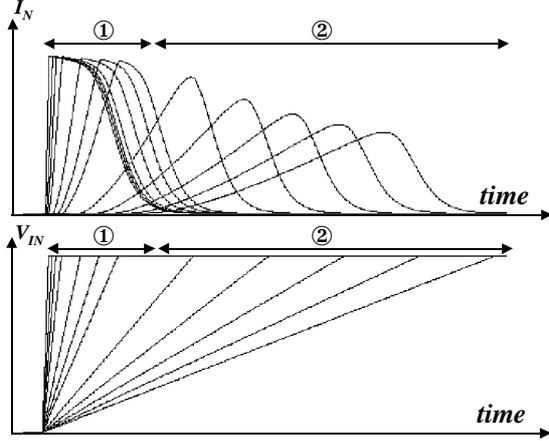
As shown the key parameter in modeling the output transition time is the current available in the switching structure of which determination depends on the structure, its size and the duration time of the input controlling edge. In order to complete an analytical model of delays developed for submicron CMOS structures [9], we present in this paper a design oriented macro modeling of the CMOS structure output transition time. In section 2 we present the method we used to obtain the value of the maximum current available in CMOS inverter and gates considering both fast and slow input ramp conditions. The modeling and the validation of output transition time is given in section 3. Section 4 draws a conclusion on this model.

## 2. INVERTER MAXIMUM CURRENT

Depending on the strength of the controlling structure two design conditions have to be considered, fast and slow input ramp conditions. Let us consider an inverter with a load  $C_L$  controlled by a rising linear input ramp of duration  $\tau_{IN}$ . As shown in Fig.1, the current sunk from the load by the N transistor depends on the value of  $\tau_{IN}$ :

- in region 1 the set up of the current of the N transistor follows the input ramp variation and exhibits a constant maximum value during all the discharge process, this defines the fast input range,

- in region 2 the maximum current is obtained before the input ramp reaches its maximum value, resulting in a smaller value of the charge evacuated by unit time. This defines the slow input range where the maximum value of the discharging current decreases when the input transition time increases.



**Figure 1.** Illustration of the fast ① and slow ② input controlling ranges of an inverter.

### 2.1 Maximum current value for fast input range

During all the input ramping process the N transistor is saturated, its current maximum value is defined for  $V_{IN} = V_{DD}$ , resulting in:

$$I_{MAX}(fast) = K_N \cdot W_N \cdot (V_{DD} - V_{TN}) \quad (2)$$

where  $K_N$  is the transistor conduction factor defined in [4] for  $\alpha=1$ ,  $V_{TN}$  and  $W_N$  the N transistor threshold voltage and width respectively.

### 2.2 Maximum current value for slow input range

As in the preceding case the transistor is still in saturation when its current reaches the maximum but its gate driving voltage is smaller and its value must be defined. For that we consider that in the time interval  $t_{VTN} - t_{MAX}$ , (Fig.2), the current exhibits a linear variation. This gives:

$$I_N(t) = K_N \cdot W_N \cdot \left( \frac{V_{DD} \cdot t}{\tau_{IN}} - V_{TN} \right) \quad (3)$$

and:

$$\frac{\Delta I}{\Delta t} = \frac{I_{MAX}}{\Delta t} = \frac{K_N \cdot W_N \cdot V_{DD}}{\tau_{IN}} \quad (4)$$

where the input ramp duration time  $\tau_{IN}$  is the output ramp duration of the controlling structure, as defined in eq.1.

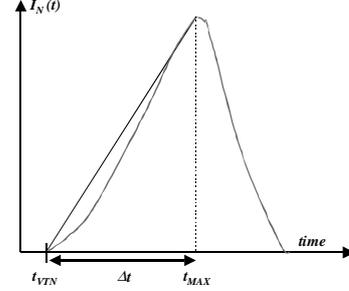
Under the approximation that the current variation is symmetric with respect to its maximum value we can evaluate the total charge removed at the output node as:

$$\frac{C \cdot V_{DD}}{2} = \frac{I_{MAX} \cdot \Delta t}{2} \quad (5)$$

Combining eq. 4 and 5 we obtain the value of the maximum current resulting from a slow rising input controlling edge as:

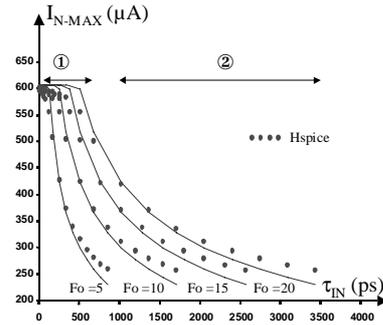
$$I_{MAX}(slow) = \sqrt{\frac{K_N \cdot W_N \cdot V_{DD}^2 \cdot C}{\tau_{IN}}} \quad (6)$$

where  $C \cdot V_{DD}$  represents the total charge to be removed from the output node, where:  $C = C_L + C_{PAR} + C_{SC}$  in which  $C_L$ ,  $C_{PAR}$  represent the inverter active load (output loading gates) and the output parasitic capacitance respectively,  $C_{SC}$  is the short circuit equivalent capacitance which represent the charge by volt unit between the supply rail during the discharge process as defined in [10,11].



**Figure 2.** Time evolution of the discharging current.

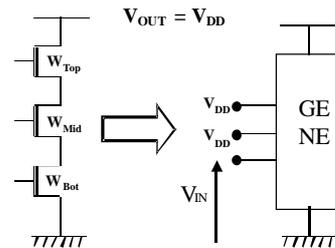
We compare in Fig.3 the maximum current values deduced from eq. 2 and 6 to the values simulated with HSPICE for an inverter defined by  $W_N=1\mu m$ ,  $W_P=2.2\mu m$ ,  $L=0.18\mu m$  for different loading conditions (5,10,15 and 20 times its input capacitance  $C_{IN}=4.5fF$ ).



**Figure 3.** Comparison between calculated and simulated maximum discharging current value; ① and ② label the fast and slow input ranges.

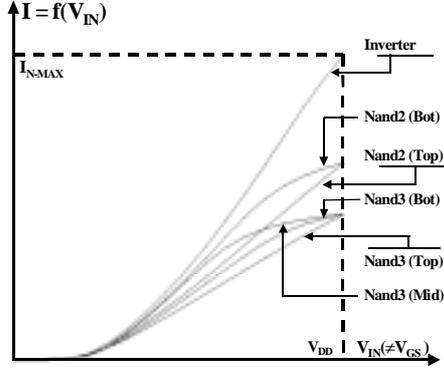
### 2.2 Maximum current value for a simple gate

The difference with respect to inverters is the occurrence in gates of a serial array of transistors. The reduction of these arrays to an equivalent transistor has been the object of numerous works [8,12-14]. We propose here a new gate reduction method to an equivalent inverter by considering the serial array of n transistors as an input voltage controlled current generator, as illustrated in Fig.4.



**Figure 4.** Reduction of the serial array of transistors to a multiple input voltage controlled current generator.

As shown in Fig.5 the current available from the serial array depends on the controlling input.



**Figure 5.** Static I/V characteristics of the current generator with respect to the controlling input (Top, Mid, Bot).

Let us consider the NAND3 of Fig.4, for a control on the top input (Bot and Mid inputs connected to  $V_{DD}$ ). The voltage drop on the Mid and Bot transistors, working in linear mode, reduces the voltage swing on the controlling gate. This induces a transistor size dependent reduction of the available current in the network with can be modeled as a reduction factor equal to the ratio of the currents available in the array and in the inverter. Direct evaluation of this ratio gives:

$$\text{Red}_{\text{FAST}} = 1 + K_N \cdot W_N \cdot R_N \quad (7)$$

where  $R_N$  represents the sum of the resistance of the bottom transistors.

For a control on the bottom input, for fast input ramps the intermediate nodes are discharged faster than the output one. In this case the current is still limited by the top transistor and the reduction factor is given by eq.7.

For slow input ramp condition the bottom and top transistors operate in saturated mode and the current is limited by the bottom transistor working with a reduced drive and drain source voltage. In this condition it appears necessary to calibrate the conduction factor of the bottom transistor in the serial array [15]. For the process under study ( $0.18\mu\text{m}$ ) values of  $\text{Red}_{\text{SLOW}} = 1.2, 1.48$  and  $1.78$  have been obtained for NAND 2, 3 and 4 respectively, which are quite different from the values obtained for fast edge conditions (1.55, 2.1 and 2.6 for NAND 2,3,4 respectively) or from a direct reduction based on the number of serial transistors [4].

The control on the middle input can easily be deduced from the preceding cases considering the middle transistor in top or bottom position for the bottom or top transistor of the array, respectively, resulting in a reduction factor:

$$\text{Red} = \text{Red}_{\text{FAST}} \cdot \text{Red}_{\text{SLOW}} \quad (8)$$

### 3 OUTPUT TRANSITION TIME

The output transition time can be obtained easily from eq.1 by replacing  $I_{\text{MAX}}$  by the expressions previously developed.

#### 3.1 Inverters

Considering fast and slow input ramp conditions results in:

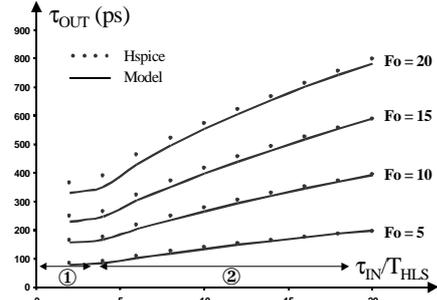
$$\tau_{\text{OUT}} = \text{MAX} \left\{ \tau_{\text{OUTFAST}}; \sqrt{\frac{(V_{\text{DD}} - V_{\text{TN}})}{V_{\text{DD}}}} \cdot \sqrt{\tau_{\text{OUTFAST}} \cdot \tau_{\text{IN}}} \right\} \quad (9)$$

with:  $\tau_{\text{OUT}}(\text{FAST}) = \tau_{\text{ST}} \cdot \frac{C_L}{C_N} = 2 \cdot T_{\text{HLS}}$  (10)

and:  $\tau_{\text{ST}} = \frac{V_{\text{DD}} \cdot L_{\text{GEO}} \cdot C_{\text{OX}}}{(V_{\text{DD}} - V_{\text{TN}}) \cdot K_N}$  (11)

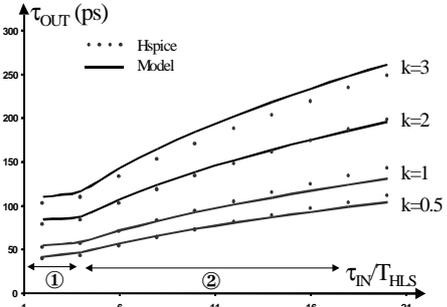
where the limit between fast and slow range can be defined easily by equalizing the two terms of eq.9.

In these equations  $T_{\text{HLS}}$  represents the step response of the inverter, and  $\tau_{\text{ST}}$  the shorter switching time of the process, as defined in [10]. Validations of these expressions have been realized on different configuration of inverters in various loading and controlling conditions by comparing simulated (HSPICE BSIM3 level 49) and calculated (eq.9) output duration time values. The results obtained are illustrated in Fig. 6-7. The output transition time evolution is given versus the ratio  $\tau_{\text{IN}}/T_{\text{HLS}}$  used as a metric for input transition times. The expression for an output rising edge can be obtained by exchanging N and P suffixes.



**Figure 6.** Output transition time values for an inverter ( $W_N=1\mu\text{m}$ ,  $W_P=2\mu\text{m}$ ,  $L=0.18\mu\text{m}$ ) loaded by 5 to 20  $C_{\text{IN}}$ ; ① and ② specify the fast and slow input ramp condition respectively.

As shown we obtain a very good agreement between simulated and calculated values (less than 10% discrepancy) over the considered full design range.



**Figure 7.** Output transition time values for an inverter ( $W_N=1\mu\text{m}$ ,  $L=0.18\mu\text{m}$ ) loaded by 5  $C_{\text{IN}}$ , for different values of the configuration ratio  $k=W_P/W_N$ .

### 3.2 Gates

Considering the current reduction factors defined in eq.7-8, the generalization to gates is straightforward, we obtain:

- for a Top input control:

$$\tau_{OUT} = \text{MAX} \left\{ \sqrt{\frac{\text{Red}_{\text{FAST}} \cdot \tau_{\text{FAST}}}{\frac{\text{Red}_{\text{FAST}} \cdot (V_{DD} - V_{TN})}{V_{DD}}}} \cdot \sqrt{\tau_{\text{FAST}} \cdot \tau_{IN}} \right\} \quad (12)$$

- for a Bot input control:

$$\tau_{OUT} = \text{MAX} \left\{ \sqrt{\frac{\text{Red}_{\text{FAST}} \cdot \tau_{\text{FAST}}}{\frac{\text{Red}_{\text{SLOW}} \cdot (V_{DD} - V_{TN})}{V_{DD}}}} \cdot \sqrt{\tau_{\text{FAST}} \cdot \tau_{IN}} \right\} \quad (13)$$

- for a Mid input control:

$$\tau_{OUT} = \text{MAX} \left\{ \sqrt{\frac{\text{Red}_{\text{FAST}} \cdot \tau_{\text{FAST}}}{\frac{\text{Red} \cdot (V_{DD} - V_{TN})}{V_{DD}}}} \cdot \sqrt{\tau_{\text{FAST}} \cdot \tau_{IN}} \right\} \quad (14)$$

Validation has been done following the same procedure than for inverters. Table 1 and 2 are relative to Top and Bottom controlled NAND2,3 ( $W_N=W_P=1\mu\text{m}$ ) loaded by  $10.C_{IN}$  and implemented in a  $0.18\mu\text{m}$  process. As shown we obtain a very good agreement between simulated and calculated values of the output transition time.

**Table 1**

$\tau_{IN}/T_{HLS}$		Nand2			Nand3		
		SIM	CAL	$\Delta\%$	SIM	CAL	%
ENTREE TOP	2	144	154	7%	240	223	5%
	6	178	172	3%	256	252	8%
	10	227	222	2%	315	325	3%
	14	270	263	3%	367	385	2%
	16	291	281	3%	392	385	2%
	20	329	315	4%	439	436	2%

**Table 2**

$\tau_{IN}/T_{HLS}$		Nand2			Nand3		
		SIM	CAL	$\Delta\%$	SIM	CAL	%
BOT INPUT	2	134	121	10%	197	204	6%
	6	166	155	7%	209	204	0%
	10	201	199	1%	233	217	1%
	14	239	236	1%	263	256	4%
	18	275	268	3%	296	291	5%
	20	292	282	4%	312	306	4%

## 4. CONCLUSION

A simple and closed form formula for the output transition time of CMOS gates is derived to reproduce the sensitivity to the design and process parameters. Based on a metric defined on inverter for fast input ramp conditions the formula includes

deep submicron effects by considering the variation of the maximum current available with the input edge. Extension has been done to gates by reduction to an equivalent inverter, considering the different input control conditions. Clear evidence of different reduction factor values for fast and slow input edges is given. Validations through HSPICE simulations for a  $0.18\mu\text{m}$  process confirm the validity of the proposed expressions which can easily be used to replace look up tables in timing estimator.

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