The 2007 Analog Decoding Workshop

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S. Hemati and A. Yongacoglu, University of Ottawa, Canada

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M. Zargham, V. Gaudet, and C. Schlegel, University of Alberta, Canada

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W. Gross, McGill University, Canada

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Stability and Singularity in Analog Min-Sum Decoders

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In this paper, we model analog min-sum decoders as piece-wise linear systems [1] and study the dynamics of these decoders. In particular, we focus on the singularity of the dynamic equations and the stability issues of analog min-sum decoders. To do so, we derive the transfer function of the analog min-sum decoder and derive eigenvalues of the corresponding characteristic matrix. For cycle-free linear block codes, we show that all eigenvalues of the characteristic matrix are negative real numbers. Thus, the analog min-sum decoder is always stable and its dynamic equations are non-singular. However, it is easy to find counter examples that show these results are not applicable to analog min-sum decoders used for codes with cycles. However, in practical analog min-sum decoders, fabrication induced randomness of the parameters (mismatch), reduces the chance of singularity by randomly scaling the messages.

Furthermore, we derive an upper bound for eigenvalues that corresponds to the maximum possible rate of variation in time-domain in analog min-sum decoders.

By using Monte Carlo simulations and analytically solving the dynamic equations, we show that singularity can substantially degrade the decoding performance for an ideal analog min-sum decoder. However, by considering mismatch, the singularity issue is mitigated and the decoding performance becomes very close to what is observed by applying successive relaxation method to the analog min-sum decoder [2].

References

[1] S. Hemati and A. Yongacoglu, “On the solvability of the dynamic equations for analog min-sum decoders,” in *Proc. Analog Decoding Workshop*, June 2006, Turin, Italy, pp.47-50.

[2] S. Hemati and A. H. Banihashemi, “Dynamics and performance analysis of analog iterative decoding for low-density parity-check (LDPC) codes,” *IEEE Trans. Comm.* vol. 54, no. 1, pp. 61-70, Jan. 2006.

Performance of Analog LDPC Decoders in Sub-100nm Processes

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Iterative decoding algorithms for LDPC codes have shown to be near-optimal in terms of error correction in communication systems. Analog CMOS implementation of these decoders offers a great advantage in terms of power and speed over its digital counterparts. As we already know fabricating circuits in smaller processes can save power and area. Implementation of these circuits in smaller processes is also important from integration point of view. These savings come by the cost of limited dynamic range of operation. Leakage currents limit the Log Likelihood ratios in the decoder and hence the performance of the decoder. These imperfections degrade the threshold as well as the error floor. We modeled some of these imperfections based on the sub-threshold circuit models in presence of leakage currents. The models were later on used in C simulations for the system level analysis. Some qualitative and quantitative results are presented based on sub-100nm circuits and such effects are discussed.

Analysis of Analog Iterative Decoders Using Generalized EXIT Charts

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EXIT charts offer a powerful method to study the traditional (digitally implemented) iterative decoders [1] and allow accelerated design of good constituent encoders. Analog VLSI, on the other hand, offers several advantages, when compared to digital VLSI implementation of algorithms [2], e.g., natural parallelism, single-transistor implementation of such operations as logarithm and multiplication, reduced size and power usage. Nonetheless, any practical design of an analog VLSI decoder has to account for limited precision for implemented (analog) arithmetic operations and other potential impairments that occur with time.

This work will present our proposed methodology and initial results on how to extend EXIT charts method to the performance analysis of analog VLSI based iterative decoders. We specifically focus on how to incorporate various analog impairments, which potentially degrade these decoders, into construction of an EXIT chart. This talk will discuss two different case studies of iterative decoders, i.e., the error-correcting turbo-decoder from the 3rd generation wireless standard [4] and iterative decoder of turbo-compressed data [5]. For each of these cases, we will present EXIT charts based results as well as bit error rate simulations, discussing in detail how to interpret validity and limitations of the obtained EXIT results with respect to potential analog implementations of the considered decoders.

References

[1] S. ten Brink, "Convergence behaviour of iteratively decoded parallel concatenated codes," *IEEE Trans. Commun.*, vol. 40, pp. 1727-1737, Oct. 2001.

[2] E. A. Vittoz, "Analog VLSI Signal Processing: Why, Where and How?," *Journal of VLSI Signal Processing*, pp. 27-44, July 2004.

[3] H.-A. Loelinger, F. Lustenberger, M. Helfenstein, and F. Tarkoy, "Probability propagation and decoding in analog VLSI," *IEEE Trans. Information Theory*, pp. 837-843, Feb. 2001.

[4] L. -N. Lee, A. R. Hammons, F. -W. Sun, and M. Eroz, "Application and Standardization of Turbo Codes in Third Generation High Speed Wireless Data Services," *IEEE Trans. Vehicular Technology*, vol. 49, no. 6, pp. 2198-2207, Nov. 2000.

[5] B. Riaz, J. Bajcsy, "EXIT chart analysis for a single source turbo compression scheme," in *Proc. Conference on Information Sciences and Systems (CISS 2007)*, Baltimore, MD, March 2007.

Thermal Effects on the Analog Decoder Performance

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The inherent sensitivity of the analog circuits to temperature makes it necessary to consider the thermal effects on the analog decoder performance within the design process. The conventional circuit level simulators are time consuming and do not provide the capability to analyze the circuits with a temperature gradient over its elements.

In this work, the effect of temperature variation on the behavior of soft gates has been studied and, as elaborated below, a procedure is proposed to investigate the thermal effects on the analog decoder performance:

- In the first step, design the circuit and the related layout according to the code structure.
- From HSPICE simulations, the *power dissipation* of each soft gate can be derived, and according to the proposed layout the *location* of soft gates in IC is determined.
- Based on the calculated power dissipation and the placement of soft gates, the *temperature distribution* over the soft gates of the analog decoder is determined, using a finite element method software such as ANSYS.
- Next, simulate individual soft gates in the related temperature using HSPICE to extract the approximate value of the *time constant* of each soft gate.
- Next, simulate the decoder in the system level (C++/MATLAB) based on the Successive Relaxation method [1], [2], [3] according to the extracted time constant for each soft gate in its working temperature to evaluate the BER performance or the convergence time of the decoder.
- Finally, go to the first step and refine the designed circuit and layout or choose the best one among different designed layouts.

Using this procedure, we can migrate from circuit level simulations towards system level simulations, which illustrate the behavior of the decoder affected by both the temperature gradients over the IC plate and the variations in the operating temperature of the IC.

References

[1] S. Hemati,and A. H. Banihashemi, "Dynamics and Performance Analysis of Analog Iterative Decoding for Low-Density Parity-Check (LDPC) Codes, " *IEEE Transaction on Communications*, Vol. 54, No. 1, Jan 2006.

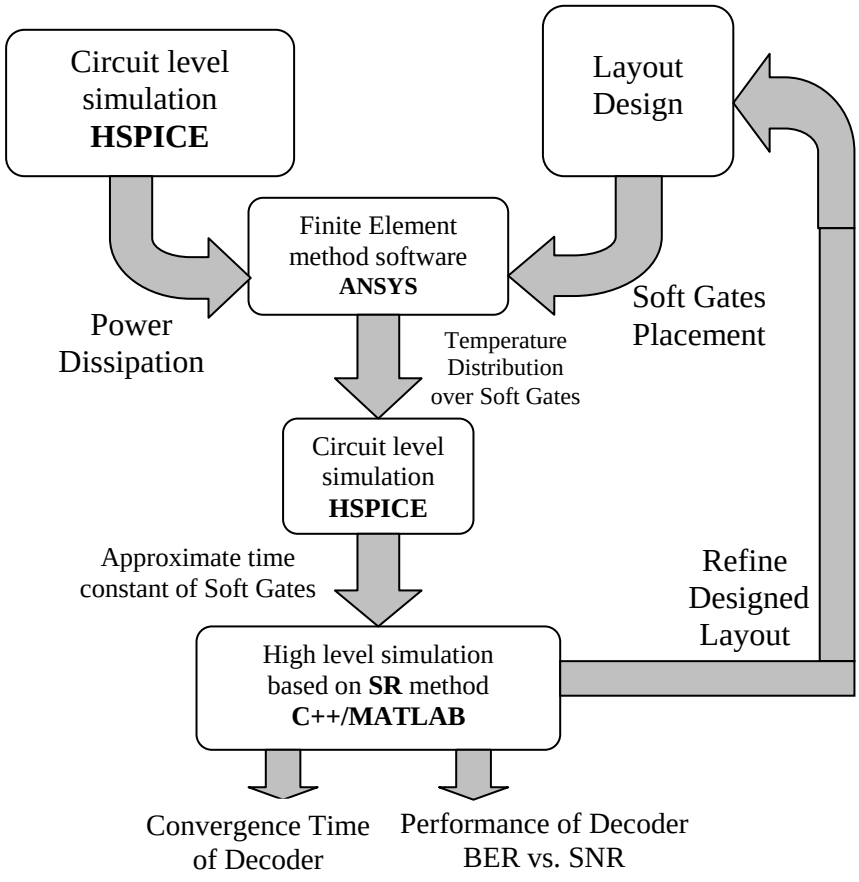
[2] V. S. S. Aditya Devarakonda, and C. Winstead, "Accuracy of Dynamical Models for Analog Iterative Error Control Decoders", *48th Midwest Symposium on Circuits and Systems*, 2005.

[3] G. i. Amat, S. Benedetto, G. Montorsi, D. Vogrig, Andrea Neviani, and A. Gerosa, "Design, Simulation, and Testing of a CMOS Analog Decoder for the Block Length-40 UMTS Turbo Code, " *IEEE Transactions on Communications*, Vol. 54, No. 11, Nov 2006.

[4] D. Vogrig,A. Gerosa, A. Neviani, A. Graell i Amat, G. Montorsi, and S. Benedetto, "A 0.35-_m CMOS Analog Turbo Decoder for the 40-bit Rate 1/3 UMTS Channel Code", *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 3, Mar 2005.

[5] F. Lustenberger, "On the Design of Analog VLSI Iterative Decoders,"*Ph.D. thesis*, ETH Zurich, Nov 2000.

[6] F. Lustenberger, H. A. Loelinger, "On mismatch errors in analog VLSI error correcting decoders", *IEEE International symposium on Circuits and Systems*, May 2001.



Analog and Digital Continuous-Time Computation and Signal Processing

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This talk presents approaches to continuous-time computation and signal processing. The first part of the talk reports on modern hybrid computation. In this approach, a CMOS VLSI (100 mm^2) analog computer is programmed by a digital-computer interface consisting of a graphical user interface in Matlab's Simulink and a data acquisition card.

The power vs. accuracy trade-offs of analog and digital computation favour analog computation for low to medium accuracy and digital computation for high accuracy computation. A usage model in which the analog computer supplies an approximate solution of a differential equation to the digital computer is demonstrated, thereby accelerating the performance of the digital computer. An example in which the system is used to predict statistics for the solution of a stochastic differential equation will also be shown.

The second part of the talk deals with continuous-time digital signal processing. In this context, an analog signal is quantized but not sampled, resulting in continuous-time binary signals which are processed directly using continuous-time digital hardware. This eliminates aliasing and results in much smaller in-band quantization error than is possible with conventional digital techniques. Preliminary experimental and simulation results support these claims. The emphasis of the talk is on principles, some of which may lead to practically important results whereas others may be interesting only from a conceptual viewpoint.

A High Resolution Sigma-Delta Modulating Digital-to-Analogue Converter

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We propose an architecture for a Sigma-Delta modulating digital-to- analogue converter (SDM-DAC) designed to achieve greater than 134dB SNR (22 bits) across a bandwidth of 0.001 - 10Hz. This architecture uses sophisticated implementations of sigma-delta modulators, higher-order quantizers, dynamic element matching systems, and ultra low- noise current sources in order to meet this target.

The bulk of the effort is oriented around minimizing and mitigating noise in the analogue half of the system. Due to the low signal bandwidth operation of the system, the predominant fundamental noise source is 1/f noise (flicker noise). Compensating for this noise is achieved through a combination of oversampled digital filtering (dynamic element matching), and innovative circuit design. As well, the minimization of layout-related noise sources such as capacitively- coupled interconnects and charge sharing from digital switches is discussed.

The relationship between Sigma-Delta modulating digital-to-analogue data converters and analogue decoders is also investigated. Methods of using digital circuits to compensate for analogue device mismatch are discussed, and layout techniques for minimizing mismatch are described.

Calibration of Analog-to-Digital Converters with Low-Precision Components

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The paper considers the calibration of flash-type analog-to-digital converters (ADCs). If such ADCs are built with very small (and thus very imprecise) analog components, the loss in static resolution (with respect to an ideal ADC) is only about 1.3 bits. The deliberate use of low-precision components may therefore allow large savings of chip area and power consumption. However, such chips need individual calibration. The paper demonstrates a calibration method based on time measurements and using very little (low-precision) hardware support. A calibration algorithm is presented that combines least squares (to find the unknown comparator thresholds) with expectation maximization (to identify the unknown parameters of the calibration signals). The algorithm is derived as message passing in a factor graph.

Stochastic Decoding of LDPC Codes

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Stochastic computation is a new alternative approach for iterative computation on factor graphs. In this approach, information is represented by the statistics of the bit stream which results in simple high-speed hardware implementation of graph-based algorithms. Despite the first purpose of the invention of stochastic computation (*i.e.*, low-precision digital circuits), the application of stochastic computation in iterative decoding of practical Low-Density Parity-Check (LDPC) codes has recently been shown to be able to provide near-optimal decoding performance with respect to the floating-point Sum-Product Algorithm (SPA). In addition, stochastic decoding introduces new decoding features and possibilities for iterative decoding of error-correcting codes. This paper provides a survey of stochastic methods for graph-based iterative decoding, the state-of-the-art and, their possible new features and applications.

Hysteresis Techniques for Stochastic Decoders

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Stochastic decoders offer the potential for very low-complexity iterative decoding. This potential is complicated by the presence of cycles in a code's graph, which frequently cause a catastrophic "latch-up" phenomenon in stochastic decoders. Two solutions have been proposed to deal with cycle-induced latch-up, namely "supernodes" and "edge memories". In this paper we examine the use of hysteresis in up-down counters as a novel way to eliminate latch-up. We show that latch-up cannot occur when hysteresis is employed, and that hysteretic counters have a much faster transient response than edge memories of the same complexity. Our hysteresis techniques are demonstrated on moderate-sized LDPC codes, revealing performance comparable to min-sum decoding. Hysteretic decoders typically requiring under one thousand stochastic clocks, compared to recently reported results which required tens of thousands of clocks for LDPC decoding with edge memories.

Implementation of an Asynchronous LDPC Decoder Using Multiple-Valued Duplex Interleaving

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Turbo codes, and Low-Density Parity-Check (LDPC) codes have been incorporated into many communication standards such as DVB-S2, IEEE 802.16e and 10GBASE-T. Bit-parallel LDPC decoders, which have a potential advantage in high speed, lead to complex interconnect wiring in an interleaver portion between computation nodes for large code length, which causes a low clock frequency and throughput because the clock cycle is determined by the worst-case wiring delay. This paper presents a bit-parallel LDPC decoder chip based on asynchronous interleaving. The use of the asynchronous interleaver makes it possible to realize the data transfer which is not determined by the worst-case wiring delay. Since both asynchronous control signals and data are directly represented by a multi-level current signal based on multiple-valued current-mode (MVCM) circuits, asynchronous full-duplex communication can be performed by just 2 wires which are one third of the conventional asynchronous data transfer, and are the same as that of the synchronous data transfer. Moreover, the binary-CMOS/MVCM mixed design flow is proposed for the LDPC decoder. As a result, throughput is increased by 65% with respect to a conventional scheme for a similar coding gain in a 90nm CMOS technology.

Cortex Codes and Analogue Decoding

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The Analogue Decoding community has mainly focused its efforts on Low-Density Parity-Check (LDPC) and Turbo codes. The Cortex codes proposed by Carlach and Vervoux are also suitable for analogue decoding given the construction and characteristics of the codes. It is a family of short block codes having good minimal distance properties.

This family of codes was originally proposed as a rate 0.5 block codes family $C[n = 2k, k, d_{\min}]$ whose generator matrices are given in systematic form $G_{[n,k,d_{\min}]} = [I_k \mid P_k]$, where I_k is the $k \times k$ identity matrix and P_k is the parity matrix of the code.

The Cortex construction is a simple way to reach, in most cases, the highest minimal distance possible for a given code size. For example, the Golay code $G[24,12,8]$ can be constructed using the parity matrix of the extended Hamming $H[8,4,4]$ code and a given permutations set.

The multi-stage construction of Cortex codes has similarities to Turbo codes since it uses short base codes and interleavers.

This paper explains what Cortex codes are. It also gives interesting perspectives and ideas on the research of optimal analogue decoders for short and long codes with good minimal distance properties.

Differential Decoding of LDPC Codes with Binary Message-Passing

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Successive relaxation (SR) method applied to the fixed-point problem of iterative decoding has proved to be superior to the conventional method of successive substitution. Inspired by the dynamics of SR, in this work we propose a binary message-passing algorithm for the decoding of low-density parity-check (LDPC) codes. Similar to SR, the proposed algorithm is with memory and the memory elements are updated differentially in each iteration according to the binary messages, hence the name "differential decoding with binary message-passing (DD-BMP)," for the algorithm.

The algorithm substantially improves the performance of purely hard-decision iterative algorithms with a small increase in the memory requirements and the computational complexity. We associate a reliability value to each nonzero element of the code's parity-check matrix, and differentially modify this value in each iteration based on the sum of the extrinsic binary messages from the check nodes. For the tested random and finite-geometry LDPC codes, the proposed algorithm can achieve performance as close as 1.3 dB and 0.7 dB to that of belief propagation (BP) at the bit error rates of 10^{-5}, respectively. This is while, unlike BP, the algorithm does not require the estimation of channel signal to noise ratio. Low memory and computational requirements and binary message-passing make the proposed algorithm attractive for high-speed low-power applications.

Joint Channel Estimation and Decoding of LDPC Codes with Analog Circuits

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To decode LDPC coded frames by the Belief Propagation (BP) algorithm successfully, it is necessary to prepare appropriate soft inputs for the decoder according to the channel SNR, which is unknown to the receiver in general. Also, to have a full analog receiver, of interest in practical applications, it is necessary to design analog circuits that receive the demodulator soft outputs and prepare appropriate soft inputs for the analog decoder.

In this work, we study the sensitivity of the performance (BER & FER) of the LDPC codes using the BP decoding in the presence of channel SNR mismatch. Then, we introduce soft metrics, including the minimum absolute value of LLR at the decoder outputs, which can be extracted from the decoder soft outputs easily, and have the same dynamic as the BER under the estimated channel SNR mismatch. Also, we show that the minimum value of the BER occurs when the minimum absolute value of the decoder output LLR reaches its maximum value.

Next, we propose a graph based algorithm which is composed of a BP LDPC decoder and a stochastic gradient-type recursive channel estimator. The estimator nodes attempt to increase the minimum absolute LLR value of the decoder soft outputs adaptively by changing the estimated channel reliability.

The circuits of the check nodes and the variable nodes of the LDPC decoder are based on the conventional voltage mode Gilbert multiplier for LLR domain decoding. Therefore, we focus on the design of the analog circuit for the implementation of the building blocks of the estimator nodes. The designed circuits include an interface between the decoder and the estimator nodes, a metric extractor, and a decision circuit to determine the direction of the estimated channel reliability variations, and a recursive update circuit as the core of the estimator.

References

[1] H. Saeedi, A. H. Banihashemi, “Performance of Belief Propagation for Decoding LDPC Codes in the Presence of Channel Estimation Error”, *IEEE Transaction on Communications*, Vol. 55, No. 1, Jan 2007.

[2] W. Oh, K. Chenun, “Adaptive Channel SNR Estimation Algorithm for Turbo Decoder”, *IEEE Communications letters*, Vol. 4, No. 8, Aug. 2000.

[3] S. Hemati, A. H. Banihashemi, C. Pelett, “A 0.18μm CMOS Analog Min-Sum Iterative Decoder for a (32,8) Low-Density Parity-Check (LDPC) Code”, *IEEE Journal of Solid-State Circuits,* Vol.41, No. 11, Nov 2006.

[4] D. Haley, C. Winstead, A. Grant, V. Gaudet, C. Schlegel, “An Analog/Digital Mode-Switching LDPC Codec*”, IEEE International Symposium on Circuits and Systems,* May 2005.

[5] C. R. Schneider, H. C. Card, “Analog CMOS Deterministic Boltzmann Circuits”, *IEEE Journal of Solid-State Circuits,* Vol. 28, No. 8, Aug 1993.

[6] J. Hagenauer, M. Moers, A. Schaefer, “Analog decoders and receivers for high speed applications”, *International Zuirch seminar on Broadband Communications,* Feb 2002.

Broadband Wireless Technology for Next Generation Mobile Communications Systems

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The 3rd generation (3G) mobile communications networks based on direct-sequence code division multiple access (DS-CDMA) technique [1], with much higher data rates up to 384kbps than the present 2G mobile networks, were put into services in some countries and their deployment speed has since accelerated. 3G mobile networks will be continuously evolving with high speed downlink packet access (HSDPA) technique, multiple-input/multiple-output (MIMO) antenna technique, etc, for providing packet data services of around 14Mbps as the mid-term evolution and of 30~100Mbps as the long-term evolution. However, demands for downloading of ever increasing volume of information will become stronger in mobile networks as well. Most of the services may contain high resolution and short delay streaming video combined with high fidelity audio. The capabilities of 3G mobile networks will sooner or later be insufficient to cope with the increasing demands for broadband services. The evolution of 3G mobile networks will be followed by the development of next generation mobile networks, called 4th generation (4G) mobile communications networks, that support extremely high-speed packet data services of e.g., 100M~1Gbps [2].

The most important technical challenge for the realization of 4G mobile communications networks is two-fold: (a) to overcome the highly frequency-selective fading channel, and (b) to significantly reduce the transmit power from mobile terminals. Recently, it was shown [3]-[5] that frequency-domain equalization (FDE) can take advantage of channel frequency-selectivity and improve the transmission performance of single carrier (SC) DS-CDMA signal transmissions as well as multicarrier (MC) signal transmissions. Either SC or MC can be used for the downlink (base-to-mobile) to achieve almost the same bit error rate (BER) performance. However, for the uplink (mobile-to-base) applications, SC transmission is more appropriate since it requires less peak transmit power. Transmit power reduction is a very important issue. Applying wireless multi-hop technique is a possible solution to this issue. In this presentation, we will discuss about some important 4G wireless techniques.

References

[1] F. Adachi, M. Sawahashi and H. Suda, “Wideband DS-CDMA for next generation mobile communications systems,” IEEE Commun. Mag., Vol. 36, No. 9, pp. 56-69, Sept. 1998.
[2] Y. Kim, B. J. Jeong, J. Chung, C.-S. Hwang, J. S. Ryu, K.-H. Kim, and Y. K. Kim, “Beyond 3G: vision, requirements, and enabling technologies,” IEEE Commun. Mag., Vol. 41, No. 3, pp.120-124, Mar. 2003.
[3] D. Falconer, S. L. Ariyavistakul, A. Benyamin-Seeyar, and B. Eidson, “Frequency domain equalization for single-carrier broadband wireless systems,” IEEE Commun. Mag., Vol. 40, No. 4, pp.58-66, Apr. 2002.
[4] F. Adachi, T. Sao, and T. Itagaki, “Performance of multicode DS-CDMA using frequency domain equalization in a frequency selective fading channel,” Electron. Lett., Vol. 39, No. 2, pp.239-241, Jan. 2003.
[5] F. Adachi, D. Garg, S. Takaoka, and K. Takeda, “Broadband CDMA techniques,” IEEE Wireless Commun. Mag., Vol. 12, No. 2, pp.8-18, Apr. 2005.

Combined Iterative Estimation/Decoding for Differential Turbo-Coded Modulation

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Phase and timing synchronization are critical receiver operations; failure to achieve phase and/or timing synchronization can result in total decoding failure. Synchronization is typically performed prior to decoding, but iterative decoders offer the potential for inclusion of synchronization within the decoding process.

This work examines integration of both phase and timing estimation into the iterative decoding process. With increasing iterations, the phase and timing synchronizers provide better estimates for use in the iterative decoder, and thus improved decoding output. A low-complexity serially concatenated code (SCC) comprised of an outer (3,2,2) parity check code separated by a bit interleaver from an inner differential 8-PSK modulation code is considered.

The phase estimation technique utilizes the inner decoder's *a posteriori* probability (APP) information about the transmitted symbols to form an iteratively-improving phase estimate for each symbol interval, and is termed APP phase estimation. Similarly, APP timing estimation uses the inner decoder's APP symbol probabilities to generate iteratively-improving symbol estimates for the classic Gardner timing error detector. Near-coherent performance is achieved with both a fixed timing offset and a uniformly random timing offset.

Both APP phase and timing estimation are then combined in the iterative decoding loop. Frame synchronization is considered to be done prior to decoding; thus the timing offset will be within [-T/2,T/2], where T is the symbol transmission time. The frame synchronizer uses multiple samples per symbol to locate the correlation peak and detect a frame. The frame synchronizer provides samples that are biased towards zero timing offset; that is, the timing offset probability function is not uniform over [-T/2,T/2] but resembles a doubly-truncated zero-mean Gaussian distribution.

Near-coherent performance results were achieved for the integrated phase/timing estimation/iterative decoder in the presence of a phase offset of pi/16 radians and a doubly-truncated Gaussian-distributed timing offset.

Dynamic Power Performance Analysis of a Digital LDPC Decoder

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A method to characterize the dynamic power in a digital low-density parity check (LDPC) decoder is presented. The method counts bitwise transitions between iterations on the edges of an LDPC graph. This is an incremental step towards reducing overall power consumption in the decoder. It is important since characterizing the dynamic power performance of decoding algorithms is necessary to understanding trade-offs. The method is applicable to both regular and irregular LDPC codes, but can be applied to other more general systems. The approach is applied to a LDPC decoder implemented in a C-simulation. The decoder itself uses finite precision min-sum decoding. The message passing is done differentially in order to show how dynamic power changes with message size. At each node a local process is used to globally monitor the dynamic power dissipation and keep track of the full messages. Dynamic power in a digital circuit can be expressed as a function of: activity factor, power supply, frequency of the clock and the capacitance. The method aims to solve for activity factor by counting bit transitions between iterations. The other factors can be estimated.

Novel Algorithms for Turbo Decoding of Product Codes

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The Adaptive Belief Propagation (ABP) algorithm of Jiang and Narayanan is an iterative SISO decoding algorithm for Reed-Solomon codes. This method adapts the parity check matrix at each iteration of the Belief Propagation (BP) algorithm according to the bit reliabilities in order to sparsify the columns of the parity check matrix associated with the unreliable bits. The ABP algorithm is especially interesting for decoding linear block codes whose parity check matrix is not sparse such as BCH or Reed-Solomon codes. In this presentation, the standard algorithm is simplified by moving the matrix adaptation step outside of the iteration loop for the turbo decoding of product codes based on BCH component codes. The complexity of the single Adaptation Belief Propagation (sA-BP) algorithm is thus significantly reduced. Moreover, the sA-BP algorithm clearly outperforms the standard ABP algorithm in terms of the bit-error-rate (BER) with a few numbers of iterations in the case of product codes. Simulation results for the turbo decoding of BCH product codes show that compared to the Chase-Pyndiah algorithm no significant BER deviation is observed. The advantages of the sA-BP algorithm are its high degree of parallelism for high data rate applications and the possibility of applying to it a new decoding method called “stochastic decoding”. Stochastic decoding previously applied to the BP decoding of LDPC codes, has the potential to be applied to product codes decoded with the sA-BP algorithm.

Analog Encoding-Decoding in Computational Biosensors

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Computational biosensors concisely refer to a class of hybrid devices where the core computation is performed using bio-molecules (eg. proteins or DNA). In this work we present architecture of a forward-error correcting biosensor, where analog encoding is based on computational paradigms inherent in antigen-antibody binding whereas analog decoding is performed using CMOS circuits. Following principles deep rooted in communication theory the hybrid computing approach can be shown to reliably detect multiple pathogens in a sample in the presence of biological interference (non-specific binding events and biosensor artifacts). A Markov random field (MRF) analog decoder is presented that processes the encoded biosensor signals. In this paper the biological logic gates have been configured as a repeat-accumulate (RA) code by immobilizing antibodies at disjoint spatial locations of an immunosensor. This structure is then mapped onto an MRF decoding graph which represents joint likelihood of valid code-words encoded by the biosensor. We show using equivalent electrical models of the bio-molecular logic gates that MRF decoders can successfully correct for random errors in a sample multi-array biosensor. A systematic method of constructing MRF decoders is also presented along with its implementation using analog and digital circuits.

La Gargotte Restaurant (Thursday Dinner)

La Gargotte Restaurant
Vieux Montreal
351, Place D'Youville
Montréal, Québec
Métro: Square Victoria Station (Orange Line)
Tel: (514) 844-1428
Web: www.bar-resto.com/gargote/

List of Restaurants Close to the ADW'07 Venue

Fast Food services in Eaton Center in the Underground City (French: La Ville Souterraine) within 10 to 15 minutes walking distance
Direction: Head southeast on Rue University, turn right at Rue Saint-Catherine, enter the Eaton center. The food court is located in zone 1-2xx

Restaurants on Avenue du Parc within 5 to 10 minutes walking distance
Direction: Head southeast on Rue University, turn left at Rue Milton and turn right at Avenue du Parc.

Acropolis Ouzerie (Greek restaurant)
3412, avenue du parc
Montréal, Québec
Tel.: (514) 845-8685

Asha (Indian restaurant)
3490, avenue du parc
Montréal, Québec
Tel.: (514) 844-3178

Bistro Isakaya (Japanese restaurant)
3469, ave. du parc
Montreal, Québec
Tel.: (514) 845-8226

Wing Fa (Chinese restaurant)
3412, ave. du parc
Montreal, Québec
Tel.: (514) 282-3938

Workshop Venue and Map

Room 2100
Trottier Building
3630 University Street (at the corner of Prince-Arthur St. West)
McGill University
Montreal, Quebec H3A 2B2