The effect of threshold voltages on the soft error rate

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Abstract

Due to technology scaling, smaller devices and lower operating voltages, next generation circuits are highly susceptible to soft errors. Another important problem confronting silicon scaling is static power consumption. In this paper, we analyze the effect of increasing threshold voltage (widely used for reducing static power consumption) on the soft error rate (SER). We find that increasing threshold voltage improves SER of transmission gate based flip-flops, but can adversely affect the robustness of combinational logic due to the effect of higher threshold voltages on the attenuation of transient pulses. We also show that clever use of high V_t can improve the robustness of 6T-SRAMs.

1 Introduction

Soft error phenomenon in DRAMs was known to exist as early as 1970s [16], also radiation effects on spacecraft and airplane electronics have been known for long [13]. But drastic shrinking in device sizes, associated with reduction in operating voltages and increase in operating frequency, is making caches and sequential logic increasingly susceptible to soft errors from natural ground level radiation [12, 20, 21]. Soft errors are the most benign form of radiation effects on the circuitry, where radiation directly or indirectly induces a localized ionization capable of upsetting internal data states. While these errors result in an upset event, the circuit itself is not damaged. These errors are particularly troublesome for memory elements as the stored values of the bits are changed. But due to increasing pipeline depths in new generation processors, soft error threat to sequential circuit is very real [21, 4, 14]. In sequential logic the transient pulse usually gets attenuated. However due to the high operating frequency the probability of these errors getting latched on is increasing [6].

On another front, leakage power dissipation is challenging the rate of scaling of the CMOS technology [7]. There is a considerable industry and academic effort spent on this problem. There have been numerous techniques proposed at circuit, microarchitecture and compiler level. Leakage current is a combination of subthreshold and gate oxide leakage [22]. Subthreshold leakage can be controlled by reducing the supply voltage or by increasing the threshold voltage (V_t) of the device. Gate leakage is a less understood term, but it is known that it can be controlled by using thicker gate oxides or high K dielectrics. Also both of these depend on the gate width and gate count.

Conventional ways of reducing the soft error rates include adding redundancy, increasing nodal capacitance and using error correcting codes. In this work we analyze the effect of increasing the V_t of the device on soft errors in standard memory elements like SRAM and flip-flop and also on combinational circuits like chain of inverters, nand gates and transmission gate based full adders, which represent the most common CMOS logic styles. We believe such an analysis is very important because it helps us make intelligent design choices that reduce leakage power consumption and improve the reliability of the next generation circuits.

The paper is organized as follows: Section II presents the background for soft errors, correcting schemes and related work, section III presents the theoretical premise of our scheme, section IV presents the experimental setup, section V discusses the results, and section VI presents the conclusions.

2 Background and related work

2.1 Soft Errors

When energy particles hit the silicon substrate the kinetic energy of the particle generates electron hole pairs as they pass through p-n junctions. Some of the deposited charge will recombine to form a very short duration current pulse which causes soft error. In memory elements, these can cause bit flips, but in combinational circuits these cause temporary change in the output. In combinational logic such a pulse is naturally attenuated, but if a transient pulse is latched, it corrupts the logic state of the circuit [6, 8].

There are three principle sources of soft errors: alpha particles, high-energy cosmic ray induced neutrons and neutron induced ^{10}B fission. Alpha particles are emitted from the packaging materials and the interaction of cosmic ray thermal neutron with boron present in the P-type regions of the devices [3]. A single alpha particle can generate anywhere from 4 to 16fC/m over its entire range.

High-energy cosmic ray induced neutron flux is strongly dependent on altitude, with intensity of the cosmic ray neutron flux increasing with increasing altitude. The primary reaction by which cosmic ray induced neutrons cause SER is by silicon recoil. The impinging neutrons knock off the silicon from its lattice. The displaced silicon nucleus breaks down into smaller fragments each of which generates some charge. The charge density for silicon recoils is about 25 to 150fC/m, which is more than that from alpha particle strike. So it has a higher potential to upset the circuit.

The third significant source of ionizing particles is from the neutron induced ^{10}B fission. ^{10}B, an isotope of p-type dopant (about 19.9%), is unstable and on impact from neutron it absorbs the neutrons and breaks apart with the release of an alpha particle and ^{7}Li (Lithium). Both these by-products are capable of inducing soft errors. To reduce SER due to alpha particle induced soft errors, one can use pure materials and shield the circuit so that components with higher alpha emission rates are physically isolated from the sensitive circuits. But such solutions are generally not effective against the neutrons as they are highly penetrative. The intensity of these neutron radiations depends on altitude, geomagnetic region and solar cycles [23]. Recent works [11, 12, 20] have shown the effect of technology scaling on soft errors. In [23], a study on radiation flux noted that particles of lower energy occur far more frequently than particles of higher energy. So it can be seen that as CMOS device sizes decrease, they are more easily affected by these lower energy particles, potentially leading to a much higher rate of soft errors.

2.2 Soft Error Mitigation Schemes

The basic soft error mitigation techniques involve information redundancy, space redundancy and time redundancy. These techniques have been applied at different granularity. Recently, researchers have proposed techniques to make use of inherent hardware redundancies of multi-threaded and on-chip multiprocessor architectures in concurrent error detection [17, 18]. In memory structures, the information redundancy can be reduced by clever use of codes and scrubbing techniques. There are also many modifications one can do at circuit level to make the circuit robust. Redundancy methods can also be used in circuits [1]. Since the logic state of a circuit at a node is stored as the charge stored at that node (Q=CV), we can increase the nodal capacitance of the gate and thus make the node more robust [15]. The $Q_{critical}$ at a node will decrease as voltage or nodal capacitance decreases. The nodal capacitance is strongly dependent on the layout. Some designs offer better immunity against SER than others. In [10, 19] we have characterized SER of different SRAM and flip-flop designs. All these techniques cost a lot in terms of complexity, area, power and performance. In this work, we find that higher V_t can reduce SER in transmission gate based designs but it increases the SER of combinational circuits.

3 Factors Affecting SER due to high threshold voltages

There are two distinct factors that affect soft error rates due to increase in threshold voltages. First, due to the physical properties of high V_t silicon, we require higher energy to create electron-hole pairs in the substrate. This effect can potentially reduce SER. Second, higher V_t increases the gain and delay of circuits. This affects attenuation of the transient pulse.

3.1 Charge creation under high threshold voltages

This section gives a simplified theory of the semiconductors and we use this analysis to explain the phenomenon of charge creation under high V_t. A detailed analysis is beyond the scope of this paper. Equation 1 represents the factors on which the threshold voltage depends.

$$V_t = V_{fb} + V_b + V_{ox} \tag{1}$$

where,
V_t is the threshold voltage of the MOS device
V_{fb} is the flat band voltage
V_b is the voltage drop across the depletion region at inversion
V_{ox} stands for potential drop across the gate oxide
When we change the threshold voltage of a device we change the flat band voltage(V_{fb}) of the device. Flat band voltage is the built in voltage offset across the MOS device [9]. It is the workfunction difference θ_{ms} which exists between polygate and silicon. By increasing the threshold voltage, we increase the energy required to push the electrons up the valence band. This is the same reason for which the device slows down. So when we increase the threshold voltage, the charge creation and collection characteristics change.

3.2 Logic attenuation under high threshold voltage

As mentioned in the earlier section in pass transistors and transmission gates the transient pulses attenuate due to V_t drop across the devices. But static CMOS sees different trends. In static CMOS, the gain of the circuit is positive. The gain of an inverter is given by equation 2

$$GainG = \frac{1+r}{(V_m - V_t - V_{dsat}/2)(\lambda_n - \lambda_p)} \tag{2}$$

where *r* is the switching threshold, V_m is half of the supply voltage, V_{dsat} is drain saturation current, and λ_n, λ_p are channel length modulation factors for an n-channel and p-channel respectively. We can see that due to higher gain, a transient pulse will propagate in a system for a longer time and travels more logic stages. Another important fact to be considered is the delay. High V_t causes the device to slow down. Now in a simple logic network, under normal V_t, a particle strike will manifest as a bit flip only if the pulse is latched under a certain window. Any pulse occurring earlier or later will not be latched and hence will not result in a logic error. Assuming the stage takes *t* time units and the window of vulnerability is *(t_v)*, any error in the time interval $t - t_v$ will either be attenuated or will not be latched at the output. In case of high V_t, owing to the slower pulse and higher magnitude, t_v is longer, thus making the logic chain more susceptible.

4 Methodology

For a soft error to occur at a specific node in a circuit, the collected charge Q at that particular node should be greater than $Q_{critical}$. $Q_{critical}$ can be defined as the minimum charge collected due to a particle strike that can cause a soft error. If the charge generated by a particle strike at a node is more than $Q_{critical}$, the generated pulse is latched on, resulting in a bit flip. This concept of critical charge is generally used to estimate the sensitivity of SER. The value of $Q_{critical}$ can be found by measuring the current required to flip a memory cell and derived using equation 3.

The particle strike itself is modeled as piece wise linear current waveform where the waveform's peak accounts for funneling charge collection and the waveform's tail accounts for diffusion charge collection. By changing the magnitude of the peak of the waveform and appropriately scaling the waveform, we try to find the minimum height for which the the wrong value is stored in the memory element. Similar approach has been used in prior work [20].
However, a transient change in the value of a logic circuit does not affect the results of a computation unless it is captured in a memory element like a flip-flop. Therefore, to measure $Q_{critical}$ of a combinational logic, we inject a current pulse and try to latch the wrong value at the output of the logic chain. A logic error can be masked by logical masking, electrical masking and latching-window masking [13]. Such masking reduces the derating effects of soft errors. Since in this work we are attempting to study the effect of increasing V_t on SER, we inject the current pulse only to those nodes which produce the change in the output. For logic circuits the input nodes were chosen to inject the current pulse. For memory elements, the internal nodes, where the logical value is stored as charge, were chosen. For the inverter chain (6 inverters), the current pulse was injected at the 6^{th} inverter from the flip-flop and for nand gates (4 nand gates in a chain) at the input of the 4^{th} nand gate from the flip-flop. Also, when we change V_t of the circuit, the setup time of the output latch also changes and this is considered in obtaining $Q_{critical}$ of the logic chain. The actual magnitude of the charge is given by equation 3.

$$Q_{critical} = \int_0^{T_f} I_d dt \tag{3}$$

I_d is the drain current induced by the charged particle. T_f is the flipping time and in memory circuits it can be defined as the point in time when the feedback mechanism of the back-to-back inverter will take over from the incident ion's current. For logic circuits, T_f is simply the time of the pulse. The formulation provided by equation 3, is used in our experimental evaluation. In this work, we focus primarily on $Q_{critical}$ in comparing the SER of our designs, since the other parameters, charge collection efficiency and linear energy transfer(LET) are quite similar across designs. Also finding these parameters is beyond the scope of our work. In our study we use two types of designs; memory elements which include 6T-SRAM, asymmetric SRAMs(ASRAM), flip-flops, and logic elements which include 6-inverter chain, 4-FO4 nand chain, 1-bit transmission gate (TG) based adders. All the circuits are custom designed using 70nm Berkeley predictive technology [5] and the netlists are extracted. The netlists are simulated using Hspice. The normal V_t of these devices is 0.22V, and the supply voltage of 1V is used. V_t is changed using *delvto* option of Hspice [24]. *Delvto* changes the V_t of the transistors by the amount specified. We analyzed all circuits by changing V_t by 0.1V and 0.2V for both PMOS and NMOS.

5 Results and discussion

Table 1 gives the absolute values of $Q_{critical}$ for change in V_t. We observe that $Q_{critical}$ increases with increase in threshold voltages. This observation is generally true for

	ΔV_t	$Q_{critical}$ /C		ΔV_t	$Q_{critical}$ /C
TGFF 1→0	0	1.99e-20	ASRAM	0	4.75e-14
	0.1	4.75e-14		0.1	6.58e-14
	0.2	3.87e-17		0.2	7.58e-14
TGFF 0→1	0	3.04e-20	Inverters	0	1.28e-20
	0.1	5.03e-20		0.1	2.3e-20
	0.2	4.18e-19		0.2	4.73e-20
Adder 1→0	0	4.60e-20	Nand	0	1.31e-20
	0.1	1.35e-19		0.1	2.26e-20
	0.2	5.87e-17		0.2	2.83e-20
Adder 0→1	0	3.67e-17	SRAM	0	4.75e-14
	0.1	4.29e-17		0.1	4.04e-14
	0.2	7.13e-17		0.2	3.82e-14

Table 1. The Critical charge of various designs

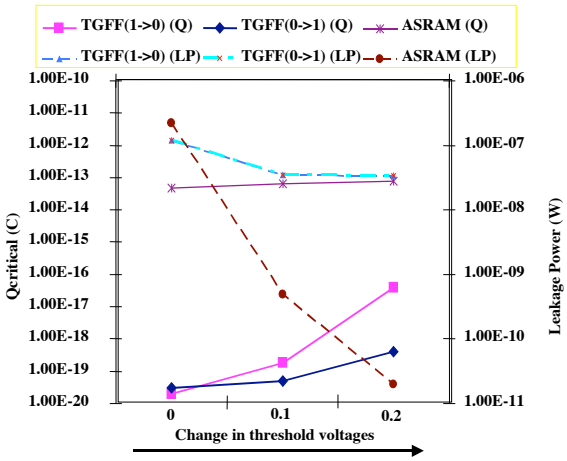

Figure 1. Critical Charge Vs Leakage Power

	ΔV_t	Leakage /W		ΔV_t	Leakage /W
TGFF 1→0	0	1.18e-07	ASRAM	0	2.20e-07
	0.1	3.42e-08		0.1	9.10e-09
	0.2	3.40e-08		0.2	3.42e-10
TGFF 0→1	0	1.20e-07	Inverters	0	2.20e-07
	0.1	3.42e-08		0.1	4.90e-10
	0.2	3.40e-08		0.2	41.99e-11
Adder 1→0	0	3.61e-05	Nand	0	22.56e-07
	0.1	3.49e-05		0.1	9.92e-09
	0.2	3.46e-05		0.2	4.90e-10
Adder 0→1	0	3.61e-05	SRAM	0	2.40e-07
	0.1	3.49e-05		0.1	9.66e-09
	0.2	4.59e-06		0.2	9.46e-10

Table 2. Leakage of different designs

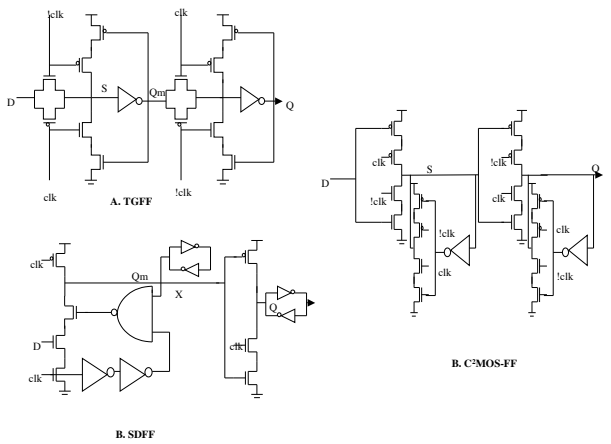

Figure 2. Flip-Flops

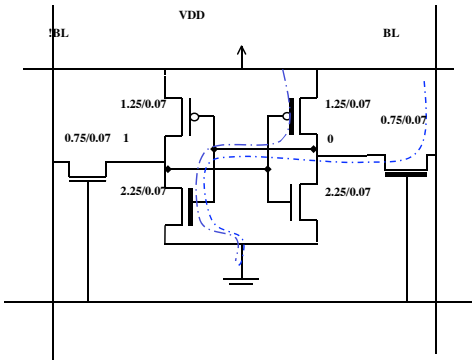

Figure 3. Asymmetric SRAM: Optimized for 0

ASRAMs and flip-flops, but requires more analysis for logic chains and SRAMs. Also for some designs we calculated the $Q_{critical}$ for both 0 to 1 flips and 1 to 0 flips and as in [14], we found $Q_{critical}$ for 0 to 1 flips higher than 1 to 0 flips. This can be explained by the fact that PMOS is intrinsically slower than NMOS. Thus we calculated $Q_{critical}$ for only 1 to 0 flip for larger designs due to the longer simulation time of these designs. From Table 2, we observe that the leakage power decreases with increasing threshold voltages. Analysis of each of these designs is presented in the following sub-sections.

5.1 SRAM memory

From Table 1, we observe that the threshold change does not affect $Q_{critical}$ of the standard 6T SRAM significantly. By increasing V_t by 0.2V, we do not notice any significant change in $Q_{critical}$. Because the threshold voltage of both PMOS and NMOS in the back-to-back inverter configuration was changed, the regenerative property of the circuit ensures that there is no loss of charge and hence relatively no gains in terms of $Q_{critical}$. However, when we analyze an ASRAM [2] optimized for leakage while storing a preferred logic state, we observe a different trend.

	ΔV_t	$Q_{critical}$ at input $/C$	$Q_{critical}$ at most susceptible node $/C$
SDFF	0	6.06e-21	1.24e-20
	0.1	5.08e-21	1.33e-20
	0.2	-	-
C^2MOS	0	3.69e-20	7.12e-21
	0.1	5.64e-20	7.12e-21
	0.2	1.68e-19	-
TGFF	0	1.99e-20	7.36e-21
	0.1	1.77e-19	7.36e-21
	0.2	3.87e-17	7.36e-21

Table 3. Critical Charge of different flip-flops

Figure 3 shows a circuit schematic of ASRAM optimized for storing a 0. In ASRAM, the threshold voltages of transistors in the leaky path of circuit are increased to reduce leakage. For a stored value of 0, the transistors on the leaky path are shown. The V_t of these transistors are increased to reduce the leakage. The $Q_{critical}$ of this SRAM in its preferred state (i.e, when storing a 0) increases significantly, however for the non preferred state it remains the same. Specifically, when V_t is increased by 0.2V, $Q_{critical}$ increases by 59%. This is due to the fact that if we try to charge the node to 1, the PMOS due to its high V_t will not be able to provide necessary feedback to quickly change the bit. But, if a value of 1 is stored, and we attempt to discharge it, then $Q_{critical}$ does not change as the NMOS is still at normal V_t. A similar behavior is also observed for an ASRAM designed for storing a preferred state of 1.

5.2 Flip-Flops

We characterize three different flip-flops, transmission gate flip flop(TGFF), C^2MOS flip-flop(C^2MOS), and semi -dynamic flip-flop (SDFF), for estimating the effect of increasing threshold voltages on $Q_{critical}$. Please refer to Figure 2 for detailed schematics of these designs. There are two different effects of the change in threshold voltages on flip-flops. Firstly, the soft error rate of the flip-flop itself could change. This is found by evaluating $Q_{critical}$ at the most susceptible node [19]. Secondly the ability of the flip-flop to latch onto an error at it's input could change. This effect will be useful in analyzing its behavior in a datapath. And since we focus on datapaths, we list the $Q_{critical}$, at the input of flip-flop in Table 1, and in Figure 4.
The results for 1 to 0 transition for the node S and the input D, for TGFF are given in the Table 3. The $Q_{critical}$ of the node remains almost constant. In fact there is a slight reduction in the value, which is not evident from the values given in the table. There are two factors that could affect the change in $Q_{critical}$. The gain of the inverter, for which the node S is an input, increases. This should result in a significant reduction in $Q_{critical}$. Also the transmission gate present at the slave stage would lead to a greater $Q_{critical}$ for the node as the threshold voltages increase. These two factors effectively cancel each other out and hence the $Q_{critical}$ remains almost constant. At the input D, the presence of the transmission gate results in a large increase in $Q_{critical}$. Similar testing was done on a C^2MOS flip-flop which also has master-slave stages sim-

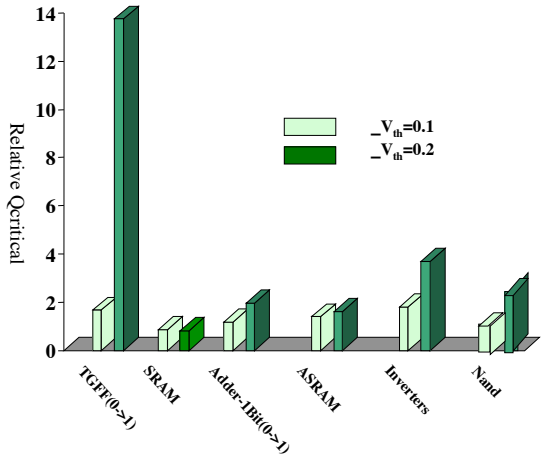

Figure 4. Relative Critical Charge of different designs

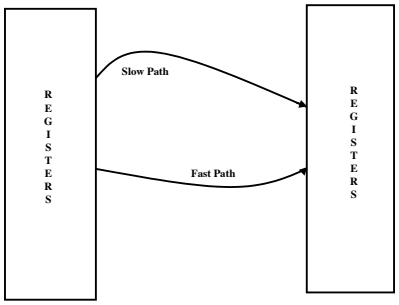

Figure 5. Critical charge of the 6-inverter chain with different Flip-Flops

ilar to that of the transmission gate flip-flop. In this case, since there is no inverter in the path to the output, $Q_{critical}$ increases for both the nodes S and D.
One of the pulse triggered designs, Semi-dynamic flip-flop is also tested for change in $Q_{critical}$. This design has few large sized devices resulting in a much higher $Q_{critical}$. Here, the node X is the most susceptible node. Since this node feeds back into a nand gate, when the threshold increases, due to the increase in delay of the nand gate and 2 inverters, $Q_{critical}$ increases. Thus the flip-flop by itself has a higher $Q_{critical}$ as threshold voltage increases. At the input the greater overlap time helps pull down voltage at node X more and hence reduces the $Q_{critical}$. When V_t increases by 0.2V, the flip-flop fails to latch the input data. Hence, $Q_{critical}$ is not listed in the table.

5.3 Combinational Logic

We analyze three kinds of logic circuits: chain of 6-inverters, chain of 4-nand gates and transmission gate based

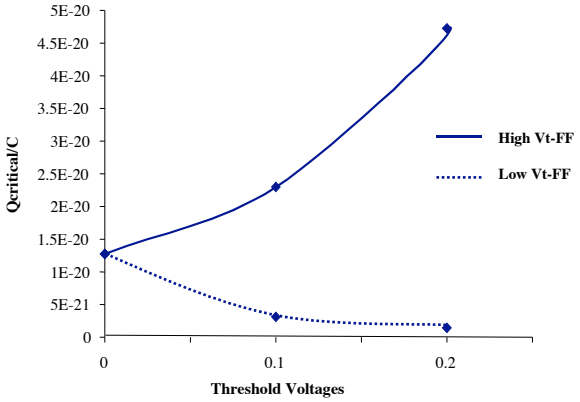

Figure 6. Critical path analysis

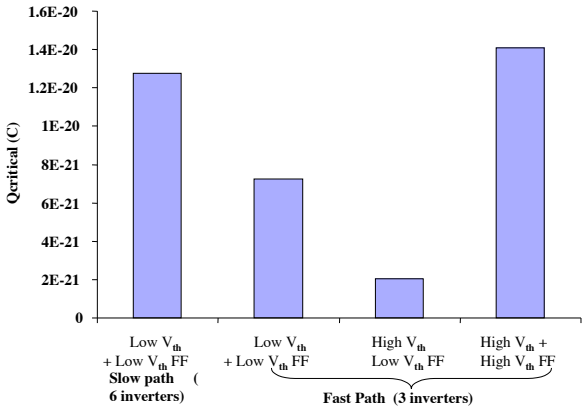

Figure 7. Effect of delay balancing

full adders. For all of these circuits we check for an error by latching the transient pulse at the end of the logic chain. A transmission gate flip-flop (TGFF) was used to latch the values. TGFF was chosen as it is one of the most common flip-flop used in computers(Used in PowerPC603). From Table 1, we note that the $Q_{critical}$ of the circuit is increasing for increasing threshold voltages. For TG based adders, the threshold drop across transmission gates account for the higher $Q_{critical}$. But for static logic this is counter intuitive. Based on the pulse propagation characteristics, the $Q_{critical}$ of the circuits should be lower. This can be accounted for the robustness of flip-flops. In Figure 4, we find the $Q_{critical}$ increase for the flip-flop many orders of magnitude higher than the others. To confirm our observations we simulated the 6-inverter chain again, but this time we used normal-V_t flip-flops and we found that as the V_t increased, the $Q_{critical}$ values decreased. The results are presented in Figure 5.

Figure 6 shows a typical pipeline. The logic between pipeline stages is distributed across slow and fast paths, with the slowest path determining the clock frequency. Thus, slow paths become critical paths and fast paths become non-critical paths. It is an accepted practice to use high V_t devices on non-critical paths. Since these are not delay sensitive, we achieve high leakage power savings with minimal performance penalty. This is some times referred to as *delay balancing*. To examine the effect of delay balancing on $Q_{critical}$, we simulate two circuits, one with 6-inverters which forms the critical path and the other with 3 inverters. Figure 7, shows the $Q_{critical}$ of the 6 inverter chain as compared to the $Q_{critical}$ of 3 inverter chain with both low and high V_t TGFFs. If we perform a delay balancing on this logic with low V_t TGFF, and high V_t 3 inverter chain, we can observe the $Q_{critical}$ of 3 inverter chain reduces. Thus, we see that this path now becomes more vulnerable to soft errors. But if a high-V_t flip-flop is used for latching, the $Q_{critical}$ of the 3 inverter chain (relative to 6 inverter chain) is still high. So, while performing delay balancing it is recommended to use high V_t flip-flops to improve the immunity to SER.

6 Conclusion

Due to technology scaling, soft errors rates are becoming increasingly important. Also, leakage energy is the biggest roadblock for continual scaling of silicon. In this work, we studied the effect of the high threshold voltages on SER. We found that for certain designs like transmission gate based designs SER reduces while for static logic SER deteriorates. Also we showed, as in ASRAM, using high V_t cleverly we can reduce both SER and leakage power. Finally we find that the use of high V_t for delay balancing can potentially increase SER, but the reliability can be brought back by the use of high V_t flip-flops. In general, we showed that use of high V_t devices not only reduces leakage but also affects the reliability of circuit. Thus analysis of leakage reduction strategies on SER is critical for reliable circuits.

7 Acknowledgment

The authors would like to thank Kerry Bernstein from IBM for valuable discussions. This work was supported in part by RSEC/PSU Reactor grant for quantifying SERs, MARCO GSRC grant and NSF Grants CAREER 0093085, 0082064 and 0103583.

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