The Testing of Superconductive ADCs in Software-Defined Radio Base Stations

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Abstract—**The available frequency allocation for the mobile communication industry is getting more and more crowded and new technologies are evolving rapidly. To efficiently utilize these emerging technologies, new generation base stations are required which can be upgraded by software rather than hardware. They are called software-defined radio base stations. These base stations require ultra high-speed data converters for their operation.**

In the near future, current state-of-the-art semiconductor ADCs cannot fulfill the requirements in frequency and resolution. Superconducting technology is promising for the implementation of this application. Superconductive ADCs are extremely fast and have very low bit error rate. Although ADCs are being developed extensively in superconducting technology, a viable test solution is still unavailable due to their high speed of operation. Current testing schemes restrict to partial low-speed testing using very expensive equipment. Furthermore, the interface between the device and the test equipments is critical.

Methods of DfT have to be applied for a complete test solution for such an ADC. In the present work, the above problem was addressed and possible solutions are presented. For determination of static parameters a linear histogram technique and for dynamic parameters sub-sampling technique has been used. Following the current trend of test-resource partitioning, our basic approach has been to reduce or omit the interfacing at high speeds and effectively down-rating the required test equipment. In its ultimate form it could end up in Built-In-Self-Test (BIST) for superconductive ADCs.

Keywords—**Superconductive devices, RSFQ circuit testing, ADC testing, BIST**

I. INTRODUCTION

Software-Defined Radio (SDR), as explained in [1], is a promising concept for the wireless communication industry since the entire transceiver function can be implemented in software, avoiding the replacement of hardware each time the system has to be upgraded. However, the practical implementation of such a system is depended on the hardware, which consists of precise, ultra high-speed electronic devices such as Analog-to-Digital Converters (ADCs). The present state-of-the-art semiconductor ADCs cannot be used for the implementation of SDR in the near future [2]. Some of the factors that hamper the implementation are the requirements of very high speed of a few tens of GHz and the high resolution (e.g. 16 bits) at these speeds.

On the other hand, using the Low-Temperature Superconducting (LTS) technology [3], which relays on the quantum mechanical property of superconductors, very high-speed electronic devices with the accuracy of a flux quantum, can be constructed. In a closed superconducting loop, the magnetic flux can exist only in discrete quantized amounts equal to the multiples of the magnetic flux quantum, $\phi_0 = h/2e \sim 2.07 \times 10^{-15}$ Wb. The theoretical speed limit of such a Rapid Single Flux Quantum (RSFQ) device is close to 1 THz [4]. These RSFQ circuits are the fastest of all devices built in any known technology. The basic building block of an RSFQ circuit is the Josephson Junction (JJ), which is formed when two superconductors are separated by an interface.

Since RSFQ circuits work at extremely high speeds, testing and verification of such a device is a difficult and challenging task. Direct testing at these speeds is not possible at this moment. Furthermore, the costs of the equipment required for such tests would be extremely high. Hence methods have to be developed to reduce the requirements of external

hardware for the test. In the SDR application, constant monitoring is favored for the Super Conducting Electronics (SCE) ADC at the base station, to ensure better service. A study on possible Design for Testability (DfT) and BIST of RSFQ circuits has been presented in our earlier paper [5].

In this paper, different aspects of testing a superconducting ADC that can be implemented in SDR applications are discussed. The paper is organized as follows. In section 2, the outcome of a study on SCE ADCs is discussed, resulting in a choice of ADC. In section 3, the chosen ADC is described in detail. Section 4 summarizes the critical parameters to be tested and in section 5 some of the associate testing schemes are described.

II. The Choice of an ADC for the SDR Application

The specifications of SDR are not yet well defined. The industry requirements and the technological advances predict that the following specifications are expected in the near future. The data stream will be 14 to 16 bits wide with at least a data rate of 120 mega samples per second. The frequency of operation will be around 20 GHz with a minimum bandwidth of 60 MHz.

Oversampling ADCs are widely used in SCE, due to the fact that filters, high precision analog components and high sampling rates can be obtained relatively easy in LTS (Niobium) technology [6]. These are extremely difficult to achieve in CMOS technology. Delta-sigma converters are highly efficient oversampling quantizers. They are known for their insensitiveness to circuit imperfections and the anti-aliasing filter preceding the ADC can be a simple structure. The majority of the anti-aliasing function can be performed in the digital domain.

In order to find the proper ADC for the SDR application, available superconducting ADCs have been investigated whose specifications are close to the above-defined SDR rating. The considered ADCs are presented in references [7-14]. Table I

TABLE I

Available ADCs in Superconducting Technology

Type	Band-Width (MHz)	Operating Frequency (GHz)	Resolution (Bits)	No. of Junctions	Tests
Delta-sigma [7]	10	2.5	16[a)]	~50[d)]	SFDR, SNR, Linearity, SQUID[e)] Response
Delta-sigma [8]	--	2	--	--	SNR
Delta [9]	20	10	--	2000+	--
Delta [10]	60	20	14[b)]	--	SNR, SFDR, Noise Bandwidth, Gain
Phase modulation-demodulation [12]	--	12	14[c)]	--	ENOB, SINAD, SFDR, Gain, FFT Analysis
Phase modulation-demodulation (with on-chip programmable decimation clock controller) [13]	--	12.8	14[c)]	2500+	ENOB, SINAD, SFDR, decimation ratio, input signal slew rate, sampling rates, linearity, performance at Nyquist sample rate, FFT analysis

a) Measured in ENOB
b) Measured in SFDR
c) ADC has 2 analog channels
d) Modulator in High-Temperature Superconductive (HTS) technology
e) Superconducting QUantum Interference Devices (SQUIDs) [15] is in principle a flux-to-voltage transducer

shows a summary of the useable results. The table is organized as follows. The ADCs are sorted by the architecture in the first column. The bandwidth of the ADC in MHz, its operating frequency in GHz followed by resolution in bits and the number of JJs are given in the next columns. The last column summarizes the tests carried out with respect to the particular device on the system.

The dynamic range (DR) of a 1st order delta-sigma modulator [16] is given by the equation

$$DR(dB) = 10\log\left(\frac{9M^3}{2\Pi^2}\right) \qquad M >> 1 \qquad (1)$$

where M is the oversampling rate. For a 2nd order modulator there will be an additional factor $\left(\frac{5M^2}{3\Pi^2}\right)$ in the log term. Considering a 16-bit delta-sigma ADC with a DR of 98.08 dB, the oversampling rate will be 2416 for a 1st order and 153 for a 2nd order converter respectively. The product of twice the sampling-rate and bandwidth gives the sampling frequency. If one considers the bandwidth to be 60 MHz, then this corresponds to an operating frequency of 290 GHz and 18.4 GHz respectively. The operating frequencies of the available 2nd order delta-sigma converters [7, 8] are far below the minimum requirements for implementation in SDR. This shows that with the present technologies, it is impossible to use 1st order converters and hence a 2nd order delta-sigma modulator has been used. The 1st and 2nd order devices are more stable than higher order systems. For the latter, special measures for stabilization are required [17].

Looking at Table I, only one of the ADCs has specifications close to the requirements. Although the delta-sigma circuits are more robust, a delta modulator ADC [10] is used in this paper because it has the required operating frequency, bandwidth and resolution. The main difference between the delta-sigma and the delta modulation is that the first one changes the spectrum of noise but leaves the signal unchanged. The latter shapes the spectrum of the modulated signal but leaves the quantization noise unchanged at the receiver end.

III. THE USED DELTA ADC

The structure of a delta modulator is shown in figure 1. It consists of an adder and quantizer in the forward loop, a Digital-to-Analog Converter (DAC), an integrator and a low-pass filter in the feedback loop. For analysis, a quantizer is assumed to be implemented as an adder in which the signal is injected with random noise. The integrator consists of an adder, a delay block and a unity gain feedback loop. In a superconducting delta modulator, the analog integrator in the feedback circuit acts like a digital one for SFQ pulses that are quantized in nature. The output of the modulator is fed to the digital integrator, which belongs to the Digital Signal Processing (DSP) part of the system.

The modified block diagram of the delta modulator for a superconducting ADC is shown in figure 2 [10]. The DAC and integrator in the feedback loop can be very simple structures in RSFQ technology, like flux amplifiers as shown in figure 2. The pulses are given to the secondary of the transformer resulting in their addition as magnetic flux quanta. The semi-circles indicate the magnetic coupling of the flux amplifier to the rest of the circuit. The flux amplifier can be implemented as a pulse multiplier. In this case, the number of resulting pulses is proportional to the number of elements in it, here m and m-1.

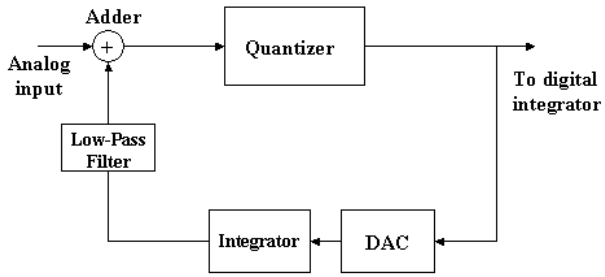

Figure 1. Block diagram of Delta modulator

The pulse multiplier can be implemented by using an SFQ splitter and confluence buffer [18]. With the pulse splitter, SFQ pulses are replicated. The confluence buffer combines them resulting in the effect of multiplication. A delay is introduced between the pulses so that they will not reach the confluence buffer at the same time, in which case only one SFQ pulse will be available at the output. The suggested circuit is shown figure 3. In the scheme, JJs are indicated as "X", I_b is the biasing current and "D" a delay block. The inductance coils and bias currents are supporting elements required for the correct operation of an RSFQ circuit.

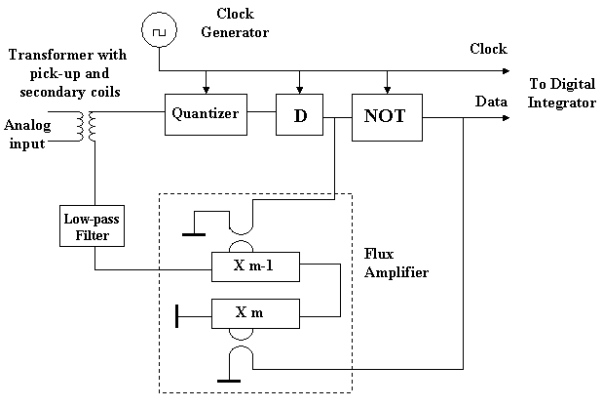

Figure 2. Superconducting Delta Modulator – Block diagram

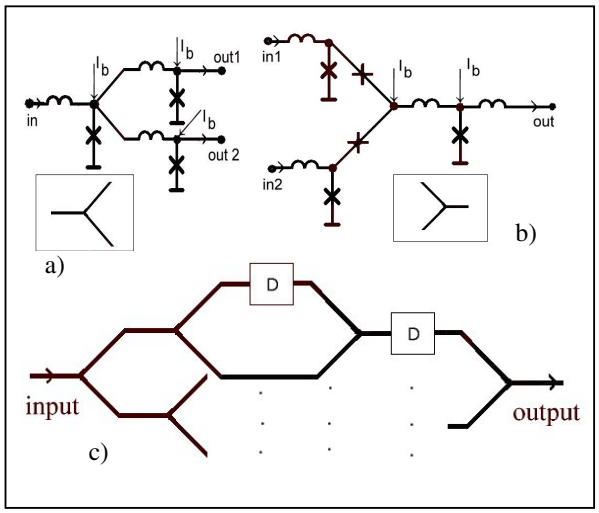

Figure 3. a) Splitter and b) Confluence buffer with notation and c) the suggested circuit for SFQ multiplication

The simulation of the above circuit has been carried out using the Josephson circuit simulator JSIM using the 3.5µm Hypres Niobium technology [19]. Figure 4 shows the splitting function. In an RSFQ circuit, the input current is first converted into an SFQ pulse using a DC-SFQ converter [18]. The resulting pulse of 20 ps width is fed into the input of the splitter. Two (amplified) pulses come out of the outputs resulting in SFQ multiplication. These pulses are applied to the input of the next stage. The multiplication factor determines the number of stages. Two of the pulses are fed into the inputs of the confluence buffer that combines them as shown in figure 5. The buffer stages are repeated till all the pulses are combined. Notice the small output amplitudes of 0.4 mV.

As a delta modulator shapes the signal and leaves the noise unchanged, a good filter is required in the feedback loop to restore the signal. This makes these modulators vulnerable to analog circuit inaccuracies. The high gain of the filter magnifies any distortion introduced by the DAC. Due to these reasons, delta modulators are not used in semiconductor technology. But as a result of the very high-speed clocking and accuracy of the RSFQ circuits, these are no longer a restriction in Niobium technology.

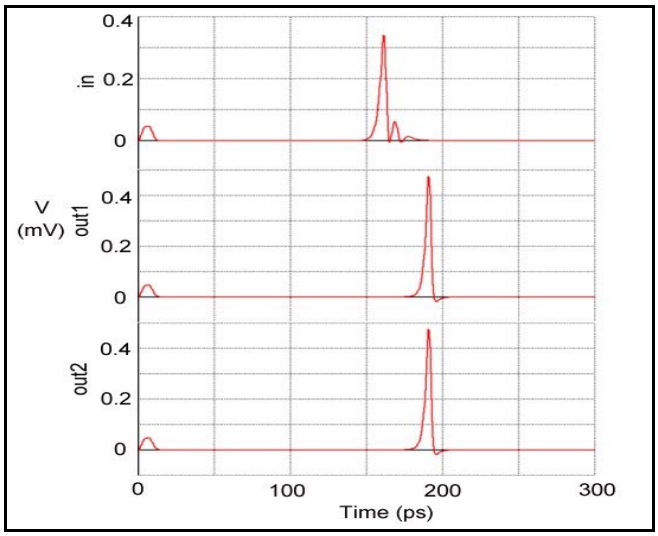

Figure 4. Simulation of splitter

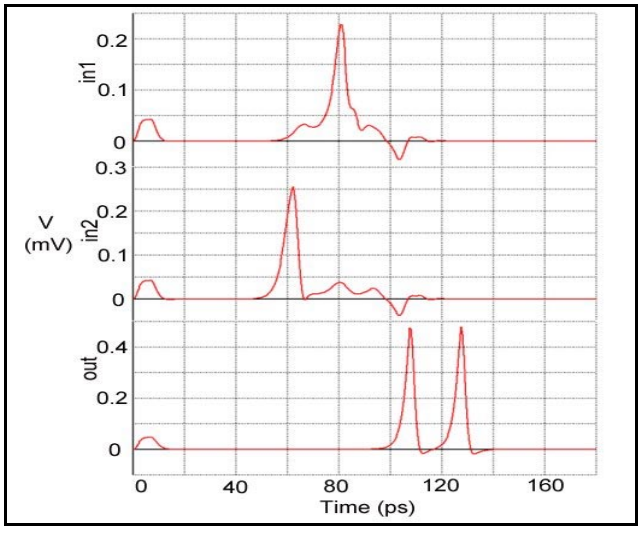

Figure 5. Simulation of Confluence buffer

IV. KEY PARAMETERS FOR VERIFICATION OF CORRECT OPERATION

From the conducted study, it was concluded that the key parameters that are to be tested are:

- Gain
- Linearity
- Bandwidth
- SIgnal-to-Noise And Distortion ratio (SINAD)
- Effective Number Of Bits (ENOB)
- Spurious Free Dynamic Range (SFDR)

Additionally delay timing and jitter are two other important parameters that are to be considered in a superconducting ADC [20, 21]. At present they are limiting the operating frequency of the circuits to a few tens of GHz. These two are not discussed in this paper as they have been dealt extensively in the above references.

ADCs for SDR applications are primarily concerned with ENOB for a given sampling rate. The resolution of an ADC can be measured quasi-statically using Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) and dynamically from SNR and SFDR by spectral analysis.

Testing of this very high-speed ADC using conventional test equipment is not possible at this moment since the instruments cannot operate at these speeds. The cost of Automatic Test Equipment (ATE), if available, will be extremely high. Hence, methods of DfT have to be applied to make the ADC testable with available "low-speed" test equipment.

From a testing and application point of view, BIST for the ADC is preferred. If applied properly, it is an efficient way to find faults. But to find a complete BIST solution is often a difficult task. In such a situation, partial BIST or methods to reduce or eliminate the external hardware for high-speed testing will be carried out. In the next section, different schemes are discussed that can be used for the proposed ADC.

V. TESTING TECHNIQUES

A. The Testing of Static Parameters

An idea that can be used for the implementation of BIST for our ADC has been suggested in [22]. This method can be applied to determine a number of static (DC) parameters. Gain, DNL and INL can be calculated using the linear histogram based test of ADCs. The block diagram for the BIST structure (figure 6) shows the different logic blocks with the additional on-chip hardware required for BIST. This scheme has been used for VHDL simulation.

A series of registers are required for the implementation of this scheme. Three 16-bit registers called output registers are used for storing the values of the three calculated parameters. The control register is an 8-bit register, which controls the BIST procedure. The data register is another 16-bit register used for storing the reference code for calculation; the execution of operations are performed in a 10-bit register called the execution register.

The main functions of the control register are mentioned below. "Procedure Select" is a 2-bit signal used to select the calculation procedure. Other signals are "Data register set/clear", "compare/count" to set the data register in compare or count mode and "pulse" to increment/decrement the execution register. The control register receives the result of comparison of the data register with the ADC output. The detailed theory on the scheme is presented in [23].

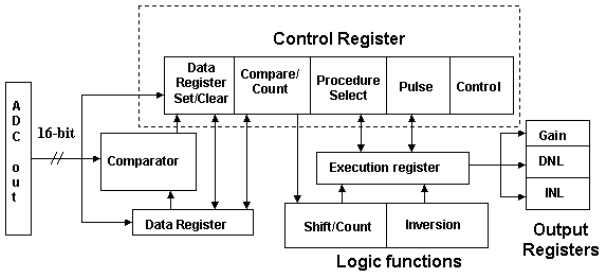

Figure 6. A Possible scheme of BIST structure for determining Gain, DNL and INL

For verification, a VHDL simulation of the above technique was carried out for an 8-bit ADC running at 500 MHz. The simulation was carried out using ModelSim VHDL running on an HP UNIX system. The results of the simulation are as follows. The gain procedure took 0.25 ms and the INL procedure 4.2 ms, thus a total time of 4.45 ms for the complete test procedure was required. Since the computations are done in real time, RSFQ circuits have to be used for the implementation of the above BIST scheme for a SCE ADC. Extensive VHDL simulations showed the correctness of this approach [24].

The RSFQ implementation of this BIST approach is as follows. As mentioned earlier, a series of registers are required to carry out the

histogram technique. The main advantage of this approach is that it involves only basic mathematical operations. Since the multiplication/division factor is a power of 2, the operations can be carried out using shift registers. The contents of the execution register are shifted accordingly to achieve it. Addition and subtraction are performed as follows. The execution register is set in a count-up/count-down mode. The value in the register is incremented or decremented depending on the code at the ADC output. The result of ADC conversion is compared with the stored value in the data register. In case of a negative result, the 2's complement is taken, thereby reducing the additional chip area.

Interesting fact is that a 1-bit stage of a SQUID Flip-Flop can be made with just 2 JJs (figure 7). The counter can be made by cascading them and the simulation of up/down counting is shown in figures 8 and 9. The Hypres Niobium technology was used for the simulation and the counter works at 40 GHz. The registers are also made from this basic SQUID Flip-Flop. Combining the basic logic gates made from JJs [18], the logic selectors and comparator can be made. Hence all the components can be implemented in LTS technology at the required speed resulting in BIST.

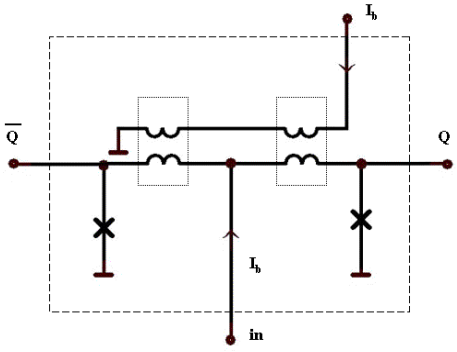

Figure 7. A simple SQUID Flip-Flop

The disadvantage of the BIST technique is the area overhead due to the introduction of the BIST structure. About 500 additional JJs are required for the implementation. If the above scheme is implemented in Hypres Niobium technology, the estimated area for this BIST structure is 0.95 mm^2. Considering the original chip to be about 14 mm^2, the area overhead is 6.3%.

B. The Testing of Dynamic Parameters

Another BIST technique for the calculation of dynamic parameters is based on the on-chip generation of a pseudo-random sequence as test stimulus. The advantage of this method is that low-resolution test stimuli can be used for testing a high-resolution modulator. But for the implementation of this technique, a large chip area is required.

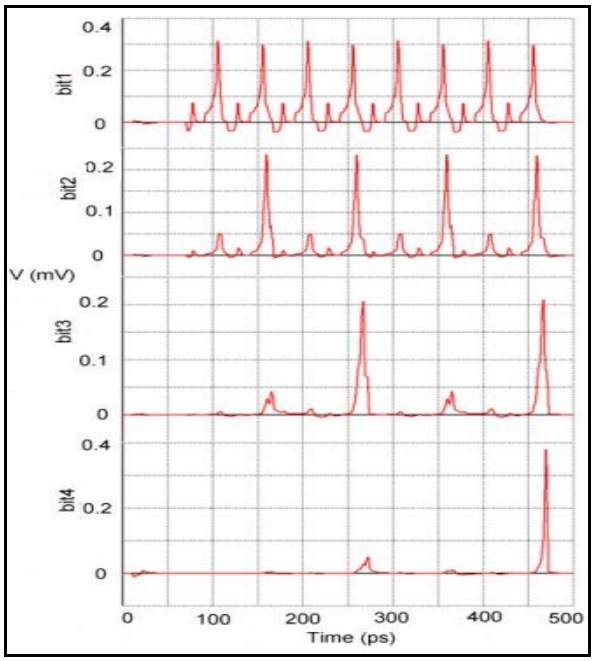

Figure 8. The simulation of the up counter

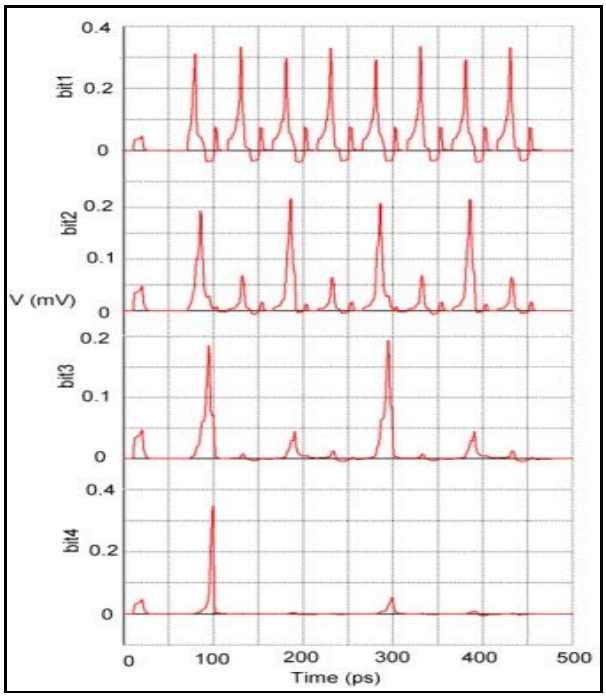

Figure 9. The simulation of the down counter

For the measurement of dynamic parameters like ENOB, SINAD and SFDR as well as the static parameters, a test approach with a DAC at the digital end of the ADC can be implemented. Here the sub-sampling technique is suggested for that purpose [17].

The suggested experimental setup is given in figure 10. A sine wave is fed into the input of the ADC. The outputs are sampled by a DAC at a frequency much lower than the sampling frequency of the ADC. The output of the DAC can then be analyzed using low-speed test equipment.

Due to the speed limitations, it is obvious that semiconductor technology cannot be used for the manufacturing of the components. A possible implementation of the setup in SCE is as follows. An over-damped JJ acts as an oscillator. Hence even an on-chip signal generation at GHz frequencies is possible with the help of signal shaping circuits. Using a series of shift registers, which is well advanced in SCE [25, 26], the sub-sampling technique can be implemented. The construction of a DAC in RSFQ technology is already proven and available [27]. Then less demanding analyzers can be used for the test parameter measurement.

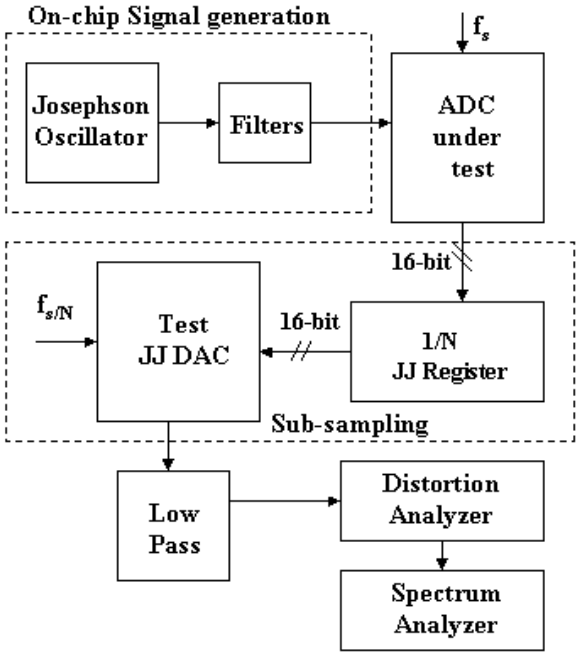

Figure 10. Block diagram for test setup for the measurement of dynamic parameters

A possible scheme for the implementation of the sub-sampling technique is shown in figure 11. The DAC and the register are clocked at a frequency $f_{s/N}$ thereby sub-sampling the ADC output by a factor of N. The limitation of this technique is that the sub-sampling factor N can only be a maximum of 4, above which the reproduced signal will be distorted.

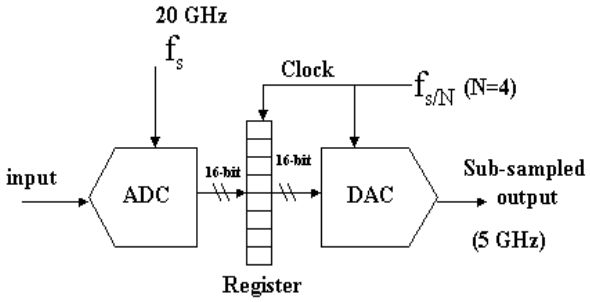

Figure 11. Sub-sampling using a Josephson register and DAC

If the above method is applied, the sub-sampled frequency will be 5 GHz in the current application. Still powerful distortion and spectrum analyzers that are capable of handling signals at these frequencies are required. The advantage of this method is less test overhead. The implementation of the sub-sampling circuit (1/N), on-chip signal generator, and DAC will be about 200 JJs. This corresponds to 0.38 mm^2 of chip area producing an overhead of 2.6%.

A total test solution for the SCE ADC can be achieved by combining the linear histogram test technique and the sub-sampling technique. If both the methods are combined, the total test overhead will be around 10%.

VI. Conclusions

In this paper, DfT for an SCE ADC has been presented. Practical implementations have been discussed and simulations were carried out to verify the techniques and found to be feasible. The actual implementations of the test structures carried out in Niobium technology are subject of a future paper.

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REFERENCES

[1] J. Mitola, "Software Radio Architecture Evolution: Foundations, Technology Tradeoffs, and Architecture Implications", IEICE Trans. Commun. Vol. E83-B, June 2000, pp. 1165-1173.

[2] R.H. Walden, "Analog-to-digital converter survey and analysis", IEEE JSAC, vol. 17, April 1999, pp. 539-550.

[3] K. Likharev, "Rapid Single Flux Quantum (RSFQ) Logic", Encyclopedia of Materials, Science and Technology, to be published by Elsevier Science. An electronic version of the document is available at: http://gamayun.physics.sunysb.edu/RSFQ/about.html

[4] W. Chen et al., "Rapid Single Flux Quantum T-Flip Flop Operating up to 770 GHz", IEEE Trans. Appl. Supercond., vol. 9, June 1999, pp. 3212-3215.

[5] H. G. Kerkhoff and H. Speek, "Defect-Oriented Testing of Josephson Logic Circuits and Systems", Physica C, vol. 350, Feb 2001, pp. 261-268.

[6] S. Tahara et al., "Superconducting Digital Electronics", IEEE Trans. Appl. Supercond., vol. 11, Mar 2001, pp. 463-468.

[7] A. H. Worsham et al., "Superconducting modulators for high dynamic range Delta-Sigma Analog-to-Digital Converter", IEEE Trans. Appl. Supercond., vol. 9, June 1999, pp. 3157-3160.

[8] D. L. Miller et al., "Flux Quantum Sigma-Delta Analog-to-Digital converter for RF signals", IEEE Trans. Appl. Supercond., vol. 9, June 1999, pp. 4026-4029.

[9] E. B. Wikborg, V. K. Semenov and K. K. Likharev, "RSFQ Front-end for a Software Radio Receiver", IEEE Trans. Appl. Supercond., vol. 9, June 1999, pp. 3615-3618.

[10] V. K. Semenov, Y. A. Polyakov and T. V. Filippov, "Superconducting ADC with on-chip decimation filter", IEEE Trans. Appl. Supercon, vol. 9, June 1999, pp. 3026-3029.

[11] S. V. Rylov et al., "High Resolution ADC using phase modulation-demodulation architecture", IEEE Trans. Appl. Supercond., vol. 9, June 1999, pp. 3016-3019.

[12] O. A. Mukhanov et al., "Progress in the development of a superconductive high resolution ADC", IEEE Trans. Appl. Supercond., vol. 9, June 1999, pp. 13-16.

[13] O. A. Mukhanov et al., "A Superconductor High-Resolution ADC", IEEE Trans. Appl. Supercond., vol. 11, Mar 2001, pp. 601-606.

[14] M. W. Johnson et al., "Wide bandwidth oscillator/counter A/D converter", IEEE Trans. Appl. Supercond., vol. 11, Mar 2001, pp. 607-611.

[15] J. Clarke, "SQUIDs: Principles, noise and applications", Chapter 2, Superconducting devices, Academic Press Inc., London, 1990.

[16] A. Perez-Verdu and A. Rodriguez-Vazquez, "Top-down design of high-performance sigma-delta modulators", Kluwer Academic publishers, Boston, 1999.

[17] R. van de Plassche, "Integrated Analog-to-Digital and Digital-to-Analog Converters", Kluwer Academic publishers, Boston, 1994.

[18] K. K. Likharev and V. K. Semenov, "RSFQ Logic/Memory Family: A new Josephson-junction technology for sub-terahertz clock-frequency digital systems", IEEE Trans. Appl. Supercond., Vol. 1, Mar. 1991, pp. 3-28.

[19] "Niobium Design Rules", Hypres Inc., New York, http://www.hypres.com/designrule/rules.pdf.

[20] A. V. Rylyakov and K. K. Likharev, "Pulse Jitter and Timing Errors in RSFQ Circuits", IEEE Trans. Appl. Supercond., Vol. 9 June 1999, pp. 3539-3544.

[21] I. V. Vernik et al., "Experimental investigation of local timing parameter variations in RSFQ circuits", IEEE Trans. Appl. Supercond., Vol. 9, June 1999, pp. 4341-4344.

[22] S Bernard et al., "Linear histogram test of ADCs - A BIST implementation", Proceedings of International Mixed-Signal Testing Workshop, Montpellier, France, June 2000, pp. 40-45.

[23] F. Azaïs et al., "Towards an ADC BIST scheme using the histogram test technique, Proceedings of the European Test Workshop, Cascais, Portugal, May 2000, pp. 129-134.

[24] V. Spoor and R. Tijssen, "VHDL implementation of the Linear Histogram test technique for ADCs", Dept. of Electrical Engineering, University of Twente, 060.18, 2001.

[25] O. A. Mukhanov, "RSFQ 1024-bit shift register for acquisition memory", IEEE Trans. Appl. Supercond., vol. 3, Dec 1993, pp. 3102-3113.

[26] A. M. Herr et al., "High-speed operation of a 64-Bit Circular Shift Register", IEEE Trans. Appl. Supercond., vol. 8, Sept. 1998, pp. 120-124.

[27] R. D. Sandell, B.J. Dalrymple and A.D. Smith, "An SFQ Digital to Analog converter" IEEE Trans. Appl. Supercond., vol. 7, June 1997, pp. 2468-2471.