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# SELF-ALIGNED GATE JFETS FOR SMART MEMS -MODELING, DESIGN AND FABRICATION

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## Abstract

Modeling, design, fabrication and characterization of Self-Aligned Gate JFET (SJFET) devices and circuits are reported. The problem of electrical isolation between devices on the same chip is solved through Self-Aligned Gate approach, enabling device integration at the application of standard bipolar discrete device technology (no epitaxy etc.). Therefore this approach offers several advantages compared to other isolation techniques (lower number of fabrication steps, lower process temperature budget, reduction of leakage problems, lower chip cost etc.) and is appropriate for application in microsystems. SJFETs are analyzed by 2D numerical device simulation. SJFET circuits are analyzed by device modeling based circuit simulation. SJFET differential amplifier circuit simulation is reviewed as an example. On the basis of modeling results, test SJFET structures were designed and fabricated. Measurements on test SJFET structures reveal reasonable agreement with modeling.

**Keywords:** JFET, self-aligned gate, device isolation, smart sensors, MEMS, device modeling, device based circuit simulation

## 1. Introduction

Different FET structures are gaining on popularity in MEMS world due to their peculiarities such as low noise, radiation hardness etc. [1]. In the paper, basic properties of modified FET structures, called Self Aligned Gate (SAG) JFETs, or shortly SJFETs, will be reported. SJFET approach is compatible with standard discrete bipolar technology. Basic SJFET device structure is presented in Fig. 1. The most interesting feature of this approach is the solution for electrical isolation between different devices on the same chip, enabling integration. Device isolation principle is shown in Fig. 2. Therefore, in SJFET approach no epitaxial step, usually introducing inconveniences such as increased number of fabrication steps, higher temperature budget of processing, leakage problems, higher chip cost etc., is necessary. Consequently, SJFET approach is appropriate for specific smart sensors and microsystems applications.

Modeling of SJFET devices and circuits with a 2D numerical simulator will be reported. It is interesting to note that in this case, numerical 2D SJFET circuit modeling is based directly on 2D device modeling. Therefore, no approximate SPICE-like models for the device description are necessary because device characteristics needed for a certain circuit simulation are calculated numerically with 2D device modeling. Consequently, model parameter validation that can be sometimes quite demanding, time consuming and also the possible source of incorrectness is not necessary. So, in this case of device modeling based circuit simulation, circuit properties are dependent only on basic device structural parameters (geometry, doping profiles etc.) and devices interconnections for a given circuit. The accuracy of results for circuit simulation is so enhanced, as well as circuit optimization based directly on device structure possible.

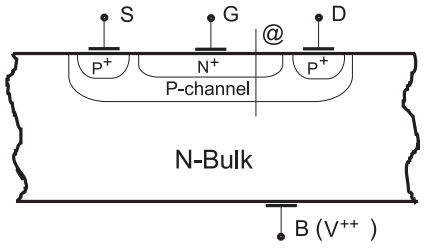


Fig. 1: Basic device structure.

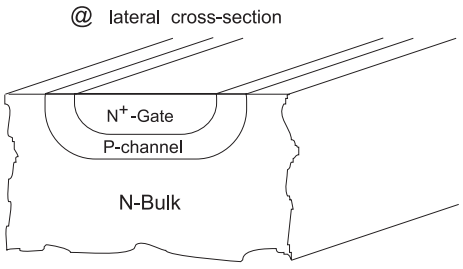


Fig. 2: Lateral cross-section through the SJFET channel.

On the basis of modeling results, various test SJFET structures were designed and fabricated. Characterization of fabricated devices will be reported and discussed. Measurements on test SJFET structures confirm expectations and are in reasonable agreement with modeling.

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## 2. Self-Aligned Gate JFET

Basic SJFET device structure is presented in Fig. 1. It is a standard JFET structure, here with P-channel (SPJFET) as an example. To provide electrical isolation of this device from other devices on the same chip, we suggest the solution with Self Aligned Gate. In this case $N^+$-Gate is diffused through the same opening as the preceding $P^+$-channel diffusion. The lateral cross-section through the channel (marked by @ in Fig. 1) is shown in Fig. 2.

If bulk electrode (B) is on the highest possible positive potential as shown in Fig. 1, there will always be an electrical isolation between different devices on the same chip. The situation is similar to device isolation in epitaxial bipolar integrated circuits: reverse biased PN junction surrounding the device provides its depletion layer that is depleted of mobile charge carriers. Depletion layer is therefore acting like an insulating layer, providing thus electrical isolation.

Typical SJFET layout for the case of *W*/*L* ratio 10 is presented in Fig.3. Test devices of various geometry were designed following the rules given in the layout in Fig. 3. Typical doping profile through the channel (path marked as @ in Fig. 1) for the case of a PJFET is shown in Fig. 4. P-channel junction is at 0.60 $\mu m$ and $N^+$-Gate junction is at 0.30 $\mu m$, resulting in P-channel thickness $d$ = 0.30 $\mu m$. Peak channel doping in this case is around $8 \times 10^{17} cm^{-3}$.

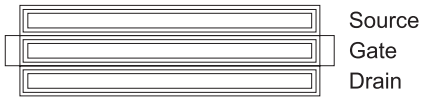


Fig. 3: SJFET layout.

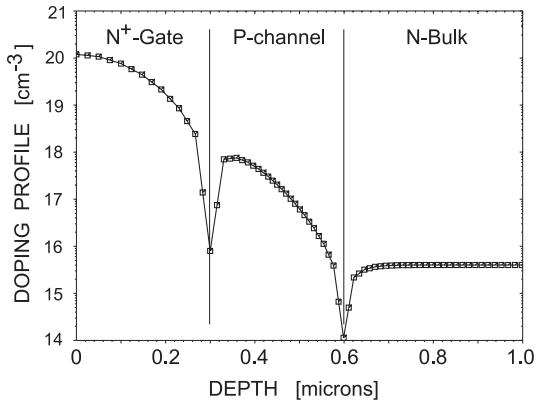


Fig. 4: Doping profile through the channel for SPJFET.

## 3. Device Modeling

JFETs described in the previous section were analyzed by device modeling with 2D numerical simulator MEDICI. All modeling results shown in this work are calculated for room temperature (300*K*). Calculated SPJFET characteristics for the device presented in Fig. 1, and for doping profile shown in Fig. 4, are presented in Fig. 5. Due to device isolation explained in the previous section, bulk voltage is hold on a maximal fixed positive value ($V_{BS}$ = +5 $V$ in this case). Channel length is supposed in this case to be $L$ = 5 $\mu m$. Current is always calculated per micrometer of structure width. Consequently, for channel width $W$ = 100 $\mu m$ the current scale is in [$mA$]. As can be observed in Fig. 5, pinch-off voltage for the doping profile shown in Fig. 4 is $U_P$ = 2.5 $V$.

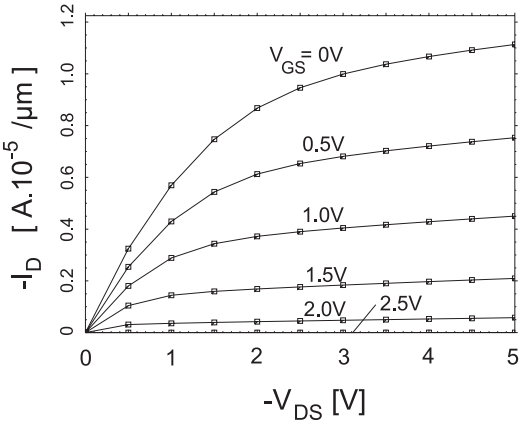


Fig. 5: Calculated SPJFET characteristics ($V_{BS}$ = +5 $V$ in this case).

More accurate insight into the device operation can be obtained by analyzing the distribution of different quantities of importance through the structure. As an example, JFET structure together with equipotentials, current flow and depletion layers is presented in Fig. 6. All dimensions in Fig. 6 are given in micrometers [$\mu m$]. Light colored regions are P-type and dark regions are N-type. Equipotential lines are instructive for 2D overview of regions in the structure with high electric field, for example critical for breakdown-smaller separations between equipotential lines indicates regions of higher electric fields. It can be observed in Fig. 6 that region with largest electric field is in the curved part of the Gate-Drain junction. Measurements on fabricated structures confirmed that SJFET breakdown indeed initiates in this part of the structure. In Fig. 6, dominating channel current and related crowding in nondepleted region of the channel can also be observed (for details, zooming must be performed). In Fig. 6, due to logarithmic scale for currents chosen in this plot (local current density magnitude is in logarithmic relation with its arrow length), it is possible to observe in the same plot also small leakage currents going into the bulk.

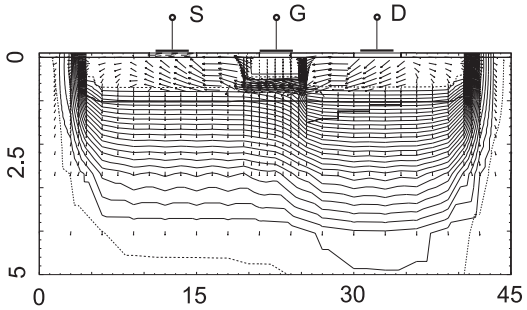


Fig. 6: SPJFET structure, equipotentials, depletion layers and current flow.

In structures where leakage is too large for adequate device isolation, what is especially critical in case of strong carrier

generation such as photogeneration in photodevices, impact generation in radiation detectors etc., the fabrication of SJFET devices and circuits on thin micromachined membranes [2] instead of structures on bulky wafers seems to provide low leakage, due to its proportionality to the generation region volume and thus approximately to silicon wafer thickness. Processing in this case is based on standard micromachining procedures, similar to the fabrication of silicon piezoresistive pressure sensors where on a thin silicon membrane made by micromachining procedures, four diffused resistors are connected in a Wheatstone bridge [3].

## 4. Circuit Modeling

Device simulation is followed by circuit simulation. In our case, circuit simulation is a direct continuation of the device simulation. Several circuit properties at 300*K* were studied to get insight into the SJFET circuits operation as well as into the modeling capabilities. In the following, circuit modeling approach and some of the simulation results will be reviewed.

In circuit simulation section, we apply 2D numerical simulator MEDICI Circuit Analysis Advanced Application Module /CA AAM/ [4] that joins together SPICE like circuit analysis with 2D numerical device modeling for device characteristics determination. So, in this case of device modeling based circuit simulation, no approximate, Spice-like models for the device description and related, often demanding and time consuming model parameters determination that is a possible source of incorrectness, is necessary. To illustrate this approach, Circuit Analysis AAM in MEDICI combining simulations of independent JFETs together with lumped circuits elements (resistors, capacitors etc.) was used for the analysis of a differential amplifier circuit performance.

Differential amplifier circuit under observation, as introduced into the numerical simulator, is presented in Fig. 7 and according semiconductor structure is shown in Fig. 8. It is a standard two input, one/two output differential amplifier circuit, based on PJFETs from previous section. Therefore, active transistors JFET1, JFET2 are PJFETs described in the preceding chapter, the other circuit components are input gate supply voltages $V_{G1} = V_{G2} = +0.5\ V$, common drain supply voltage $V_{DD} = -5\ V$, bulk voltage $V_B = +5\ V$, drain resistances $R_{D1} = R_{D2} = 150\ k\Omega$ and current generator resistance $R_g = 75\ k\Omega$.

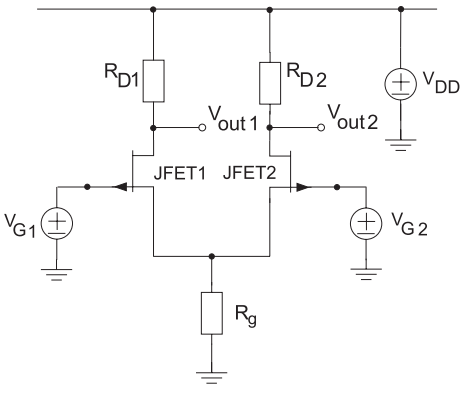


Fig. 7: Differential amplifier circuit.

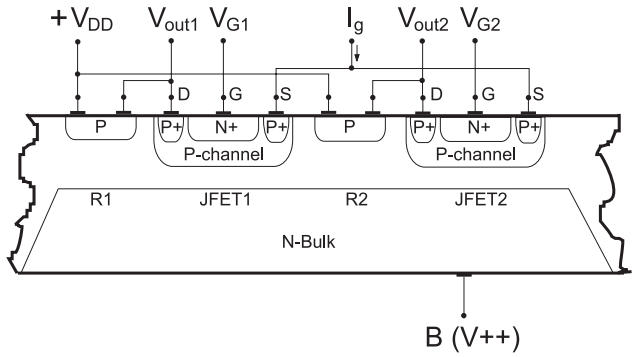


Fig. 8: Semiconductor structure of the differential amplifier.

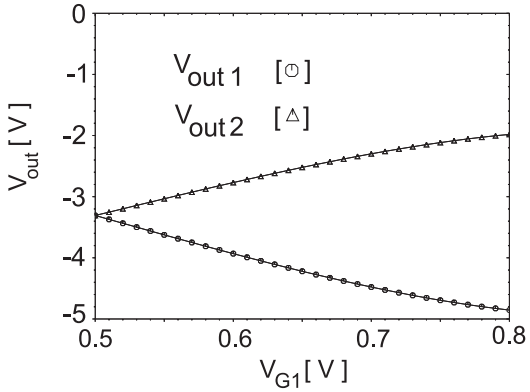


Fig. 9: Calculated voltage transfer characteristics of the differential amplifier ($V_{in} = V_{G1}$ , $V_{DD} = -5\ V$, $V_{BS} = +5\ V$).

Using described features of MEDICI, static operation of differential amplifier circuit is studied for applied voltage ramp $V_{in} = V_{G1}$ , varying from 0.5 *V* to 0.8 *V*. The response, calculated DC transfer characteristics $V_{out1}$, $V_{out2}$ vs. $V_{in} = V_{G1}$ of the amplifier circuit, are shown in Fig. 9.

All simulations were performed on HP Apollo 9000/720 system. As an indication of the computer time consumption, CPU time needed for the complete circuit analysis of differential amplifier voltage transfer characteristics shown in Fig. 9, is around 20 *min*.

## 5. Experimental

Different test SJFET structures were fabricated, following the layout rules presented in Fig. 3. Starting material were N-type silicon wafers, Phosphorus doped, $N_D = 4 \times 10^{15} cm^{-3}$ , one side polished, orientation (100). SJFET test structures were fabricated by standard bipolar discrete device technology. Special attention during the fabrication process was paid to low pn-junction leakage currents [56] to assure good device isolation.

First, source and drain regions were fabricated. Then, P-channel was fabricated. This was followed by $N^+$-gate fabrication. Here, the crucial step in the proposed process for the SJFET fabrication is performed: selective thin/100*nm*/-thick/500*nm*/ oxide etch, resulting in SAG fabrication by $N^+$-Gate diffusion into P-Channel, through essentially the same

oxide window in the channel (Figs. 1, 2 cross-section).

Different SJFET test structures were designed and fabricated, for various channel lengths ($L$) and channel width ($W$) vs. length ($L$) ratios ($W/L$). In Fig. 10, the structure of a fabricated test SJFET (channel length L = 40 $\mu m$, channel width W = 400 $\mu m$) is shown.

## 6. Measurements

DC characterization of fabricated test SJFET structures was performed with PC controlled parametric analyzer HP4145B. Measured output I/V characteristics for the example of a test SPJFET with channel length $L$ = 40 $\mu m$ and channel width $W$ = 400 $\mu m$ are presented in Fig. 11. Different channel pinching properties for modeled and measured structure are mainly due to differences in the doping profile of the fabricated structure. Taking into account the strong dependence of pinch-off voltage $V_P$ on the variation of the actual channel doping profile, it is concluded that measured characteristics are in reasonable agreement with modeling results. Measurements on test SJFET structures from two consecutive runs revealed good repeatability of the SJFET process.

## 7. Summary

Self-Aligned Gate JFET (SJFET) devices and circuits were reviewed. Electrical isolation between devices on the same chip is in this case realized through the Self-Aligned Gate approach. By this approach, electrical isolation of the devices on one chip, enabling integration is realized with simple, bipolar discrete device technology. Therefore, in this approach no epitaxial step, usually introducing inconveniences such as increased number of fabrication steps, higher temperature budget, leakage problems, higher cost etc., is necessary. Taking into account others, generally accepted properties of FET structures (low noise, radiation hardness etc.), it is concluded that SJFET structures are appropriate for applications in specific smart sensors and microsystems.

To get a deeper insight into the electrical operation of SJFET devices and circuits, initially SJFET devices are analyzed by 2D numerical device simulator MEDICI. This is followed by device modeling based numerical circuit simulation of SJFET circuits, again originating in possibilities of 2D device simulator MEDICI. So, circuit modeling in this case is a direct continuation of the previous device modeling, enabling thus the exact analysis of circuit properties in dependence of basic semiconductor device structural parameters (geometry, doping profiles etc.). As an example, a SJFET differential amplifier circuit modeling is reviewed.

On the basis of modeling, different test SJFET structures were designed, fabricated and characterized. Measurements on fabricated test SJFET structures revealed reasonable agreement with modeling.

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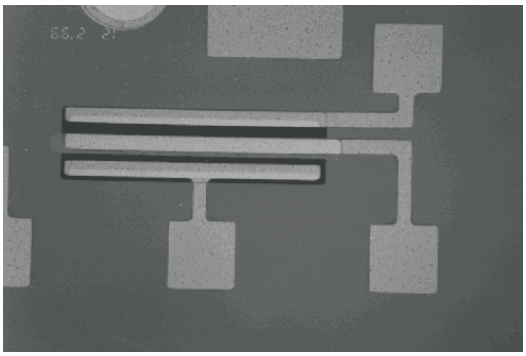

Fig. 10: Fabricated test SPJFET (channel length $L$ = 40 $\mu m$, channel width $W$ = 400 $\mu m$).

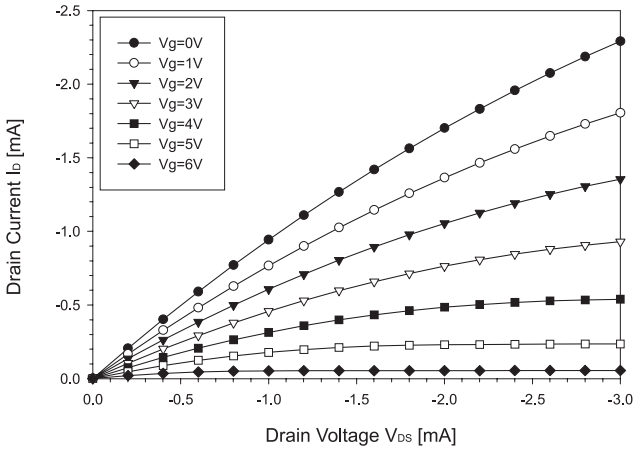


Fig. 11: Test SPJFET measured characteristics.

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