Substrate Coupling Trends in Future CMOS Technologies

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Abstract- Coupling through common silicon substrate has become an important limiting factor in high-performance mixed-signal ICs. A study of the evolution of this type of interaction with technology scaling down is presented in this paper. The level of noise when devices and parasitic elements are scaled down is obtained for a typical situation. High performance and low power scaling scenarios are considered, together with highly and lightly doped substrates. Previously, the best biasing strategies for each kind of substrate are determined. Results show that, as far as power-supply voltages are kept constant, noise will increase as devices are scaled down. When V_{dd} is reduced, the amount of noise drops drastically, leading to an increase in signal-to-noise ratio for next-years technologies.

I. INTRODUCTION

In the recent years, feature size reduction and better processing quality has allowed the integration of complex mixed-signal systems in single monolithic ICs. This has taken advantages in reliability and cost reduction, but digital and analog parts sharing some elements of the IC implies interaction between both parts, and analog signal degradation problems. Noise in power-supply lines or simultaneous switching noise (SSN) is one of the major sources of trouble, and digital and analog power trees must be split to achieve better isolation. Nevertheless, the common substrate biased by different ground lines provides a path for SSN to affect distant sensitive circuitry. Furthermore, switching devices inject noise to substrate through the depletion capacitances, which adds to the noise injected by the contacts. A number of circuits have been reported, mainly A/D converters, that showed performance limitations due to substrate coupling [1], [2], while measures to prevent this interaction are now a common practice in mixed-signal design, and tools that evaluate coupling effects for a given layout are appearing [3], [4].

The increasing speed and density of integration have worsen the problem. Forecasts for scaling of CMOS technology show an increase in circuit speed, but also a continuous voltage reduction due to reliability limitations. Taking into account these forecasts, a study of the trend of noise coupling for future CMOS

technologies is done in this work. Since the type of substrate and its biasing are of crucial importance, both lightly (P-) and highly (P+) doped substrates are considered in the work, and an evaluation of the best biasing strategies is done before the analysis of noise scaling down.

In section II, the general conditions of the study are presented: the approach followed in the analysis, the determination of the biasing strategies, and the characteristics of the scaling scenarios. In section III, the results obtained are showed for both types of substrates. For heavily doped substrates, it is shown how the characteristics of packaging can help to reduce noise drastically. For lightly doped substrates, the trend obtained is compared against that shown by a popular family of digital CMOS technologies.

II. Description of the Analysis

A. Situation analysed

A typical mixed-signal situation, consisting of a number of switching inverters disturbing a saturated transistor, is to be studied. A layout of 21 inverters and another sensitive transistor 50 μm away is generated following a 1–μm process rules, and parasitic capacitances between all nets are extracted. All transistors have an aspect ratio of 10/1, and the inverters and the sensitive device are powered by different lines. Of all the capacitances extracted, only those between *Vdd* and *GND* have shown to be of significance. Each inverter is loaded with the gate capacitances corresponding to another equal size inverter. These load capacitances and those between power-supply lines are the only ones that will be scaled down.

Substrate resistance extraction is achieved using a two-dimensional device simulator (MEDICI [5]). Given that silicon is three dimensional, only the resistances between adjacent contacts or transistors are considered. This approach is being followed by modern substrate resistance extractors [4], [6]. Resistances between non-consecutive elements are usually little significant and add complexity to the extracted circuit. As an example, if we consider the layout in Fig. 1, resistance between adjacent transistors is obtained simulating the cross-section along axis A, taking into account the width of the transistors *W*. A simulation along axis B gives the resistance between two contacts, and another one along axis C provides resistance between a contact and a transistor. If a guard ring is placed between two transistors, like happens along axis D in the figure, the resistance between each transistor and the ring and that between both transistors must be obtained. Given the regularity of the layout taken as a reference, a few simulations will provide all the resistances of interest. Obviously, the approach presented skips some three-dimensional effects in the calculation of resistances, but the approximation is good enough for our analysis.

Modeling a lightly doped substrate with lumped resistances is usually not recommended because of the distributed nature of currents in such case. Nevertheless, in [7] it is shown how the approach is also suited for these P-wafers if the biasing is good enough, with a sufficient number of contacts. When substrate is highly doped, the resistance of each element to bulk through the epitaxial layer is also extracted.

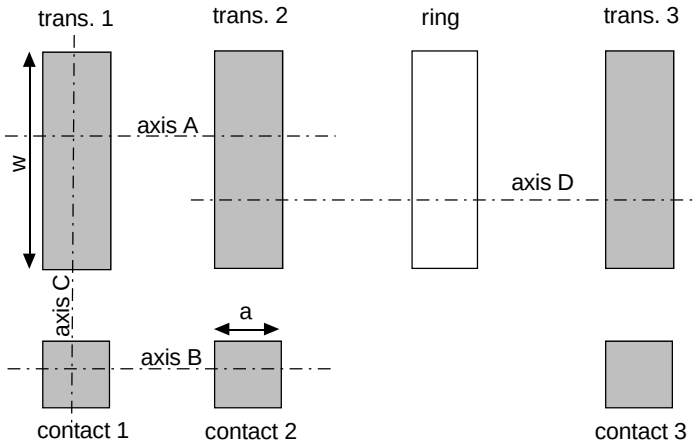

Figure 1.- To extract resistances between pairs of elements, two dimensional simulations are done along vertical sections of the layout.

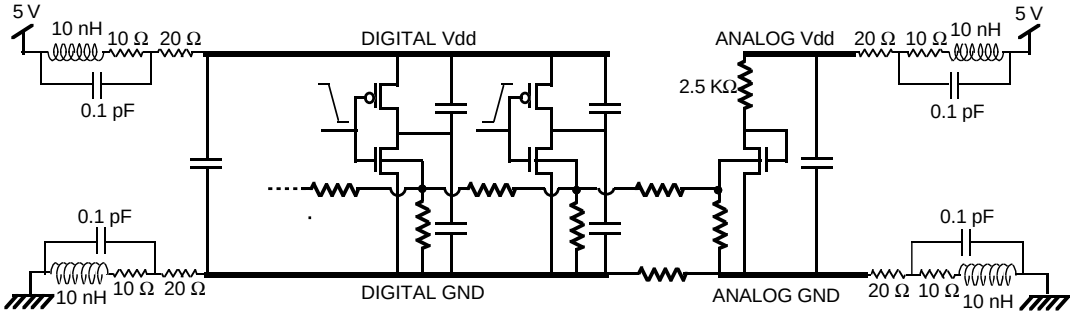

Figure 2.- Diagram of the situation analysed, including parasitic elements for the substrate and package pins, lightly doped substrate biased by the digital (left) and analog (right) ground lines.

All the noisy inverters are driven by a square clock with 0.25 ns rise/fall time, half of them switching counter-phase. All the power-supply nodes are connected to package pins with 10 nH inductance. A diagram of the resulting circuit is shown in Fig. 2, assuming contacts connected to digital or analog *GND* lines. In section II.B, the possibility of connecting those contacts to a dedicated line will be considered. It can be seen in the figure that no resistances are extracted in the wells. Those resistances are usually an order of magnitude larger than those of the bulk, and results obtained show very little difference when they are skipped. Furthermore, the analog and the digital sections have independent wells. In heavily doped substrates, a resistance from every NMOS or contact to P+ bulk should be added in the diagram. Bulk is then considered as a single

circuit node, given its high conductivity. The value extracted for the capacitance between digital power lines is 0.3 pF, and that for analog ones is 0.025 pF, both values for a 1 μm technology and the layout of reference.

B. Choosing the best biasing strategy.

With the circuit and parameters extracted for a 1 μm technology, a number of simulations are performed connecting the contacts either to the digital *GND*, the analog one, or a *GND* line exclusively dedicated for biasing purposes. The effect of placing a guard ring between coupled sections is considered, and also the presence of a backplane in P+ substrates. Fig. 3 shows the results obtained, with noise in the drain of the sensitive device in terms of its RMS value over a 10 ns period.

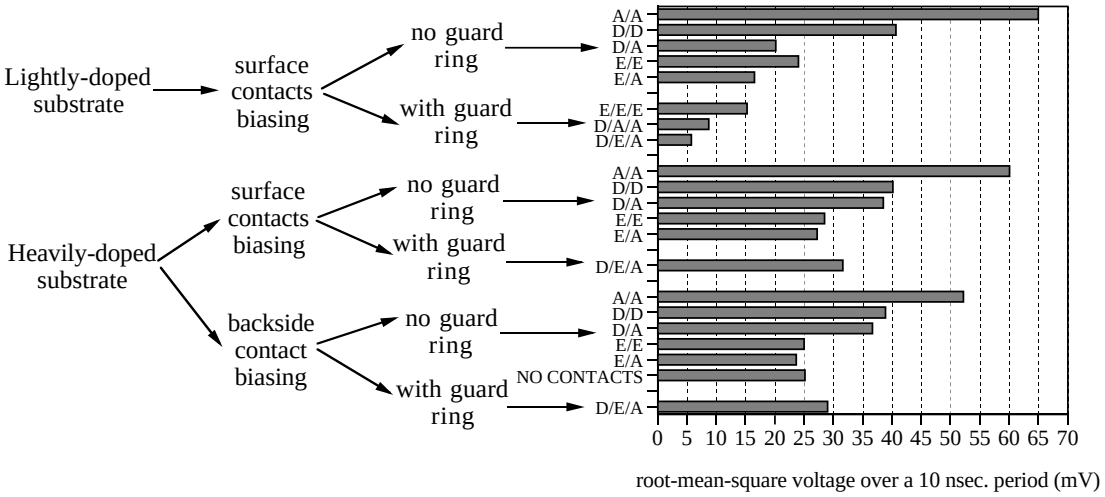

Figure 3.- Comparison of the noise coupled in function of the different biasing approaches and substrate type.
Labels: Biasing of digital section/(Biasing of guard ring)/Biasing of analog section.
D stands for "digital *GND*", A stands for "analog *GND*", and E for "dedicated *GND*".

In the layout taken as a reference, there are as many contacts as inverters. This means a very low equivalent resistance between noise sources and contacts, so any power line connected to the contacts in the digital section will become severely contaminated. This implies that if a single rail is used to bias all contacts in the layout, noise will be transmitted from the digital to the analog part through this line. This can be easily seen in Fig. 3 for lightly doped substrates. Moreover, in the circuit taken as a reference, the PSRR of the sensitive device is very low, so if the analog ground is used to bias all contacts, we get the largest amount of noise at the sensing node. In P- substrates, the best biasing approach is connecting contacts in each section to their corresponding ground, and the presence of guard rings is particularly effective. It should be noted that when three different grounds are used to bias all contacts and rings, the best results are

obtained, mainly because we get more isolation between noisy and sensitive section, and because the equivalent impedance of the ground pins is reduced.

In P+ substrates, heavily doped part offers a low-resistive path for noise to transmit to distant sections in the IC. This is why splitting the biasing network is no longer effective. Not very much can be done if the substrate is biased only with contacts at the surface. Even guard rings do not reduce noise, because the disturbance flows below the epi-layer. The best alternative that exists to minimise noise in this type of wafers is to bias the P+ part of the bulk with a grounded backside contact. This will allow skipping the contacts in the digital section, that add no advantage from the noise reduction viewpoint due to the presence of SSN. In Fig. 3 not much difference is seen between using a backside contact or not. This is because in the layout taken as a reference, the noisy section is made up of a relatively large number of noise sources (21 inverters with a 10/1 aspect ratio), that form a very low equivalent resistance to P+ bulk. This way, a sort of voltage divider is formed with the resistance through the epi-layer, and the impedance of the backside contact pin, as shown schematically in Fig. 4. If the upper resistor of the divider is low, which will depend on technological (epi-layer thickness, resistivities) and layout parameters (number and size of the inverters), impedance of the pin must be minimised. This can be achieved lowering the equivalent inductance of this node to the external "ideal" ground, by accurate package and pin selection, multiple wire-bonding, and multiple pin assignment. As an illustration, noise dependence on backside contact pin inductance is shown in Fig. 5, for a P+ substrate with no contacts at the digital section. It can be seen that noise decreases continuously with inductance, but the decrease is especially strong below the value (around 2.5 nH) that makes both impedances of the voltage divider comparable.

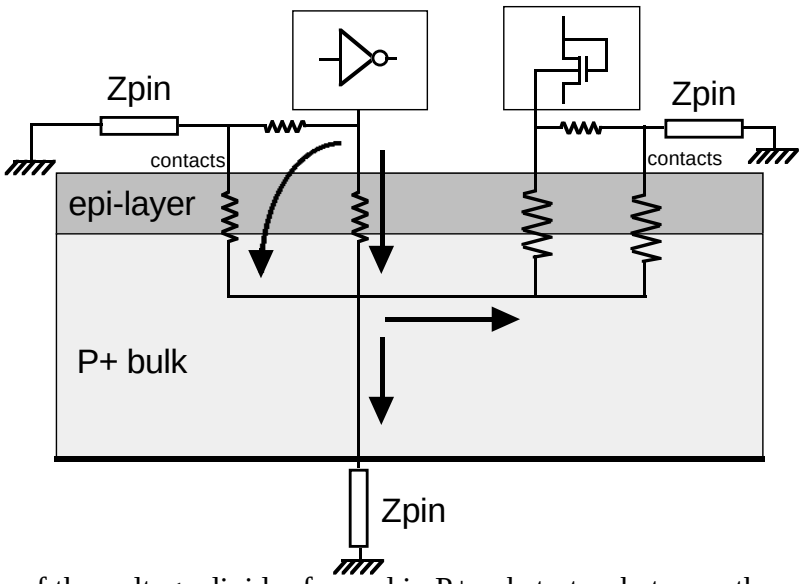

Figure 4.- Schema of the voltage divider formed in P+ substrates, between the resistance through the epi-layer, and the impedance of the backside contact pin.

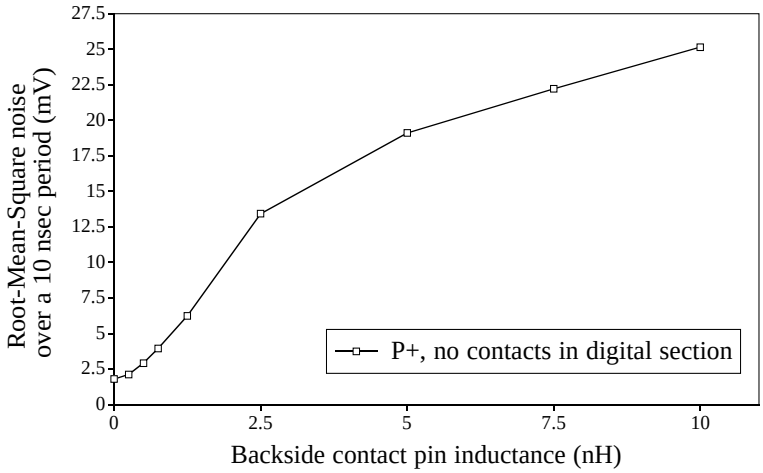

Figure 5.- Noise dependence on backside contact pin inductance. Under a certain limit, bounce in the P+ region is drastically minimised.

C. Scaling scenarios.

Up to the early nineties, technology followed a constant-voltage scaling scheme, due to the reluctance to move from standarized voltage levels, and because of the lose of performance (speed, leakage) that voltage-scaling implies. Due to reliability constraints introduced by high electric fields, a constant-field scaling scheme is starting to be followed, with voltages scaled as well as physical dimensions [8], [9]. On the other hand, portable appliances demand minimum power consumption, which cannot be achieved together with maximum speed. This way, forecasts for immediate future technologies describe two scaling scenarios [9], [10]: a high-performance scenario, in which voltages are optimised for maximum speed while maintaining device reliability; and a low-power scenario, in which supply voltage is selected to maintain a constant power density in the IC while scaling down.

Gate length	2 μm	1.5 μm	1 μm	0.7 μm	0.5 μm	0.35 μm	0.25 μm	0.2 μm
Substrate doping (N_{sub})	1e16	1.3e16	2e16	2.86e16	4e16	5.7e16	8e16	1e17
Gate oxide (t_{ox})	400 Å	300 Å	200 Å	140 Å	100 Å	70 Å	50 Å	40 Å
High Performance scenario:								
Supply voltage (V_{dd})	5	5	5	5	3.3	2.5	1.8	1.5
NMOS Threshold (V_{ton})	0.76	0.76	0.76	0.76	0.5	0.38	0.27	0.23
Low Power scenario:								
Supply voltage (V_{dd})	-	-	-	3.3	2.5	1.8	1.3	1
NMOS Threshold (V_{ton})	-	-	-	0.5	0.38	0.27	0.2	0.2

Table I.- Summary of the values taken by the most relevant parameters for the two scaling scenarios, taking 1 μm technology as a reference.

Both scaling scenarios are considered in this work. HSPICE level 6 parameters for a 1 μm process are taken as a reference. In the low-power

scenario, supply voltage is scaled along with channel length for technologies beyond 1 μm, while in the high performance scenario voltages are kept constant until 0.7 μm, and afterwards they are scaled with geometry to keep an electric field across gate oxide of approximately 3.5 MV/cm. Threshold voltages are scaled together with supply voltage, with a limit at $V_t \approx 0.2$ V [9]. Vertical dimensions are always scaled by the same factor as device geometry, and substrate doping is increased by the same factor, too. Junction capacitances are scaled according to their dependence on substrate doping and junction depth. Table I summarises the values taken by the most relevant parameters.

III. SUBSTRATE COUPLING TRENDS

A. Lightly-doped substrates

Noise measured at the sensitive device drain against gate length is shown in Fig. 6. All layout dimensions are scaled together with gate length. Capacitances extracted are scaled taking into account their nature -oxide capacitances, junction capacitances-, while resistances are re-extracted for every technology. Substrate is biased with digital *GND* in the noisy section and analog *GND* in the sensitive section, all pins modeled as shown in Fig. 2. It can be seen that constant-voltage scaling has taken a continuous increase of substrate coupling importance, mainly due to faster transients in digital circuits. Nevertheless, as supply-voltages start decreasing, noise peaks decrease drastically. This trend is checked comparing the results with that obtained using the device models of available technologies -not scaled models- of a popular digital CMOS family.

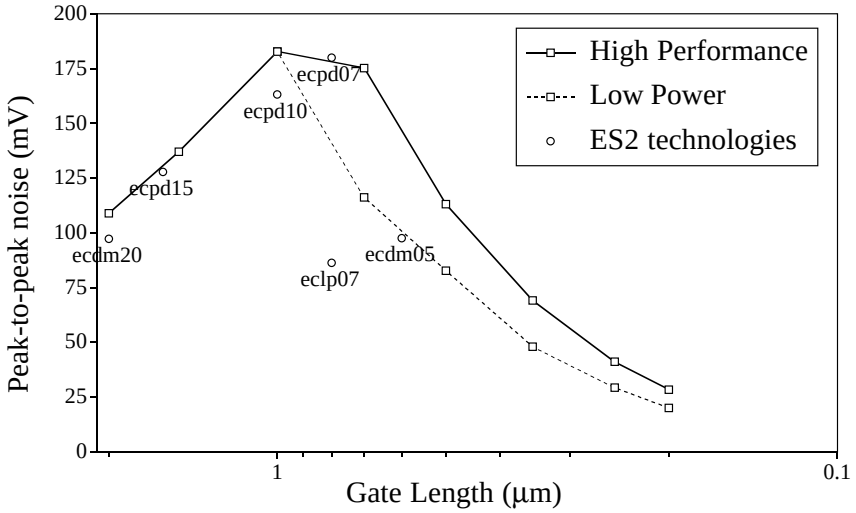

Figure 6.- Predicted trends for substrate noise in future technologies, lightly doped substrates.

In Fig. 7 the ratio between supply voltage and noise amplitude is represented. According to this figure, the noise decreases faster than voltages in the IC, which implies that signal degradation will stop in the next years, and SNR

will increase. This can be explained by the fact that transient times do not decrease as predicted by theoretical constant-field scaling, due to carriers velocity saturation. Furthermore, current across devices saturates too, decreasing SSN which is the main source of noise. Another aspect to be noted in Fig. 7 is that SNR is approximately the same for both scaling scenarios.

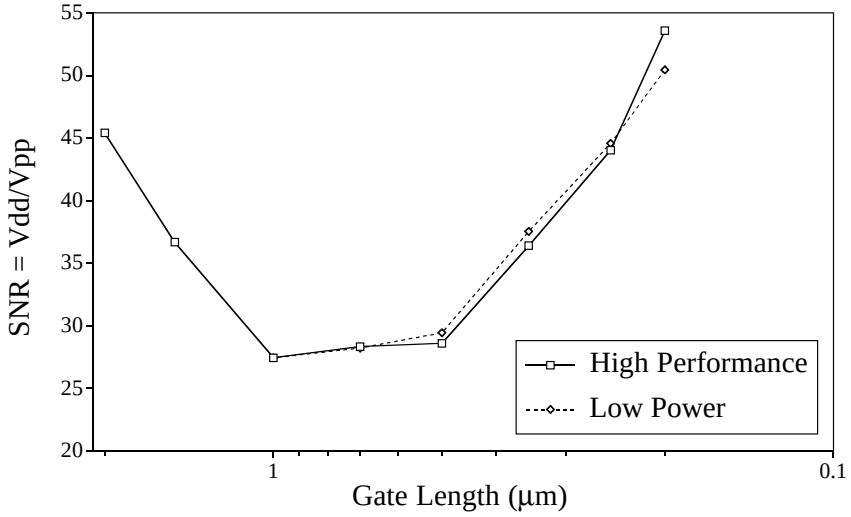

Figure 7.- Expected evolution of signal degradation due to substrate coupling.

B. Highly-doped substrates

Results obtained for highly doped substrates are shown in Figs. 8 and 9, for the same circuit and scaling criteria as in P- type. Wafer characteristics like thickness, P+ bulk resistivity, or epitaxial layer thickness are kept constant. Substrate is biased with a backside contact with an associated pin inductance of 2.5 nH, and there are no contacts in the digital section to minimise noise as results from section II.B. Trends are fairly similar to that shown for lightly doped substrates. Anyway, it can be seen how, for past technologies with constant voltage scaling, noise level remains steady, while the decrease trend for

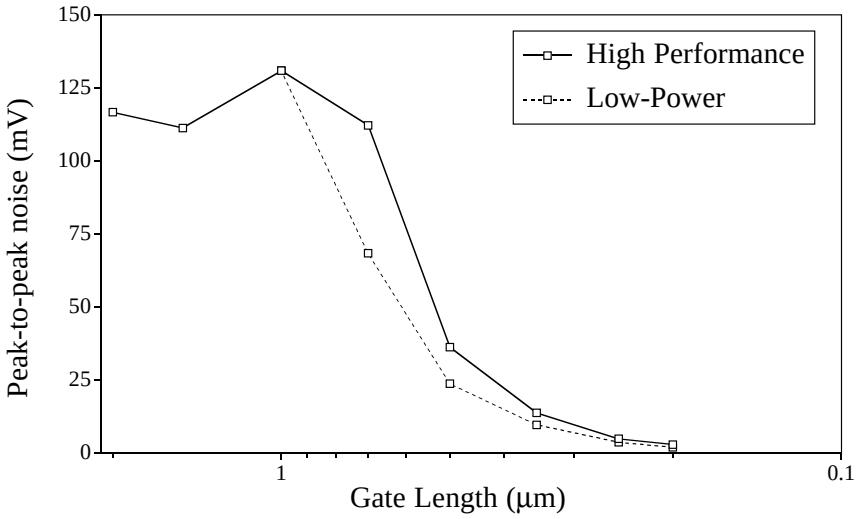

Figure 8.- Predicted trends for substrate noise in future technologies, highly doped substrates.

voltage-scaled processes is stronger than in P- substrates, leading to a higher SNR, and very low noise levels for deep submicron. This is due to the fact that, as feature size is reduced, resistance of any device to P+ bulk through the epi-layer increases roughly by the scaling factor, while the package pin impedance is independent of scaling. As a consequence, P+ bulk is more isolated from devices as the size of those devices is diminished, resulting in a better grounding and a higher isolation between coupled parts.

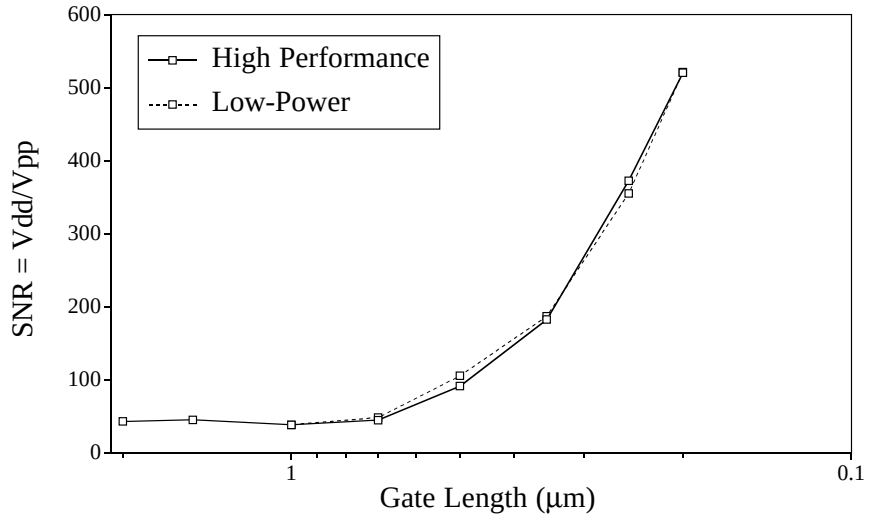

Figure 9.- Expected evolution of signal degradation due to substrate coupling.

IV. CONCLUSIONS

An analysis of substrate coupling evolution with technology scaling down has been done in this paper. Previously, the best biasing strategies for mixed-signal circuits manufactured in lightly doped or in heavily doped wafers have been determined. It has been seen that, in both kinds of substrates, digital and analog section should not be biased with the same power rails, because they would provide a low-resistance path for noise to affect distant devices. In P- wafers, biasing each section with its corresponding ground line is advised, and guard rings are recommended, especially if biased with a dedicated line. In heavily doped substrates, highly conductive bulk provides a path for noise to affect distant devices. This means that the main objective should be to ground this P+ bulk as well as possible. This can be achieved with a die backside contact minimising the impedance of the associated pins. If this approach is followed, contacts in the digital section can be skipped, since they are connected to a line contaminated with SSN and inject noise to the bulk.

It is predicted that substrate coupling trouble will decrease in the next years, due to the predicted scaling of power-supply voltages together with feature size. Up to now, constant-voltage scaling implied an increase in transient speed and a larger amount of noise generated. In deep submicron technologies, reduced

voltages and velocity saturation effects will imply smoother slopes in voltage transients, lower noise levels, and higher signal-to noise ratios. In heavily doped substrates, the trend is even more clear because reduced feature size takes an increase of the impedance between the noise sources in the wafer surface, and the heavily doped bulk.

ACKNOWLEDGEMENTS

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