RF/Wireless Interconnect for Inter- and Intra-Chip Communications

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Invited Paper

Recent studies showed that conventional approaches being used to solve problems imposed by hard-wired metal interconnects will eventually encounter fundamental limits and may impede the advance of future ultralarge-scale integrated circuits (ULSIs). To surpass these fundamental limits, we introduce a novel RF/wireless interconnect concept for future inter- and intra-ULSI communications. Unlike the traditional "passive" metal interconnect, the "active" RF/wireless interconnect is based on low loss and dispersion-free microwave signal transmission, near-field capacitive coupling, and modern multiple-access algorithms. In this paper, we address issues relevant to the signal channeling of the RF/wireless interconnect and discuss its advantages in speed, signal integrity, and channel reconfiguration. The electronic overhead required in the RF/wireless-interconnect system and its compatibility with the future ULSI and MCM (multi-chip-module) will be discussed as well.

Keywords*—*Adaptive networking, bidirectional interconnect, fault-tolerant computing, interconnect reconfiguration, inter- and intra-chip communications, multi-I/O interconnect, RF/wireless interconnect, ultrabroad bandwidth.

I. INTRODUCTION

For the past three decades, the performance of integrated circuits has depended primarily on device properties. To enhance the circuit and system performance, the major effort has been focused on improving the device speed through scaling of device dimensions. The decrease in minimum feature size of devices has led to a proportional decrease in interconnect cross-sectional area and pitch. The parasitic resistance, capacitance, and inductance associated with interconnects are beginning to influence the circuit performance and have increasingly become one of the primary showstoppers in the evolution of deep submicrometer ULSI technology. Recent studies indicated that, below 1-μm minimum feature size, the interconnect parasitics seriously hurt circuit and system performance [1]–[3]. The scaling results, from signal attenuation and dispersion in wires, show that electrical interconnects become more difficult once the bit-rate capacity exceeds $\sim 10^{16}\ A/l^2$ (or $\sim 10^{17}\ A/l^2$ by equalizing the channels [4]), where A is the cross-sectional area of the interconnect wiring and l is the length of the wire. The RC (or LC) time delay, IR voltage drop, CV^2f power loss, and the crosstalk of wires become significant as well.

For the past few years, a great deal of work has been focused on improving the conventional interconnect technology by reducing the resistivity of conductors (using copper) and reducing the dielectric constant of interlayer dielectric materials (by using low-κ polymers). Nevertheless, these evolutionary approaches may soon encounter fundamental material limits [5]. Revolutionary methods and techniques must be pursued to carry on the fast progress of the future ULSI technology. One of such possibilities is to use "active" RF/wireless interconnects.

II. RF/WIRELESS INTERCONNECT

A. System Concept

With appropriate designs, RF/microwave signals can be transmitted efficiently through either free space or guided mediums. Free-space signal broadcasting/receiving has become a common practice in modern wireless systems due to its excellent channeling capability and low-cost implementation. However, the efficient transmission and receiving of RF/microwave signals in free space require the size of antennas to be comparable with their wavelengths. As the CMOS device dimensions continue to scale down, operating speeds and cut-off frequencies (f_t and $f_{\max}$) of CMOS devices will exceed 100 GHz in the near future. But, even at this frequency, the optimal aperture size of the antenna is on

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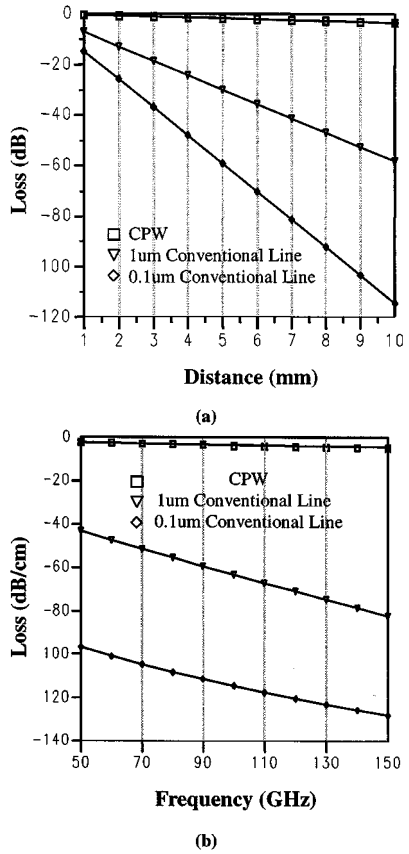


Fig. 1. (a) Attenuation of RF/microwave signal (100 GHz) via CPW and conventional ULSI interconnects as a function of distance. (b) Attenuation of RF/microwave signals (50–150 GHz) via the same CPW and interconnects as a function of frequency.

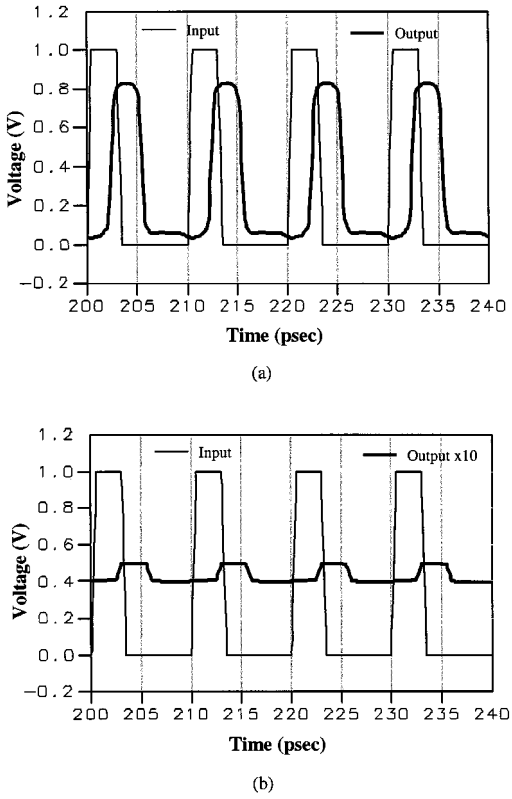


Fig. 2. Time domain simulations of RF/microwave signals (100 GHz) via (a) 1-cm-long CPW and (b) conventional 1-μm-wide metal interconnect.

the order of 1 mm^2, which is too large to be comfortably implemented in the future ULSI.

Microwave transmission in guided mediums, such as the microstrip transmission line (MTL) or coplanar waveguide (CPW), is known to have low attenuation up to at least 200 GHz [6]. Simulations in Fig. 1 indicate that signals transmitted through a 1-cm-long CPW experience extremely low loss [$-$1.6 dB at 100 GHz as shown in Fig. 1(a)] and low dispersion [$<$2 dB as shown in Fig. 1(b)] across the complete frequency range of simulation (50–150 GHz). On the contrary, the loss of conventional ULSI interconnects is very severe, up to $-$60 dB and $-$115 dB per centimeter at 100 GHz for 1-μm- and 0.1-μm-wide interconnect lines, respectively. The frequency dispersion of these interconnects also reaches 30–40 dB across the same frequency range. Time-domain simulations in Fig. 2(a) confirm the integrity of transmitted square-wave signals through a 1-cm-long CPW, in contrast to the highly deteriorated output signals of a conventional 1-μm interconnect for the same transmission distance [as shown in Fig. 2(b)]. Evidently, conventional metal lines with narrow geometry are inadequate for global interconnect applications in the future ULSI.

In order to design an RF/wireless interconnect system which may be compatible with the future ULSI and MCM, we must be very careful in choosing the appropriate system architecture and transmission/receiving components. Since the communication distance is relatively short (several centimeters apart), the sizable "far-field" antenna, for instance, can be substituted with much smaller "near-field" capacitive couplers [7]. The center/top conductor of the CPW/MTL is typically 10–100 μm wide, depending on its characteristic impedance ($Z_c = 25$–$100\ \Omega$) and other signal transmission requirements [8], [9]. Although the size is not extremely large, CPW or MTL is used more frequently in high-speed or RF packages instead of ULSI circuits. To justify its constraint in size, the CPW or MTL can be used as an "off-chip" but "in-package" transmission medium and shared by multiple ULSI I/Os.

Based on these considerations, the proposed RF/wireless interconnect system is depicted in Fig. 3 as a **miniature wireless LAN** (local-area network) located inside a MCM package. The intended miniature LAN contains ULSI I/Os as users, capacitive couplers as near-field antennas, RF circuits for transceivers, and an off-chip but in-package MTL or CPW as a shared broadcasting medium. Output signals can be up-linked to MTL or CPW via transmission capacitive couplers (C_T), then down-linked via receiving capacitive couplers (C_R) to input ports to fulfill the interconnect function. Modern code division (CDMA) and/or frequency division multiple-access (FDMA) algorithms can be used effectively to alleviate the undesired cross-channel interference within the shared medium. With orthogonal-coded and/or frequency-filtered RF transceivers, a passive MTL or CPW can be very suitable to relay ultrabroad-band signals up to 150 GHz [6], [8].

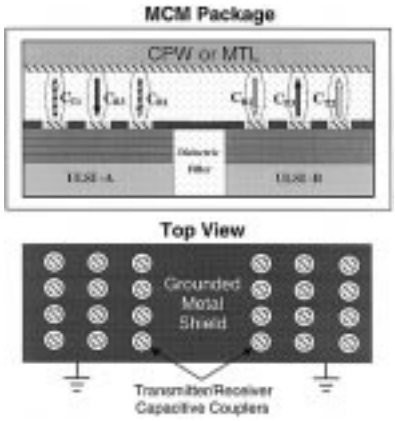


Fig. 3. ULSI chips communicate with each other through a miniature wireless LAN inside a MCM package.

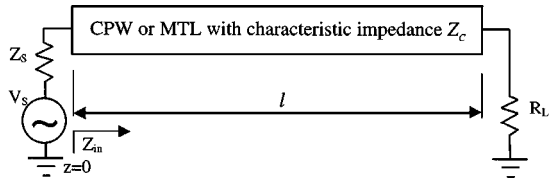


Fig. 4. CPW must be properly terminated with $R_L = Z_C$ to minimize the frequency dispersion.

B. High-Frequency/High-Speed Signal Channeling

The communication channel of the RF/wireless-interconnect system, which comprises I/O transceivers, capacitive couplers, and a shared microwave transmission medium, is analyzed to quantify the system effectiveness. Firstly, the voltage distribution of signals at any point z of the transmission medium (either CPW or MTL), as shown in Fig. 4, can be expressed as

$$V(f, z) = V^+(f, 0)\exp(-j\beta z) + V^-(f, 0)\exp(j\beta z) \tag{1}$$

where $V^+(f, 0)\exp(-j\beta z)$ and $V^-(f, 0)\exp(j\beta z)$ represent the forward and reverse traveling waves, respectively. The complex amplitudes of the traveling waves can be written as

$$V^+(f, 0) = \frac{V_S}{2Z_S}\frac{Z_C + R_L}{\left(\frac{R_L}{Z_S}+1\right)\cos\beta l + j\left(\frac{R_L}{Z_C}+\frac{Z_C}{Z_S}\right)\sin\beta l} \cdot \exp(j\beta l) \tag{2}$$

$$V^-(f, 0) = \frac{V_S}{2Z_S}\frac{R_L - Z_C}{\left(\frac{R_L}{Z_S}+1\right)\cos\beta l + j\left(\frac{R_L}{Z_C}+\frac{Z_C}{Z_S}\right)\sin\beta l} \cdot \exp(-j\beta l) \tag{3}$$

where

- Z_s impedance looked into the source;
- Z_C characteristic impedance of the transmission line;
- R_L load impedance;

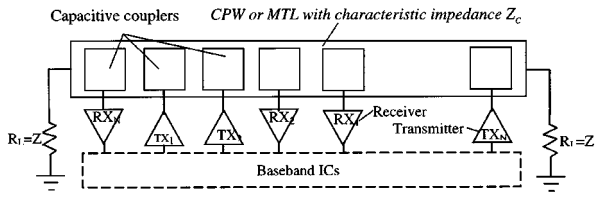


Fig. 5. A representative RF/wireless interconnect channel with multiple I/Os.

- l total propagation distance;
- β complex propagation coefficient with its real part expressed as

$$\mathrm{Re}(\beta) = 2\pi\frac{f}{c}\sqrt{\varepsilon_{\mathrm{eff}}(f)} \tag{4}$$

where $\varepsilon_{\mathrm{eff}}(f)$ represents the effective permittivity of dielectrics which surround the transmission line [6], [8], [9].

When the transmission line is properly terminated by its characteristic impedance ($R_L = Z_C$), (3) diminishes, i.e., $V^-(f, 0) = 0$, and (1) becomes

$$V^+(f, z) = \frac{Z_C}{Z_C + Z_S}V_S\exp(-j\beta z). \tag{5}$$

The resulting voltage distribution in (5) is virtually dispersion-free because the real part of β, i.e., $\mathrm{Re}(\beta)$, is almost independent of the frequency at $f < 200$ GHz [6]. The imaginary part of β, i.e., $\mathrm{Im}(\beta)$, that represents dielectric and/or radiation loss and ohmic dissipation is insignificant and can be ignored in the frequency range of interest.

Fig. 5 shows a representative RF interconnect channel shared by multiple I/Os (Rx_1 to Rx_N and Tx_1 to Tx_N). The channel consists of a uniform and homogenous CPW with its Z_C equal to 50 Ω. The signal line of the CPW is designed to be 100 μm wide with 20-μm signal-to-ground isolation gaps [8]. Since the channel is designed to hold bidirectional communications, both ends of the CPW are terminated with Z_C to avoid the signal reflection.

The equivalent circuit of a specific transceiver (Tx_N–Rx_N) loop is shown in Fig. 6, in which the signal voltage, V_{rec}, received at the Rx_N can be derived according to (5) as

$$V_{\mathrm{rec}} = \frac{\frac{Z_C}{2}R_R}{\left(\frac{Z_C}{2}+R_T - j\frac{1}{\omega C_T}\right)\left(\frac{Z_C}{2}+R_R - j\frac{1}{\omega C_R}\right)}V_S \cdot \exp(-j\beta d) \tag{6}$$

where

- V_s source signal voltage;
- d distance between the Tx_N and Rx_N;
- R_T Tx_N's output resistance;
- R_R Rx_N's input resistance.

It is very obvious from (6) that we must choose R_T and R_R to be much greater than Z_C to preserve CPWs characteristic impedance and choose $R_R \gg j(1/\omega C_R)$ and $R_T \gg j(1/\omega C_T)$ to obtain a dispersion free V_{rec}. Fig. 7 shows the

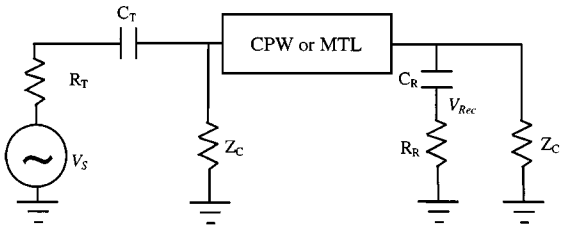


Fig. 6. Equivalent circuit for a representative transmitter–receiver loop.

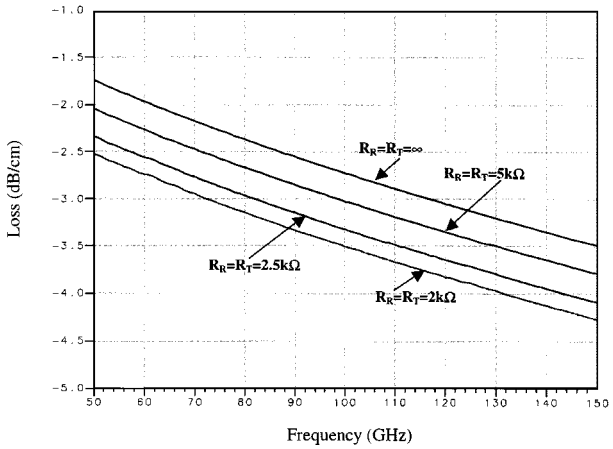


Fig. 7. Extra CPW attenuation caused by 20/20 shunted I/O transceivers.

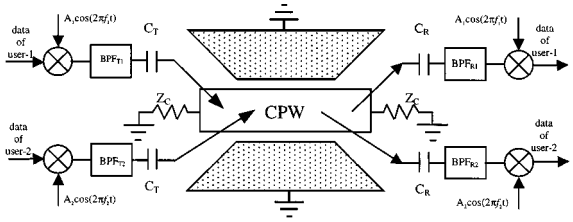
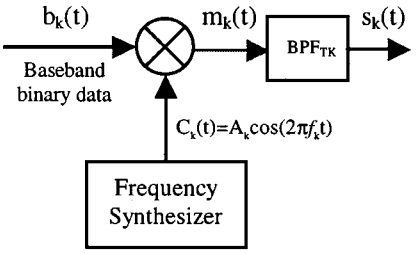


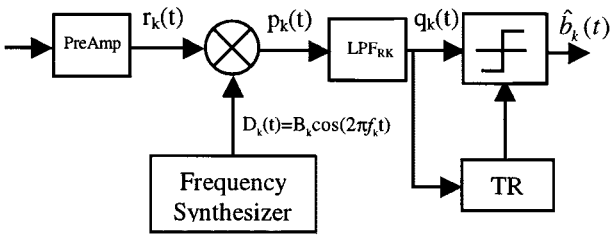
Fig. 8. Top-level schematic of a FDMA-interconnect.

impact of multiple Tx/Rx on the performance of the communication channel. The worst case is simulated by placing Tx_N and Rx_N at the opposite end of the CPW and the rest of 20/20 Tx/Rx uniformly across the transmission line. Assuming $R_T = R_R = 100Z_C$ (5 kΩ) and $1/\omega C_T = 1/\omega C_R = 0.1R_T$, we find the loss caused by shunted 20/20 Tx/Rx is 0.3 dB/cm. The loss is still as low as 0.8 dB/cm when reducing both R_T and R_R to 2 $k\Omega$.

Larger C_T and C_R help signal coupling between transceivers and the transmission line. However, the size of C_T and C_R must be made small enough in order to be compatible with the future ULSI fabrication. A good compromise can be reached by choosing $R_T = R_R = 2$ kΩ and $1/\omega C_T = 1/\omega C_R < 0.1R_T$. When operating at 100 GHz, the required C_T or C_R capacitance is estimated to be larger than 8.3 fF. Assuming the vertical coupling distance is 25 μm and using ZrO ($\varepsilon_r > 10$) as the dielectric between coupler electrodes, the pad size of C_T or C_R is calculated to be <600 μm^2. Capacitive couplers of this size can be easily implemented in future ULSI.



(a)



(b)

Fig. 9. (a) Block diagram of the FDMA-interconnect transmitter. (b) Block diagram of the FDMA-interconnect receiver.

Provided that the CMOS transmitter output stage is operated in class A and biased at $V_{dd} = 1.8$ V, the signal power received at the farthest Rx_N is calculated as $P_{\rm rec} = -[39 + 10\,{\rm Log}(L)]$ dBm according to the formula

$$P_{\rm rec} = LV_{dd}^2 Z_C^2/(8R_R R_T^2) \tag{7}$$

where L accounts for CPWs attenuation. Since the signal is virtually dispersion-free, it can be boosted to adequate power level at the receiver by CMOS preamplifiers for subsequent signal/data processing. System noise floor and receiver sensitivity must be analyzed to ensure the adequacy of $P_{\rm rec}$ for supporting low bit-error-rate (BER) communication. Such analysis is carried out in Section II-C.

C. Multiple Access Techniques for Simultaneous Communication Channels

Multiple access algorithms, such as FDMA and CDMA, can be used to achieve simultaneous communications in RF/wireless interconnects. In FDMA-interconnect, frequency bands of I/O channels may be allocated between 5–105 GHz with bandwidth of 5∼20 GHz in each channel to provide a minimum data rate of 5∼40 Gb/s, depending on the modulation scheme. The schematic of a FDMA RF-interconnect modulated by either a digital or analog carrier is shown in Fig. 8. Block diagrams of the transmitter and receiver are shown in Fig. 9(a) and (b), respectively.

In FDMA-interconnect, the kth transmitter's binary data stream $b_k(t)$ is multiplied by its sinusoidal carrier $c_k(t) = A_k \cos(2\pi f_k t)$. The resulting signal $m_k(t)$ is filtered through BPF_{TK} to form the function $s_k(t)$, which is eventually coupled into the shared CPW or MTL. At the kth receiver, input signals are boosted by a preamplifier and then demodulated to form received signal $q_k(t)$. This signal

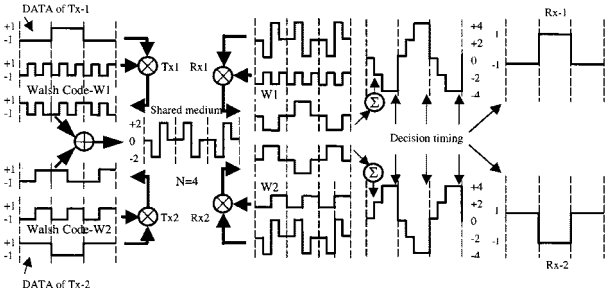


Fig. 10. Operation of a CDMA-interconnect with two I/O subchannels.

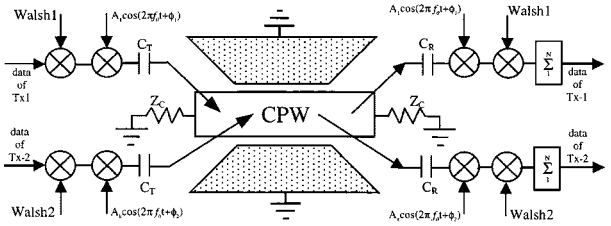


Fig. 11. Top-level schematic of a CDMA-interconnect.

is fed to a threshold comparator to recover data $b_k(t)$ sent from the kth transmitter [10].

The operation of the baseband CDMA-interconnect is illustrated in Fig. 10 with two I/O channels as an example. Outputs of Tx_1 and Tx_2 are spread first by orthogonal Walsh codes (W1 or W2, respectively) and then capacitively coupled into a shared CPW or MTL where they can be linearly superposed and broadcast to receivers. At the receiver end, the superposed signal is despread by the same Walsh codes (W1 or W2) for data recovery. Unlike the hardware-oriented FDMA-interconnect, CDMA-interconnect is easy to be reconfigured by changing spreading codes through software commands.

We may also use the CDMA-interconnect beyond the baseband by modulating CDMA signals with RF carriers as shown in Fig. 11. In this case, coherent demodulation [10] and sequence timing acquisition and tracking [11] may be used for signal recovery.

As in any communication systems, several parameters are concerned in CDMA-interconnect: the number of I/Os, i.e., the system capacity, bit rate, i.e., the transmitted signal rate, BER, which is the measure of the system performance. Let us assume the transmitted power of each Tx being well controlled and all signals are received at Rx with an equal power. If we use orthogonal codes and operate the interconnect under a synchronous access condition, the total number of I/Os is limited only by the spreading factor N as shown in (8)

$$N = \frac{F_C}{F_S} = \frac{T_S}{T_C} = G \tag{8}$$

where

N equivalent to the CDMA processing gain G;
F_S symbol rate (or CDMA subchannel data rate);
F_C chip (or clock) rate of the spreading code[11];

and the BER of the RF/wireless interconnect system is totally determined by the signal-to-noise ratio (SNR) of the receiver.

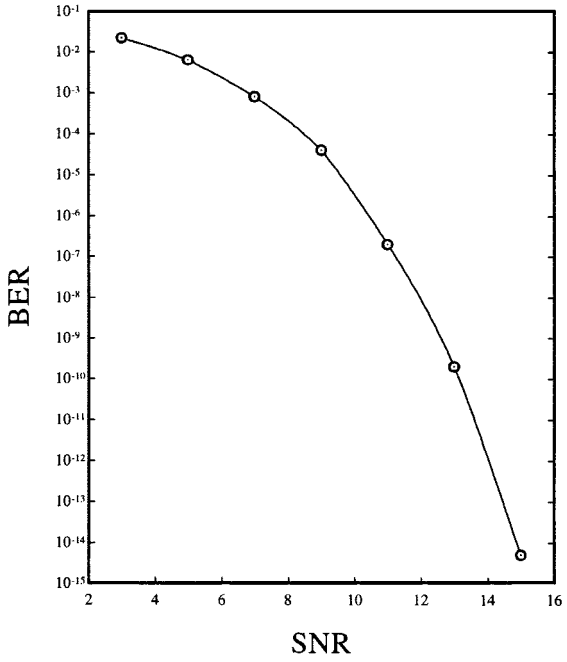


Fig. 12. BER versus SNR in CDMA-interconnect with 4 I/O subchannels.

We provide simulations that clearly establish the tradeoff and feasibility of the designed system. In our simulations, we choose processing gain to be 20 and use Walsh codes as the spreading code sequence. In this test, we consider only the case of synchronous access. Since Walsh codes are used, one may specify at most 20 I/O channels in a shared CPW. Fig. 12 shows the simulation results under various SNR. From these simulations, the system reaches an extremely low BER ($<10^{-14}$) as SNR >15 dB.

The synchronous access condition is fulfilled if the signal traveling distance during one T_c is larger than the longest span between any two Txs within the same CDMA-interconnect. Assuming the data rate is 20 Gb/s, the maximum synchronous access distance between any two Txs is limited to about 0.7 cm. In order to maintain flexibility in allocating transmitters geographically and high overall data rate (or high spectrum efficiency) of the RF/wireless interconnect, we may choose to use an FDMA/CDMA combined access system. In this system, frequency bands are divided by using different carriers while I/O data are spread within individual frequency band by using orthogonal codes. For example, we may divide 100 GHz into five 20-GHz bands to hold four CDMA I/O subchannels in each frequency band. Each subchannel runs 5–10 Gb/s/subchannel according to the modulation scheme. Under such circumstances, the signal-to-noise budget for the intended RF/wireless interconnect system is calculated and plotted in Fig. 13.

In this calculation, the noise floor is set first at the thermal limit of -174 dBm/Hz. This is valid under an assumption that the switching noise of digital circuits can be effectively blocked from the RF/wireless-interconnect by the grounded metal shield that surrounds the capacitive couplers, as depicted in Fig. 3. This assumption is supported by a recent study which measured the digital switching noise to be 10 dB

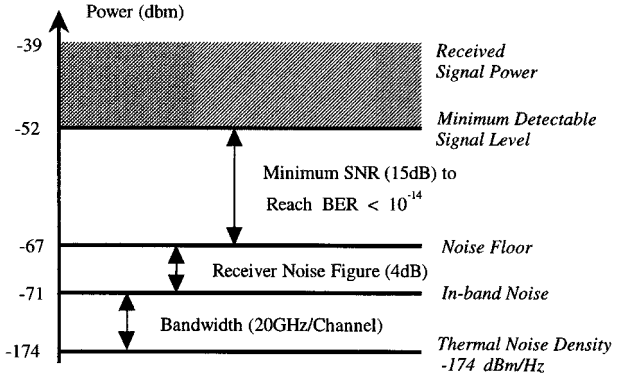


Fig. 13. Signal-to-noise budget for the intended RF/wireless interconnect system.

lower than that of the thermal noise in an open-air wireless interconnect using antenna to transmit and receive signals without shielding [12]. Based on that, the minimum detectable power per CDMA subchannel equals

$$P_{\min} = 10\,\mathrm{Log}(F_c) + N_f + \mathrm{SNR} - 174\ (\mathrm{dBm}) \quad (9)$$

where F_S is the I/O data rate and N_f is the noise figure of the receiver (assumed to be 4 dB). The minimum detectable signal level is calculated as

$$P_{\min} = -52\ \mathrm{dBm}. \quad (10)$$

This limits the maximum CPW or MTL loss to 13 dB for keeping low BER transmission. This also limits the synchronous transmission distance to about 4 cm up to 100 GHz, which is sufficiently long for most intra- and inter-chip interconnect applications. We may also utilize T/R repeaters to gain a longer synchronous access distance. The random (or asynchronous) access process, however, should be avoided to simplify the Tx/Rx architecture and circuit implementation.

D. Electronic Overhead

The electronic overhead of the RF/wireless interconnect system comprises I/O transceivers, frequency/code generators, frequency/code mixers, code correlators, clock/frequency recovery circuits, and bandpass filters. As previously described, the RF transceivers may be designed to operate in each of the separate 20-GHz bands and digital circuits are only required to clock at 20–40 Gb/s within each band. This architecture renders RF-interconnect with total 100-GHz bandwidth while relaxes challenges in wide-band transceiver and digital circuit designs for operation efficiency and signal integrity. Without such arrangement, the transceivers must work over the complete 100-GHz bandwidth with digital circuits clocked up to 100–200 Gb/s for an equivalent interconnect data throughput.

Up to date, digital circuits clocked up to 4–10 Gb/s have been demonstrated. But can CMOS operate up to 100 GHz as RF transceivers? Presently, W-band (70–110 GHz), D-band (110–140 GHz), and G-band (140–220 GHz) RF circuits have been demonstrated only by III–V MMICs based on high-performance InP–InGaAs HEMTs or HBTs with cutoff frequencies of $f_t > 300$ GHz and $f_{\max} > 600$ GHz [13], [14]. The f_t and $f_{\max}$ of today's 0.1-μm CMOS are about 60 and 90 GHz, respectively [15]. With further scaled CMOS devices, lower sheet resistance gate and enhanced electron velocity in the sub-0.1-μm regime, one may obtain CMOS devices with ultrahigh $f_{\max}$ and f_t to perform RF carrier functions up to 100 GHz in the foreseeable future. Some of the detailed implementation issues and demonstrations for RF/wireless interconnect are summarized as follows.

1) FDMA: For system simplicity, the RF/wireless-interconnect system may be implemented with a direct conversion or zero-IF transceiver architecture. Fig. 9 shows such FDMA-interconnect receiver in which preamplifiers, mixers and frequency synthesizers are key circuits to be realized. Preamplifiers with 20–30-dB gains are needed for input signal amplification. Balanced or double balanced active mixers, such as the Gilbert cell, may be used for modulation and demodulation functions. It is advantageous to use a noncoherent detection scheme for simple receiver implementation. Frequency shift keying (FSK) is a possible choice.

Bandpass filters are needed in FDMA-interconnect to minimize cross-band interference. The implementation of low-loss and high-selective filters requires high-Q (>50) inductors. The spiral type inductors in silicon RF ICs are generally with very low Q (about 2–10), depending on the inductance. High-Q and tunable inductors are very difficult to realize due to significant energy loss to the conductive silicon substrate. Fortunately, these issues have been partially resolved by using a transformer-type inductor design, in which the lost energy is recovered via a secondary inductor with delayed phase angles to attain extremely high Q (>1000) inductance and high tunability (0%–100%) [16]. Based on this technique, a 5-GHz elliptical filter is being designed as shown in Fig. 14. The bandwidth of the filter is simulated to be 2 GHz with 1-dB passband insertion loss and 22-dB stopband rejection. In addition, recent progress made in silicon MEMS (microelectromechanical system) also led to successful demonstrations of high-Q silicon resonators and filters in millimeter-wave frequencies [17].

2) CDMA: The baseband (digital part) of the CDMA-interconnect transceiver, as shown in Figs. 15 and 16, comprises Walsh code generators, mixers, correlators, and registers. The FDMA/CDMA combined interconnect transceiver consists of both RF and digital circuits. The RF part of the interconnect transceiver is similar to that of the FDMA transceiver.

The Walsh code generator creates a set of mutually orthogonal codes as shown in Fig. 17. When n-bit Walsh codes are chosen, the maximum orthogonal codes generated are 2^n, which equals the total communication channels that can be simultaneously supported. Since Walsh codes are mutually orthogonal, there will be no cross-channel interference in a synchronous access operation. In this case, the BER of each channel depends only on the SNR of the receiver, as indicated in Fig. 12.

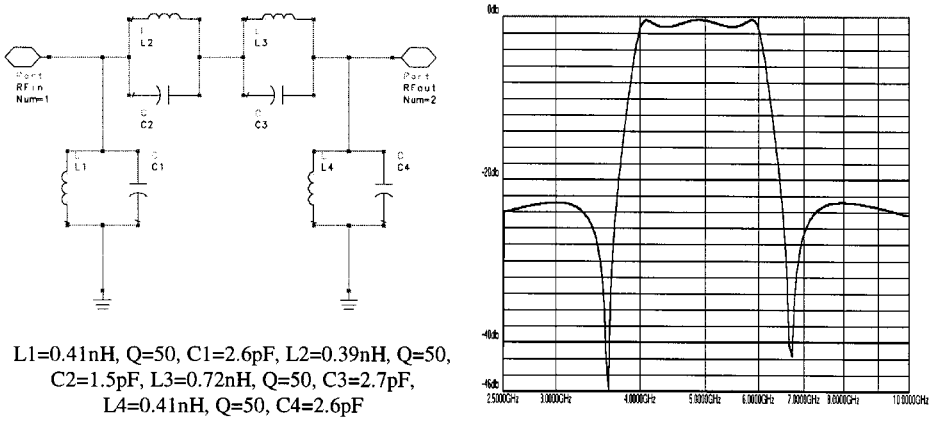


Fig. 14. Elliptic filter based on high-Q transformer type on-chip inductors.

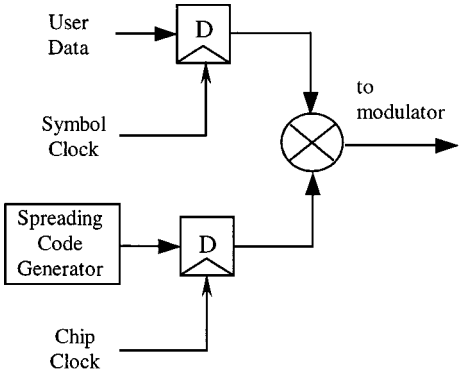


Fig. 15. Baseband CDMA transmitter.

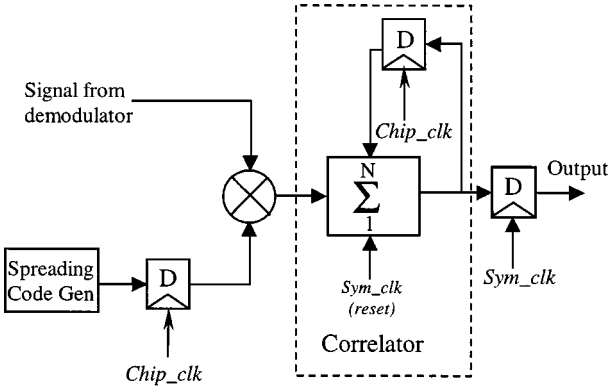


Fig. 16. Baseband CDMA receiver.

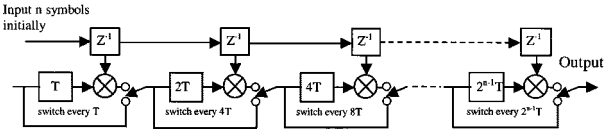


Fig. 17. N-bit Walsh code generator.

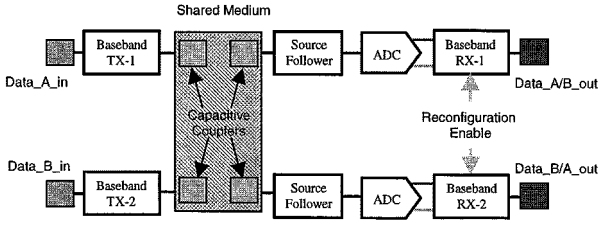


Fig. 18. Block diagram of 2 × 2 baseband CDMA-interconnect system.

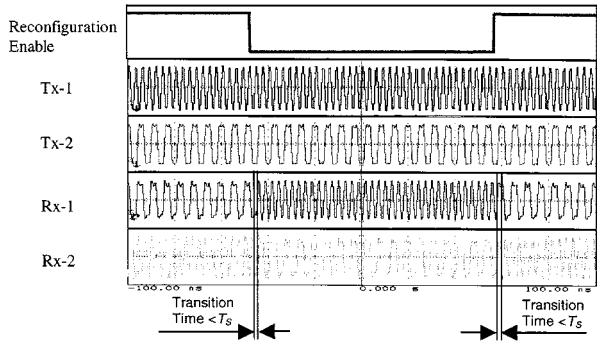


Fig. 19. Channels reconfigured seamlessly within one symbol period of T_s at $F_c = 2.8$ GHz.

III. RF-Interconnect Demonstration

As the first step to prove the RF/wireless-interconnect concept, we have recently demonstrated a 2 × 2 baseband CMDA-interconnect system on 0.35-μm and 0.18-μm CMOS [18]. As shown in Fig. 18, the CMDA-interconnect system comprises transmitters and receivers, T/R capacitive couplers, a shared transmission line, high-impedance receiver front-ends, ADCs, and a reconfiguration enable switch. In each transmitter Tx, input data is spread by Walsh codes and then transmitted in-and-out of a shared transmission line through T/R couplers. In each Rx, transmitted data are first quantized by the ADC and then despread by CDMA correlators. Reconfiguration-enable is implemented to alternate data paths between two communication channels. Fig. 19 shows measured results of designed 2×2 CDMA-interconnects based on 0.18-μm CMOS operating at a clock rate of $F_c = 2.8$ GHz. As shown in the same experiment, channels are seamlessly reconfigured within one symbol period of T_s, which fully demonstrates the interconnect reconfigurability on-the-fly. The power consumption is measured to be 15 mW per transceiver-pair at the clock rate of $f_{CLK} = 2$ GHz and $V_{dd} = 1.8$ V. The speed–power consumption relationship for future CDMA-interconnects is simulated in Fig. 20, according to the CMOS scaling rule of

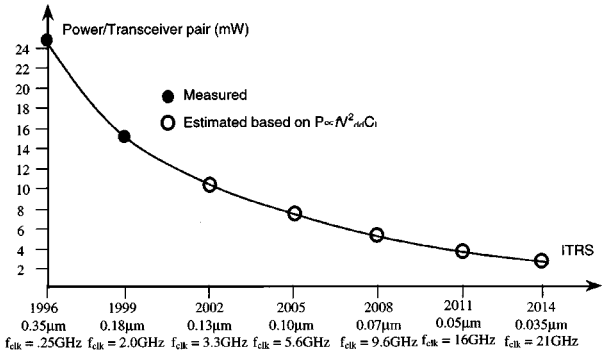
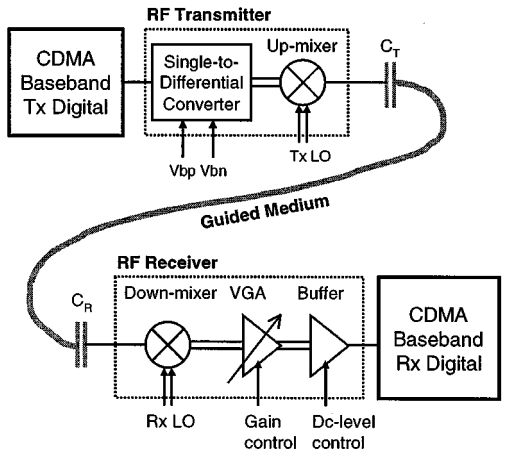
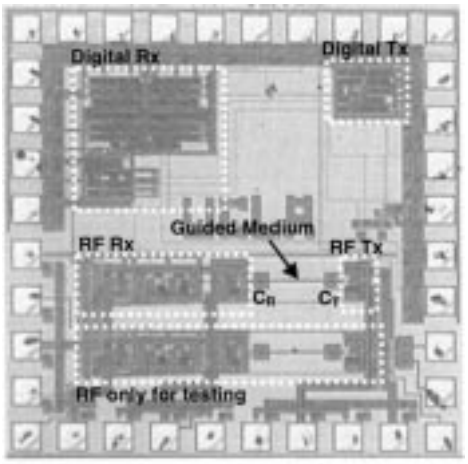


Fig. 20. Measured and simulated power consumption for CDMA-transceivers.



(a)



(b)

Fig. 21. (a) FDMA/CDMA combined interconnect system with CDMA baseband circuits with 5-GHz direct conversion RF transceiver. (b) Microphotograph for the fabricated test chip.

$P \propto fV_{dd}^2 C_L$ and the minimum power supply voltages and clock rates forecasted by ITRS [5].

An FDMA/CDMA-interconnect test system has also been demonstrated with a baseband CDMA-interconnect combined with a direct conversion 5-GHz RF transceiver as shown in Fig. 21(a) and fabricated chip in Fig. 21(b).

Fig. 22 shows receiver output waveforms with and without 5-GHz RF carrier. The clock rate for the baseband CDMA-

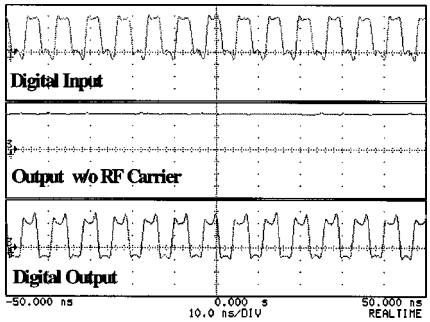


Fig. 22. Input and output waveforms of FDMA/CDMA-interconnect system with 5-GHz RF carrier.

interconnect is measured at 1.1 GHz with digital input data rate of 275 Mb/s per subchannel. The power consumption is measured to be 48 mW per transceiver-pair (15 mW for digital circuits and 33 mW for RF transceiver). This experiment demonstrates the functionality of the FDMA/CDMA-interconnect including RF and digital transceivers, signal coupling, and transmission.

IV. System Advantages

It is widely believed that further significant improvement in system performance can only be achieved through integration of different components of the system. This trend is clearly indicated in the rapid growth of system-oriented products, including complete systems on a chip, and/or MCMs. The major bottleneck in pushing the frontiers of system integration further into the new millennium, is the lack of availability of ultrabandwidth, multi-I/O, and reconfigurable networks that can be packaged on a single chip or integrated into the MCM. Let us briefly look at how the proposed RF/wireless interconnect scheme meets these architectural requirements, and how it compares with other existing or proposed schemes.

- ***Effective Bandwidth:*** Several research efforts on intra- and/or inter-chip high-speed interconnects have been pursued in the recent past. For example, high-speed end-to-end wire interconnects (with signal-processing hardware, such as channel equalizers, at both ends) for data transmission speeds up to 4–10 Gb/s have been successfully demonstrated [19]. However, such wire interconnect is often based on high-clock-rate time-domain multiplexing. To compensate for the signal loss over the wire, such a system would require sophisticated processing of the signal to compensate for frequency-dependent attenuation. In our proposed RF/wireless interconnect, the total data rate can go up to 100 Gb/s/interconnect or 20 Tb/s/chip (assuming 200 RF-interconnects, each 2 cm $\times$ 100 μm in size, are fabricated on a 2 cm $\times$ 2 cm chip) but the clock rates in each frequency band are maintained as 20–40 Gb/s, which significantly reduce the complexity in both RF and digital circuit design and implementation. It is only the RF transceivers that are required to operate at the carrier frequencies. This architecture takes full advantage of the fact that the RF circuits are operable up to $f_{\max}/2$ of the CMOS device while digital circuits can only operate up to $f_t/4$.

- ***Multi-I/O Service:*** Another important feature that many proposed schemes cannot offer is a high-integrity interconnect where multiple I/Os can communicate simultaneously. Using frequency and/or code division multiplexing, one can achieve multiple access in our scheme, while maintaining reliability. In fact, our simulations show that up to 20/20 I/Os can simultaneously communicate using one shared transmission line. From an architectural perspective, this enables the use of extensive parallel processing at the systems level, leading to faster overall processing speed. One can in principle achieve such a shared network using optical interconnects; however, the overheads incurred per I/O in terms of area, power, and integration difficulties may be more challenging compared with our RF-based scheme. Another advantage of our system is that it may enable the architect to cut down the number of I/O ports on a chip. Since one can use on-chip modulation schemes to interleave multiple data sets on the network, one I/O port can serve multiple I/O needs simultaneously.
- ***Reconfigurability and Online Computing:*** The architectural flexibility that is being increasingly demanded by applications is the ability to reconfigure any given hardware online. At the logic level, this is accomplished by using FPGAs, which can be programmed online to perform different functionalities. The reconfigurable network we are proposing, will add such flexibility at the system level as well. Since the whole network can be programmed via software instructions, one can envision a complete online rewiring of connections. In our system, CDMA or FDMA-CDMA combined (i.e., multicarrier CDMA) algorithms allow each I/O pair to choose an orthogonal address code. The address code can be electronically changed for interconnect reconfiguration. Assuming total frequency bandwidth $W = 100$ GHz and the average data rate per RF channel up to 20–40 Gb/s, the simultaneous access of 20 CDMA subchannel/per-interconnect with guaranteed performance may be achievable in an enclosed low-noise MCM environment.
- ***Programmable Fault-Tolerant Architectures:*** As devices are scaled down to nanoscale dimensions, an issue that is becoming increasingly important is that of fault tolerance. For example, a recent influential paper [20] proposes a fault-tolerant hierarchical architecture with fault tolerance incorporated down from the logic level to the top level of interconnects. The main idea is: instead of perfecting one's nano-technology to the extreme limit, where fabrication lines are going to cost billions of dollars, one could instead have inexpensive fabrication technology with potentially low yield. One can then use the architectural flexibility to program a virtual machine on the resulting hardware by first testing and then followed by reconfiguration. The key underlying enabling technology is the design of flexible interconnection network. While our ideas are not suitable for a programmable network at the nanoscale level, it definitely can be used at the system level to attain fault tolerance. As pointed out in the previous discussion, one can reconfigure the network by software commands (even remotely) to debug the system architecture and then to eliminate faulty units via reconfiguration.
- ***Packaging and System Assembly:*** The RF/wireless interconnect also allows greater flexibility in packaging and system assembly. With RF/wireless interconnects, the total number of bonding wires can be greatly reduced and the future ULSI can be nondestructively tested before packaging through RF signal sensing and diagnosis. The RF interconnects may provide the necessary dynamic testability required prior to assembling ULSIs into high yield MCM packages.
- ***Silicon Compatibility:*** Both RF/wireless interconnect system and components can be implemented based on a silicon-based CMOS technology, which is and will continue to be the mainstream of the future ULSI industry.

V. System Constraints

There are several system and practice issues and constraints that must be considered and resolved for implementing the proposed RF/wireless interconnect system. Those include the following.

- ***Circuitry Overhead and Power Consumption:*** If the network flexibility is the highest concern, e.g., both bidirectional communication and arbitrary transceiver distribution are of the top priorities of the RF/wireless interconnect system, then each I/O transceiver should have its own dedicated RF and CDR (clock and data recovery) circuits. This of course will impose heavy circuit overhead as well as large power consumption to the interconnect implementation. Practically, this may not be possible or even necessary for all RF/wireless interconnects. For most inter-chip interconnects, I/Os are often located in separate clusters. To reduce the power consumption, clustered Tx's within the synchronous access range may share a common RF transmitter as that in the cellular telephony, while clustered Rx's inputs may share a common RF receiver and even a shared CDR without sacrificing channel reconfigurability. The only nonsharable circuitry is the digital part of the transceiver. Fortunately, the real estate and power consumption of these circuits are insignificant with advanced CMOS, as demonstrated in Section II. It is also noted that the power consumption of Tx output stage, which is usually determined by the receiver sensitivity, does not scale as the digital circuitry. The Tx driver stage typically consumes 1$\sim$2 mW according to V_{dd}^2/R_T, where the V_{dd} is the power supply voltage and R_T is the transmitter output impedance.
- ***On-Chip Filtering:*** FDMA-interconnect requires high-quality bandpass filters for high spectrum efficiency as described in Section II. This requirement may be relaxed in a guided medium such as the proposed RF-interconnect compared with an open-air wireless system whose frequency usage is strictly limited by the Federal Communications Commission (FCC). In addition,

the communication channel may be further selected in the direct conversion receiver with low pass filters. The quality of bandpass filters at RF frequencies may be greatly relaxed as well.

- ***Off-Chip Components:*** Since the reference crystal oscillator needed for FDMA cannot be easily implemented on-chip and its size is relatively large compared with future ULSI, it appears as an issue. However, since the reference clock is always used in modern computer or communication systems, it is possible to reuse a reference clock in existing systems to minimize the off-chip overhead.

VI. Summary

Future ULSI interconnect system demands extremely high data transmission rate, multi-I/O service, reconfigurable and fault-tolerant computing/processing architecture, and full compatibility with mainstream silicon CMOS and MCM technologies. In this paper, we have presented a novel RF/wireless interconnect system that provides a unique solution to those system needs. Unlike the traditional "passive" metal interconnect, the "active" RF/wireless interconnect is based on capacitive coupling, low loss and dispersion-free microwave signal transmission, and modern multiple-access algorithms. The proposed RF/wireless interconnect promises ultrabroad bandwidth (100 Gb/s/interconnect or 20 Tb/s/chip), simultaneous multi-I/O communications and reconfigurable networking. As the first step to prove the feasibility, we have realized on-chip 2×2 CDMA- and FDMA/CDMA combined interconnects with 2.8-GHz clock and 5-GHz carrier based on 0.18-μm MOSIS CMOS, which demonstrates the intended functions of capacitive coupling, signal transmission, and channel reconfiguration on-the-fly.

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