# Design of Integrated Circuits for the Power Domain

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***Abstract:*** Until the late 80's, the only constraints when designing integrated circuits (IC's) were the area and speed. The field of low power design was confined to applications such as digital wrist watches or cardiac pacemakers. In the beginning of the early 90's, this changed rapidly with the growing demand for portable electronic equipment such as cellular phones and notebook computers. However, decreasing feature sizes and the demand for real-time processing systems have resulted in a level of miniaturisation where the heat dissipation is now the main problem. Here the trade-off between special packaging, capable of cooling the chip and expensive fan solutions has to be balanced against the consumer's demand for low cost applications. Furthermore, the recent demand for environmentally friendly consumer goods have pushed companies to design non-portable systems using low power techniques. This has resulted in increased market share for companies producing such 'green machines'.

## 1 Introduction

The low power design group of Dublin Institute of Technology and Trinity College Dublin focuses its work in two main areas: the design of high speed low power structures and the estimation of the power consumption at the earliest possible stages of the IC design cycle.

In the area of high level circuit design members of the group are investigating computational intensive high-speed designs such as real-time image processing and RISC processor implementations.

The microchip design activity has been ongoing in the department over the last 5 years. During this time various microchips were fabricated through the EU-funded initiative Eurochip. Sponsorship of Sun Microsystems in conjunction with funding from Forbairt enabled the installation of a network of state of the art CAD workstations. This work has taken place with the co-operation of Fachhochschule Dieburg, Germany, involving an exchange of researchers. Current projects include the development of a simulation tool using supercomputing resources provided by the Italian inter-university computing centre CINECA. Close links have been developed between the research group and the major companies in microchip design in Dublin. This has extended to the successful transfer of technology and design skills from industry to academia.

## 2 Theory

One of the main aspects of the research is the investigation of novel structures, which have a reduced power consumption without compromising performance. Most research in the area of low power CMOS design is focused on the lower levels of the design cycle. However, previous work of the group has shown that if low power design methodologies are applied at the earliest possible stages of the design cycle, the power consumption of the final microchip can be effectively reduced. Equation 1 shows the equation of the dynamic power dissipation

$$P_{Dynamic} = C_{active} \times V_{dd}^{\ 2} \times f_{clk} \qquad [1]$$

In this equation $f_{clk}$ represents the clock frequency at which the microchip is operating, $V_{dd}$ is the supply voltage. These two terms are often determined by the operating conditions. Therefore, the group is focusing on reducing the active capacitance. This term is the sum of all physical node capacitances multiplied by the number of times this capacitance is charged to the supply voltage. Equation 2 shows the equation for the active capacitance.

$$C_{active} = \sum_{0}^{number\ of\ nodes} \left( n_{(0,1)} \times C_{node} \right) \qquad [2]$$

At the higher levels of the design cycle the designer is unable to influence the node capacitance, $C_{node}$, and even at the lower levels it is a time consuming task and therefore uneconomic. As the group is working on new, practicable design methodologies, the work is concentrated on reducing the number of power consuming events. This is done by investigating the switching activity of traditional standard implementations and on developing structures with a lower active capacitance, without compromising other performance parameters such as speed or area.

## 3 Low Power Design Activities

This chapter will show two examples of how the power consumption of traditional implementation can be effectively reduced by developing new design structures. In this paper only the results are presented and the interested reader is encouraged to consult the given references or contact the authors for further information.

The first example presented in Figure 1, shows different methods of implementing the mathematical function arctan. The first bar in the graph shows the traditional implementation using the CORDIC algorithm. The other three bars show alternative methods developed by the group [1]. It should be noted that these new methods reduce the power consumption by a factor of 20.

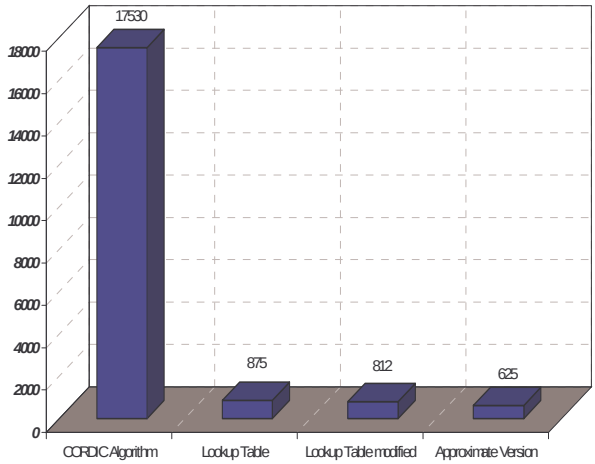


Figure 1: Power Consumption of different Arctan Implementations

Figure 2 shows the capacitance of shift registers (the capacitance is proportional to the power consumption). Here it was possible to reduce the switching, which ultimately causes the power consumption, almost to the theoretical minimum [2]. Figure 2 compares traditional implementations of shift registers (shift4, shift8, shift16) with the newly developed storage method (mux4, mux8 mux18). As seen in Figure 2, this leads to significantly reduced power consumption.

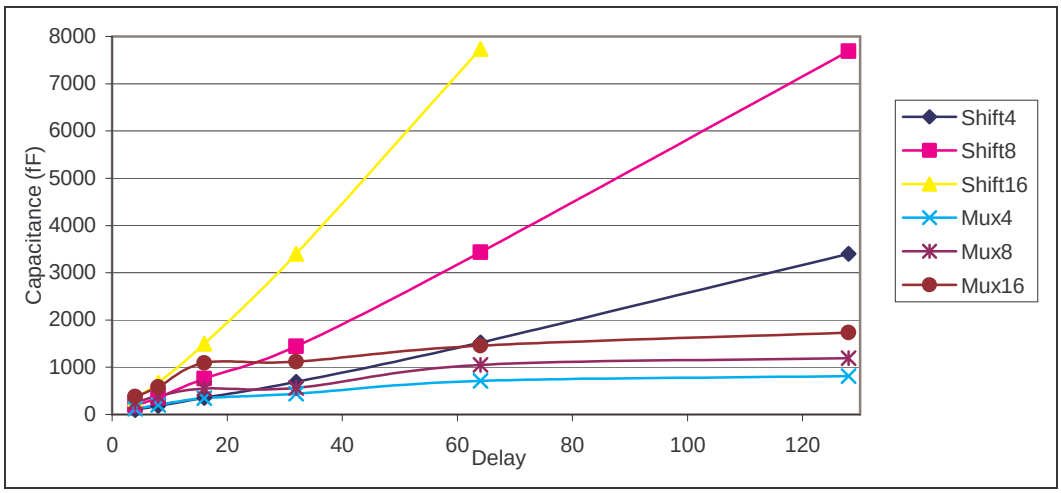


Figure 2: Capacitance of Shift Registers

## 4 Power Estimation

The second main area of interest is the estimation of the power consumption at the earliest possible stage of the design cycle. This research is again split into two main focus areas. The first is the development of a high-level power estimation tool and the second is the investigation and improvement of input vectors used for the simulation of the design.

### 4.1 Power Estimation Tools

The group has already developed a tool, PowerCount [3][4], capable of estimating the power consumption at the netlist level. This tool has several advantages over existing tools. It is fully incorporated into the normal IC design cycle. This means that the designer does not need to spend time in writing additional files. Only one additional file is needed for the computation of the power consumption and this file can be generated automatically within the design environment within seconds. The two most important advantages of PowerCount are the testing of the design within the first stages of the design cycles and the fast simulation times. This means that designers are able to test and compare the power consumption at a level where re-designs are still fast and therefore economical to perform.

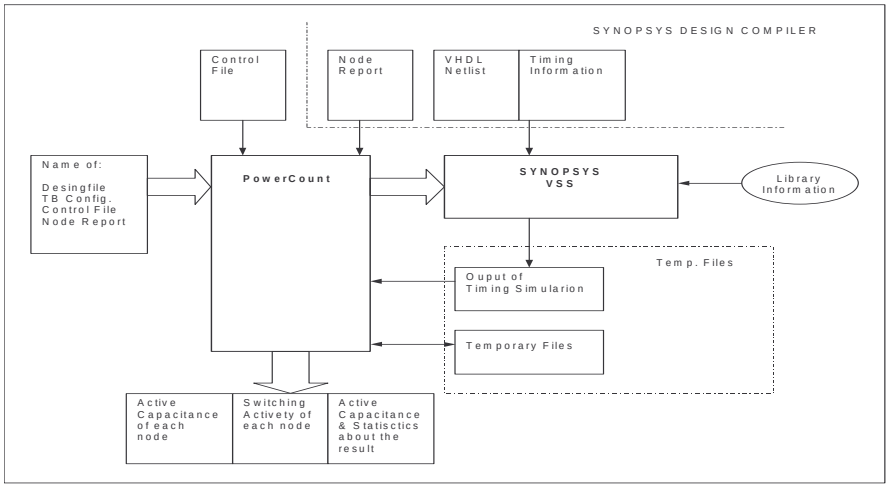


Figure 3 PowerCount in the IC Design Environment

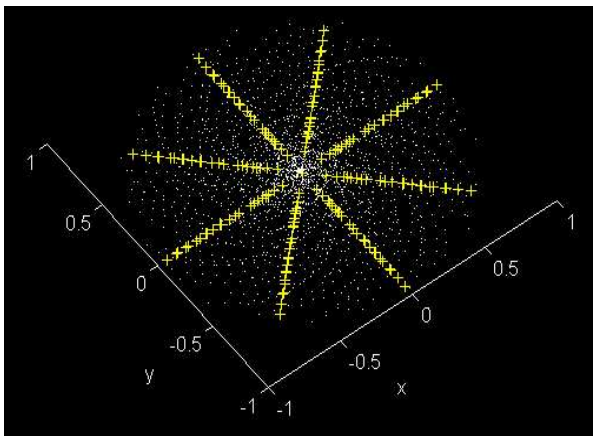


Figure 4a 3-d Structure of Digital Data

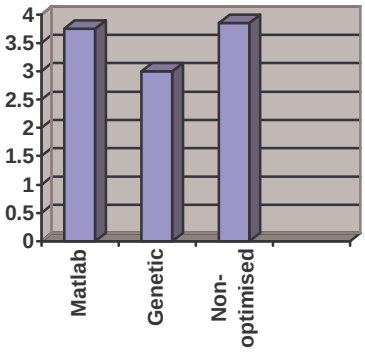


Figure 4b Improvement in Estimates

### 4.2 Effects of Input Vectors in the Power Estimation

While Nature contains many random processes, Science has yet to successfully mimic those processes by supplying a method for producing truly random numbers. The best that can be produced is a pseudo-random sequence, which can pass an arbitrary number of tests for randomness and which has sufficient statistical properties to make it 'look' random. Because VLSI systems have a finite number of inputs, any random digit must be truncated to form a binary input vector with a fixed number of bits. The effect of the truncation in the sequence can be easily visualised by plotting the truncated numbers in either 2- or 3- dimensional space, as shown in Figure 4a. The plotted vectors lie in a series of lines (in two dimensions) or in a family of planes or hyper-planes (in three or more dimensions). The closer the planes are to each other, the better the properties of the sequence [5]. This inter-planar distance is a good figure of merit when searching for a suitable pseudo-random generator. In general, the inter-planar distance is measured in six or more dimensions, to rigorously test the generator.

In order to verify the properties of the genetically-optimised generators with respect to the intended application domain of CMOS power estimation, a series of comparative power estimations was carried out. Firstly, the arithmetic circuit referred to previously was driven by a set of non-optimised generators and the power was repeatedly estimated with Monte Carlo simulations. The multiplier for each generator was chosen at random. The results are shown in Figures 5 and 6. Also included is the true power for the circuit. This was obtained using a known good generator within MATLAB, and will be used as a benchmark result. There is a considerable variation in the results obtained for the average power. In addition, the non-optimised generators appear to slightly underestimate the power consumption. The same circuit was then driven with a genetically-optimised generator. The power estimations were obtained under identical conditions, again with a Monte Carlo estimation technique. For these results there is a much closer correspondence between the reference value and the values obtained from the genetically optimised generator.

Another feature of the genetically-optimised generators is seen by examining the average number of iterations required for the power estimation to converge. A lower number of simulation runs was observed for the genetic generator, while the non-optimised generators had a larger number of average runs. This means that the genetically optimised generators reach their final answer more quickly, and also with greater accuracy. The average number of runs required for convergence of the Monte Carlo simulations is shown in Figure 4b. The optimised generator has the best performance.

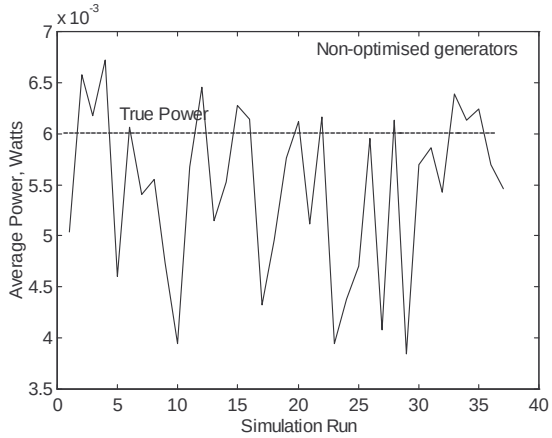


Figure 5 Power estimation with non-optimised generators

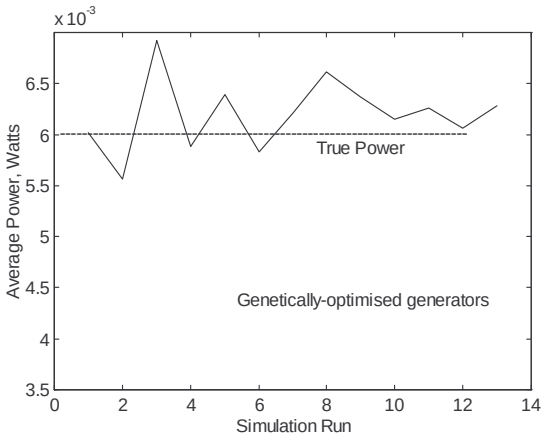


Figure 6 Power estimation with optimised generators

## 5 Conclusions

The principal objective of the VLSI research group at DIT Kevin Street is the investigation into, and the development of, low power silicon architectures. In order to further these aims, substantial effort has been applied to the design of software tools for the prediction of the power consumption of microchips before their fabrication. This has resulted in the tools PowerCount and LLAMA, which have been recently presented at a number of international conferences. The group has also examined the mathematical properties of digital data necessary for power estimation. Visualisation of these signals in 3 dimensions has enabled the formulation of a system for the synthesis of digital signals with improved statistical properties. When incorporated into PowerCount and into the circuit level Monte Carlo estimation tool, LLAMA, this enhanced data has resulted in quicker and more accurate power estimates. Current research is focussed on energy efficient architectures for real-time video applications and on control structures to be incorporated into a low power microprocessor implementation.

## References

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[2] A.Th. Schwarzbacher, P.A. Comiskey and J.B. Foley, "Improving the power consumption in image processing algorithms," *UK Low Power Forum*, Sheffield, September 1998.

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