Engineering Band-Edge High-κ/Metal Gate n-MOSFETs with Cap Layers Containing Group IIA and IIIB Elements by Atomic Layer Deposition

H. Jagannathan a, L. F. Edge a, P. Jamison a, R. Iijima b, V. Narayanan c, V. K. Paruchuri a, R. D. Clark d, S. Consiglio d, C. S. Wajda d, G. J. Leusink d

a IBM Research @ Albany NanoTech, 255 Fuller Rd, Albany, NY 12203, USA.
b Toshiba America @ Albany NanoTech, 255 Fuller Rd, Albany, NY 12203 USA
c IBM Research, T.J. Watson Research Center, Yorktown Heights, NY 10598, USA.
d TEL Technology Center, America, 255 Fuller Rd, Albany, NY 12203, USA

This paper presents studies performed in engineering high-κ metal gate stacks by using capping layers containing Group IIA and IIIB elements. Both high-κ gate dielectric (HfO₂) and capping materials, namely, the oxides of barium, lanthanum and yttrium are deposited by atomic layer deposition (ALD) to offer superior process control and flexibility. Position specific insertion of cap layers into the gate stack is studied and the device tradeoffs are highlighted. The magnitude of threshold voltage shift is correlated to the electronegativity of the cap layer species and its relative position in the gate stack. For a given cap position, BaO provides the maximum threshold voltage shift with the highest penalty in carrier mobility, followed by La₂O₃ and Y₂O₃ caps. Both lanthanum and barium incorporation into the high-κ gate stack provides a Tinv scaling benefit. Ozone based ALD processes are shown to adversely impact Tinv scaling due to the re-growth of the interface layer between the high-κ and the silicon substrate. This penalty is exacerbated in gate stacks with cap layers situated directly below the high-κ film. Significant improvements in Tinv scaling are obtained by migrating to a water based ALD process.

Introduction

The use of capping layers in conjunction with high dielectric constant (high-κ) gate dielectrics has been actively pursued to obtain band-edge (BE), scaled CMOS devices. Materials containing group IIA and IIIB elements (e.g. MgO and La₂O₃) have been of specific interest for BE n-type field effect transistor (n-FETs) devices (1-4), while Al₂O₃ (5) and TiO₂ capping layers have been investigated as viable p-type field effect transistor (p-FET) options. With increasing reports of cap incorporation within high-κ dielectrics and a multitude of elements being investigated, the need to have a clear understanding of the mechanism of threshold voltage (Vt) shifts and device dependencies is now greater than ever. Accordingly, this paper presents a systematic study examining the use of La₂O₃, Y₂O₃ and BaO as capping layers to tune the threshold voltage of nFET high-κ metal gate devices. Both high-κ (HfO₂) and capping layers are deposited by atomic layer deposition (ALD). The use of an all ALD process to form the gate stack provides excellent flexibility and precision in controlling the composition of the gate dielectric as well as the positioning of the capping layer in the stack. Empirical results from gate-first nFETs emphasize the need to recognize the importance of the group electronegativity of...
the different material species in the gate stack. The degree of threshold voltage shift and mobility impact is directly correlated to the electronegativity of the cap layer species. Furthermore the importance of using optimized ALD conditions and processes for high-κ and cap layer deposition is highlighted in obtaining gate stacks with tunable threshold voltage, competitive scaling and low gate leakage. Understanding the dynamics of the various elements will be critical in engineering the desired high-κ metal-gate devices for upcoming device technologies.

**Experimental Details**

**ALD Growth**

The system used in this study consists of a traveling wave-type geometry counter-flow ALD system with horizontal flows of precursor and oxidant across the wafer that was previously described (6). HfO\textsubscript{2} growth was performed by an ALD process using tetrakis(ethylmethylamido)hafnium (TEMAH) with ozone as an oxidant and this process exhibited a steady-state growth-per-cycle of \( \sim 0.8 \) Å/cycle. For deposition of La and Y oxides the La precursor used was the tetraglyme adduct of the La \textit{beta}-diketonate precursor tris(2,2,6,6-tetramethylheptanedionato)lanthanum (La(THD)\textsubscript{3}•TGLM), while the Y precursor utilized was the triglyme adduct of the analogous Y complex (Y(THD)\textsubscript{3}•TRGLM) using ozone as an oxidant. The characteristics of the ALD processes used for Hf, La and Y oxides have been described in detail previously (7). The deposition of BaO was performed utilizing a solution of a Ba ketoiminate complex, bis(2,2-dimethyl-5-(2-(2-(dimethylaminoethyl)(methylamino))ethyl-imino)-3-hexanonato)barium (BaON\textsubscript{3}) in mesitylene delivered by a direct liquid injection (DLI) system in conjunction with either water or ozone as an oxidant at 290 °C wafer temperature.

![Figure 1: Growth versus cycles of La\textsubscript{2}O\textsubscript{3} and Y\textsubscript{2}O\textsubscript{3} films using O\textsubscript{3} oxidant and BaO using O\textsubscript{3} or H\textsubscript{2}O oxidant on chemical oxide (SiO\textsubscript{2}).](image1)

![Figure 2: Overlaid RBS spectra confirming the presence of Ba (30 ALD cycles with H2O), La (80 ALD cycles with O3) and Y (80 ALD cycles with O3) on chemical oxide. Inset shows the La3d\textsubscript{5/2} and Ba3d\textsubscript{5/2} core level spectra measured by XPS for the corresponding films.](image2)
Figure 1 shows the growth characteristics of BaO, La$_2$O$_3$ and Y$_2$O$_3$ films on a chemical oxide (SiO$_2$) interfacial layer. The condition of each ALD process was tuned to obtain reasonable film uniformity and a linear relationship between the film thickness and ALD cycles was obtained, consistent with an ALD mechanism. The films deposited were analyzed by XPS and RBS to confirm the absence of metallic impurities as can be seen from the spectra in Figure 2. The presence of metallic impurities in these films is below the detection limit of RBS.

**Device Fabrication**

The steps involved in the fabrication of capped high-$\kappa$ dielectric nFETs are outlined in Figure 3. The fabrication begins with the preparation of the interface layer (IL) followed by the ALD of HfO$_2$ and capping (La$_2$O$_3$, Y$_2$O$_3$ or BaO) layers (< 2 nm in thickness). The desired gate stacks with bottom, middle and top caps are obtained by tuning the sequence of deposition during ALD. The use of ALD for high-$\kappa$ and cap deposition provides the maximum flexibility in engineering the desired gate dielectric. The gate stack deposition process is succeeded by the deposition of TiN and poly-silicon and followed by typical gate first processing steps involving gate RIE, extension implants, spacer formation and Source/Drain implantation. The devices are subjected to a rapid thermal anneal (RTA) at 1000 °C and is followed by salicidation of the source, drain and gate regions of the device. The MOSFETs are annealed in forming gas for 30 minutes at 450 °C prior to electrical characterization.

Figure 3: Gate-first process flow for the fabrication of position-specific cap layers in gate stacks of n-MOSFETs.
Results and Discussion

Capacitance-Voltage (CV) measurements were performed to characterize the impact of the different cap layers in the gate stack. Figure 4 describes the results of these measurements where increased cycles of Ba (C3=2+C2 cycles and C2=2+C1 cycles), La and Y (C3=3xC1 cycles and C2=2xC1 cycles) were used to deposit the cap layer above HfO2. The three cap layers (BaO, La2O3 and Y2O3) were found to induce a parallel shift of the CV curves towards negative voltages (reduction in $V_t$) with respect to a reference device containing only HfO2. The quantity of $V_t$ shift in the devices among different species of caps is commensurate to the electronegativity and thickness of the capping layer. With an increased amount of capping layer (higher ALD cycles), an increased $V_t$ shift is observed. However, though the physical thickness of the capping layer has a linear relationship to the number of ALD cycles, characteristic of ALD growth as shown in Figure 1, the $V_t$ shift tends to saturate with increased ALD cycles of the capping layer. In addition to the $V_t$ shift, the introduction of each cap layer species into the high-$\kappa$ dielectric has a clear and observable impact on the scalability of the gate stack. BaO provides the most scaling observed by an increase in the inversion capacitance followed by La2O3 caps. Y2O3 on the other hand provides little to no scaling benefit.

Figure 4: Capacitance-Voltage characteristics of HfO2 gate stacks incorporated with (a) BaO (b) La2O3 and (c) Y2O3 deposited above the high-$\kappa$ layer as a function of ALD cycles. (measured @ 1 MHz)
Position Dependence of Capping layers

The specific impact of introducing capping layers in localized regions of the gate dielectric was further studied. Figures 5, 6 and 7 outline the CV characteristics and electron mobility measured from nFET devices with cap layers inserted below, in between and above the high-κ layer respectively. To perform a fair comparison among different capping layers in this study, ALD cycles for Ba, La and Y (using the ozone process) were chosen so as to obtain an equivalent thickness of the cap layers based on their respective growth rates as discussed in Figure 1.

![Figure 5](image_url) (a) Capacitance-Voltage characteristics (@ 1 MHz) and (b) electron mobility (@ 1 MV/cm) of gate stacks with BaO, La₂O₃ and Y₂O₃ deposited below the high-κ layer.

![Figure 6](image_url) (a) Capacitance-Voltage characteristics (@ 1 MHz) and (b) electron mobility (@ 1 MV/cm) of gate stacks with BaO, La₂O₃ and Y₂O₃ sandwiched between the high-κ layer.
Figure 7: (a) Capacitance-Voltage characteristics (@ 1 MHz) and (b) electron mobility (@ 1 MV/cm) of gate stacks with BaO, La2O3 and Y2O3 deposited above the high-κ layer.

The threshold voltage dependence was found to not change by the movement of the cap layer position among different cap layer species. However, in general for a given cap layer, the most Vt shift was obtained with the bottom caps followed by caps situated in the middle of the high-κ and with the least Vt shift obtained from caps deposited above the high-κ dielectric. The most Vt shift towards nFET band-edge (BE) was obtained from BaO which is the most electropositive among the three cap layers. The electron mobility degradation was also observed to follow the same trend as the Vt shift with the BaO caps having the most mobility degradation. However, the degree of mobility degradation of the bottom BaO and bottom La2O3 were observed to be lower compared to the middle and top capped samples. This observation was attributed to the re-growth of the interface layer between the silicon channel and the high-κ layer. This observation is further supported by the corresponding CV measurements in these devices. Figure 5(a) shows the reduction in inversion capacitance for both bottom BaO and bottom La2O3 caps compared to their middle and top cap counterparts in Figures 6(a) and 7(a). The trade-off existing between Vt tunability, carrier mobility and Tinv scalability with cap layers can be appreciated from these observations in this study and provide design latitude based on the device and technology requirements.

Dependence on ALD process

With the observation of interface layer re-growth being prominent in bottom caps, studies were performed to improve the ALD process to inhibit such re-growth. Figure 8 compares an ozone based ALD BaO process to a water based ALD BaO process. The splits with a bottom BaO cap in the ozone process clearly show a lower inversion capacitance and corresponding higher Tinv. The top, bottom and middle cap samples using the water ALD process all have similar Tinv but have lower overall threshold voltage shift which could be due to a lower deposition rate in the water process compared to the ozone process as shown in Figure 1. However all the splits in the water based ALD process provides superior Tinv scaling. These results highlight the use of an optimized ALD process in obtaining a tunable and yet scalable gate stack. For the La and Y precursors used in this study, an H2O process was not feasible due to the low reactivity of these sources.
Figure 8: Capacitance-Voltage characteristics (@ 1 MHz) comparing the BaO ozone and water process. The water process shows more scalable gate stacks with negligible re-growth.

The overall response of $V_t$ and electron mobility to the different capping layers explored in this paper is summarized in Figure 9. Y$_2$O$_3$ caps provide a $V_t$ shift of $\sim$200 mV with respect to HfO$_2$ only devices while La$_2$O$_3$ caps provide a shift of $\sim$300 mV. The water and ozone BaO caps provide a large $V_t$ shift of $\sim$900 - 1200 mV moving the nFET devices well beyond BE. The scaling trends of these gate stacks are shown in Figure 10 where the increase of $T_{inv}$ in bottom capped samples using the ozone process is clearly visible. This reduction in re-growth resulting in $T_{inv}$ $\sim$ 11 Å can also be observed in the devices with BaO caps using the ALD water process. In addition, locating the capping layers in the middle of the high-$\kappa$ provides the best trade-off in scaling and gate leakage and with little compromise in the $V_t$ shift.

Figure 9: Threshold voltage and electron mobility (at 1MV/cm) as a function of cap layer type and position.

Figure 10: n-MOSFET gate leakage (at 800 mV overdrive) as a function of $T_{inv}$ for different cap layers and position in the high-$\kappa$ stack.
Mechanism of Threshold Voltage Shift

The mechanism of voltage shifts obtained by the incorporation of capping layers in high-κ materials can be explained by the differences in the group electronegativity (EN), between the capping and high-κ layers (4,8) with respect to SiO₂. Table 1 (adapted from 4, 8) lists the Pauling’s elemental EN for Si, Hf, Ba, La and Y along with the group EN values of their corresponding oxides. The group EN is obtained by applying the Sanderson’s definition (9) which is calculated by the geometric average of the elemental EN values in the oxide. It can be seen that BaO has the largest difference in group electronegativity with respect to SiO₂ followed by La₂O₃ and then by Y₂O₃. The most electropositive cap layer tends to provide the maximum threshold voltage shift from empirical data due to the higher strength in the dipole formed. In addition to threshold voltage shift it is expected that the stronger dipole would impart a higher penalty in carrier mobility. This too is clearly observed in the BaO, La₂O₃ and Y₂O₃ capped systems as discussed in the earlier sections. The use of group electronegativity to explain the origin of threshold voltage shifts has been reported for several element systems using materials that provide both nFET and pFET Vₜ shift (4). However, recent reports (10) also highlight the importance in recognizing the differences in the areal density of oxygen between the high-κ and SiO₂ IL. Though a consensus is yet to be reached on the true origin of the Vₜ shifts in these systems it is evident that there is a strong relationship between group EN and the areal oxygen density in these systems.

<table>
<thead>
<tr>
<th>Element</th>
<th>Pauling Electronegativity</th>
<th>Dielectric Cap</th>
<th>Geometric Mean Electronegativity (Sanderson Criterion)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ba</td>
<td>0.89</td>
<td>BaO</td>
<td>1.75</td>
</tr>
<tr>
<td>La</td>
<td>1.1</td>
<td>La₂O₃</td>
<td>2.18</td>
</tr>
<tr>
<td>Y</td>
<td>1.22</td>
<td>Y₂O₃</td>
<td>2.27</td>
</tr>
<tr>
<td>Hf</td>
<td>1.3</td>
<td>HfO₂</td>
<td>2.49</td>
</tr>
<tr>
<td>Si</td>
<td>1.9</td>
<td>SiO₂</td>
<td>2.82</td>
</tr>
<tr>
<td>O</td>
<td>3.44</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 1: Pauling electronegativity of cap elements along with the group electronegativity of their respective compounds.

Conclusion

High-κ metal gate n-MOSFETs containing group IIA and IIIB elements, namely, La-, Y- and Ba-containing cap layers were studied as a function of position in the HfO₂ gate stack. Both the cap layers and high-κ dielectric were deposited by ALD. BaO caps provided the maximum Vₜ shift followed by La₂O₃ and Y₂O₃ caps. Both BaO and La₂O₃ caps provided T_inv scaling compared to gate stacks containing no additional capping layer. The location of capping layers in the middle of the high-κ stack results in lower gate leakage for a given T_inv and Vₜ shift. The degree of Vₜ shift obtained from these cap layers was related to the group electronegativity of the cap layers with the most electropositive layer (BaO) providing the most nFET Vₜ shift. The mobility degradation and T_inv scaling were also found to be correlated to the electronegativity of the cap species. For BaO, a water based ALD process was developed and was found to be superior compared to an
ozone based ALD process. These studies and tradeoffs will help in enabling the engineering of optimized high-κ gate stacks in CMOS integrated circuits.

Acknowledgments

The authors would like to thank S. Guha for helpful discussions. This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

References